Introduction

ClockMatrix provides many tools for managing timing references. It has several different modes to align output clocks, control skew, measure clocks, select clock sources, and have independent timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks.

Typical large telecom system consists of Line Cards (LCs), Routing/Switching Processors (RSPs), Timing Cards (TCs), Fan Trays, back/mid-planes, and/or switching matrices. Some of these functions can be combined in the same cards; for example, RSP can have TC functionality as well. If such system needs to participate in network timing distribution, then it is expected that they support SyncE and IEEE1588 standards. It is also expected that these system contribute very little constant Time Error (cTE) noise to the network clock.

This document addresses how to use ClockMatrix’s reference monitors and independent System DPLL for applications that require nCXO (compensated XO) redundancy using ClockMatrix.

Why have nCXO Redundancy?

Most PLL architectures use a single nCXO for operation. This nCXO is not only for normal DPLL operation but used as a system clock to perform many of the other features required for today’s sync applications, such as input reference monitoring and holdover.

For Telecom, the nCXO provides a stable frequency backup on the loss of network synchronization. For redundancy in chassis-based systems, the TC functionality is duplicated, thus, there would be a need for two nCXOs in the system to provide this backup. With OCXOs (Oven-Compensated XO) and their passive components, there is an increased chance of failure of the nCXO. For this reason, it is becoming desirable to use the alternate/secondary TC’s nCXO as a backup to the local nCXO.

Because the local nCXO is also used for clock monitoring, with nCXO redundancy, it makes it very difficult to do the following:

- Detect if something is wrong with the local nCXO itself (i.e., single point of failure for the timing system)
- Switch, if one could detect such a failure, to a redundant nCXO with minimal impact to the rest of the system (e.g., no unnecessary transients/glitches on the other clock outputs)

With ClockMatrix’s SysDPLL architecture, all of the above points can be addressed to provide nCXO redundancy within the system.

Per-Input Reference Monitors (REFMON)

The ClockMatrix Reference Monitor uses the SysDPLL as the measurement clock for the short-term (LOS), mid-term (activity) and long-term (frequency) monitors. Each of the sixteen CLKn inputs can have its own independent setting each monitor’s threshold, along with independent masking of either monitor to determine if the input is qualified or disqualified. XO_DPLL is a clock input itself but there is not the same monitoring capability on this input, as discussed below.

REFMON Measurement Clock Source

The SysDPLL provides the measurement clock for the reference monitors. The SysDPLL typically locks to the XO_DPLL input, which is connected to a local nCXO – TCXO (Temperature-Compensated XO), OCXO, etc. – and provides a stable clock source for these measurements. As previously mentioned, there is no monitoring on the XO_DPLL pin, thus, the SysDPLL will track this clock as long as it is within its DCO range (±244PPM). If the clock at XO_DPLL is lost (squelched high/low or tri-stated), the SysDPLL will follow the last phase offset seen, thus, eventually rail at ~1.5%. Optionally, the SysDPLL can lock to any of the 16 input clocks, which would then allow the use of the reference monitor to qualify/disqualify the input. This is discussed more in the following sections.
**nCXO Monitoring**

The simplest clock monitor is for LOS, but unfortunately XO_DPLL does not have LOS detection. If you want to avoid this limitation then it is recommended to put the local nCXO on a CLKn input so that it can use the available LOS monitoring. This will allow the SysDPLL to go into Holdover on LOS. See Figure 1 below. All other reference inputs should also use LOS monitors, or use an external LOS signal to trigger LOS via GPIO for the CLKn that is associated with that GPIO.

Activity monitoring is useful for identifying a toggling clock at the input; however, its precision is likely not enough to identify any failure of an nCXO (range is from 1000PPM down to 12PPM). For this reason, activity monitoring is best used to qualify recovered line clock sources (i.e., SyncE) or to detect large, quick FFO transients (i.e., > 12PPM in 1.25ms).

Frequency monitoring measures the FFO between the clock and the measurement source (SysDPLL). To acquire precision in this measurement, longer measurement windows are used (i.e., seconds). Since the maximum frequency accuracy of the nCXO is known, this can be used to determine if there is an unexpected offset detected. For example, if the nCXO is accurate to ±1.5PPM over 25 years and the backup has the same accuracy, then you know the FFO measured should always be between ±3PPM. By adding a second source, such as a SyncE clock traceable to PRC (10-11), you can use this to determine which nCXO is out of specification. Even if the second source is not traceable to PRC (Primary Reference Clock), its short-term accuracy should be sufficient (e.g., G.8262 option 1 is ±2PPM over 24hrs).

To simplify the above, the local nCXO can also be placed on a CLKn input. Although this would mean its FFO value would always be 0PPM, it may make the voting system easier as the relative offsets of all three sources would be easily calculable, even after a switch to the redundant nCXO or when adding additional monitoring sources (i.e., GNSS).

---

**Figure 1. ClockMatrix GUI Showing Local nCXO on a CLKn Input**
nCXO Error Detection

Since the SysDPLL is typically locked to the local nCXO via the XO_DPLL pin, it is difficult to detect if there is an issue with the nCXO connected to XO_DPLL. However, by comparing other sources in relation to the SysDPLL, such as a redundant nCXO or SyncE, you can determine if the nCXO is the source of the failure.

For example, let’s say you have an alternative nCXO on CLK0 and a SyncE source on CLK1. Let’s also assume both nCXOs have a long-term accuracy of ±4.6 PPM. Since the SysDPLL will be locked to the local nCXO on XO_DPLL, it will also have an accuracy of ±4.6 PPM. We can then use the Reference Monitors for CLK0 and CLK1. For CLK0, since the alternative nCXO has the same long-term accuracy, we would expect a value for the frequency (long-term) monitor to be < 9.2 PPM. For CLK1, since the SyncE source is traceable to PRC, we would expect a value for the frequency (long-term) monitor to be < 4.6 PPM. With these two values, a voting system can now be performed to detect if any of those monitors exceed an expected threshold. In addition, the LOS (short-term) monitor can be used to detect a loss of clock, along with the Activity (mid-term) monitor to detect any quick, large transients.

To determine if there is an issue with XO_DPLL, review both the CLK0 and CLK1 monitors. To simplify, you can bring the local nCXO to a clock input (i.e., CLK2) as displayed in Figure 2. This will allow you to complete three-way relative comparisons between the three (or more) clock sources. This will also allow you to take advantage of the LOS and Activity monitor on the local nCXO to quickly disqualify the clock to the SysDPLL.

In Table 1, the input frequency offset monitors are used to measure the Fractional Frequency Offset (FFO) for CLK0 (-4.6ppm), CLK1 (0ppm), and CLK2 (+4.6ppm) when CLK0 and then CLK2 are used as the SysDPLL source. As shown in the figure, the FFO is 0ppm for CLK0 when the SysDPLL has CLK0 as the source. The FFO is 0ppm for CLK2 when the SysDPLL has CLK2 as the source.

Figure 2. Test Setup for nCXO Error Detection

<table>
<thead>
<tr>
<th>Input</th>
<th>FFO (ppb)</th>
<th>SYSDPLL Source</th>
<th>Input</th>
<th>FFO (ppb)</th>
<th>SYSDPLL Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK0</td>
<td>0</td>
<td>CLK0</td>
<td>CLK0</td>
<td>-9200</td>
<td>CLK2</td>
</tr>
<tr>
<td>CLK1</td>
<td>4600</td>
<td>CLK0</td>
<td>CLK1</td>
<td>-4600</td>
<td></td>
</tr>
<tr>
<td>CLK2</td>
<td>9200</td>
<td>CLK0</td>
<td>CLK2</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Table 1. Input Monitor Results
nCXO Error Recovery

Once an error/failure is identified, that clock source can be immediately disqualified. If that clock source is the current SysDPLL source then the SysDPLL will go into Holdover. At this moment, any channel using the SysDPLL for stability will fall back on the XTAL (SysAPLL). For this reason it is important to switch very quickly to an alternate source.

To minimize impact to the other channels’ outputs, you should not just switch to the redundant source. Even with hitless switch (i.e., to absorb the phase offset), there will be a frequency offset between the previous source and the new source (in the example above, it could be up to 3PPM). To manage this, there are a couple of options:

1. Use the ClockMatrix’s fast frequency lock capability, which can perform a frequency slope (change) limit (ppb/s) when re-locking to the new source.
2. Use the combo bus filter when using the SysDPLL as a combo source.

IDT recommends to use the first option, as the latter will have an impact on the combined phase noise of the channel’s outputs (since you are further filtering the SysDPLL, thus, losing the benefit of the nCXO’s close-in PN). Figure 3 shows the impact of switching from a local nCXO (±4.6ppm) to a redundant nCXO (±4.6 ppm) for the clock source of SysDPLL using the suggestion in option 1. The SyncE output is monitored during the switch for G.8262 Option 1. The maximum ppm offset would be 9.2ppm but during the test it would be random. The displayed in the figure show a phase hit of less than 60ns for a random frequency offset between the local and redundant nCXO. If you have additional questions about device configurations, please contact IDT application support at support-sync@idt.com.

Figure 3: Phase/FFO Plots of Switching from Local nCXO to Redundant nCXO for the SyncE Output
## Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>November 5, 2018</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
   - **Standard**: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   - **High Quality**: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of semiconductor products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0.1 November 2017)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.