Introduction

MicroClock clock generators are very small devices that consume very little power, and all devices in the family are suitable for portable and wearable applications. The power consumption is not determined by the circuit inside the MicroClock device only, the circuit external to the device also has an influence on the power consumption. This application note explains how to configure MicroClock devices and application circuits to optimize for power and other important parameters. IDT's Timing Commander software can help configure the programming settings and will be useful when optimizing for power consumption.

Table 1. MicroClock 5X1503/5L1503 Family of Products

Product	Description	Package
5L1503	Standard MicroClock device.	10-DFN
5L1503L	Ultra Low Power MicroClock device.	10-DFN
5L1503S	Spread Spectrum capable MicroClock device.	10-DFN
5X1503	Standard MicroClock device with integrated crystal.	10-DFN
5X1503L	Ultra Low Power MicroClock device with integrated crystal.	10-DFN
5X1503S	Spread Spectrum capable MicroClock device with integrated crystal.	10-DFN

All MicroClock devices have the same small 2 x 2 mm 10-DFN package. The "5X" devices save extra space with the integrated crystal, making them very suited for Wearable applications.

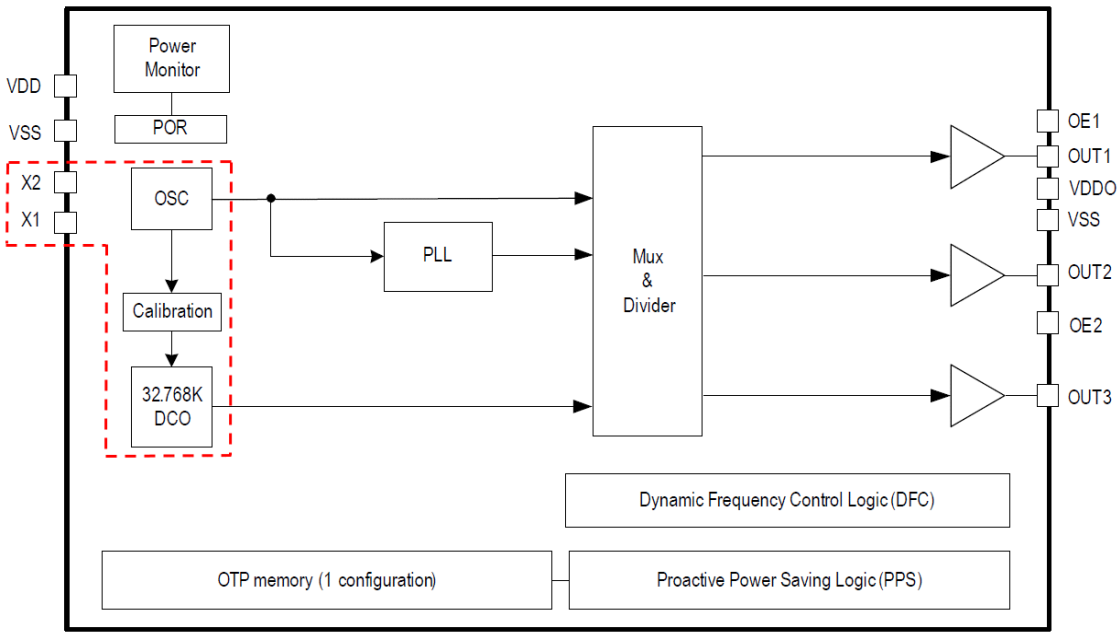
The 5L1503L and 5X1503L achieve ultra low-power when outputting only 32.768kHz by controlling the output amplitude on the OUT1 = 32.768kHz output. All MicroClock devices can control the OUT2 and OUT3 amplitude.

Ultra Low-Power Operation

The MicroClock device can operate with ultra low-power with only a 32.768kHz output. This is possible because of the ultra low-power DCO. The DCO is a dedicated 32.768kHz oscillator. The DCO itself lacks the accuracy required for the 32.768kHz clock but it is semi-locked to the internal or external crystal. Ultra low-power is achieved by running the crystal for just a few milliseconds to line up the DCO, and then turn it off for a few seconds until the next alignment. When the DCO was slightly too slow at one alignment, the DCO will be set slightly faster for the next alignment cycle to catch up on the total amount of clock pulses. This way, the average 32.768kHz clock accuracy is the same as for the internal or external crystal and the 32.768kHz clock can be used for Real Time Clock applications.

See Figure 1 for the MicroClock device block diagram. The blocks involved with the 32.768kHz clock are outlined in red.

Figure 1. MicroClock Device Block Diagram



Designing and Configuring for Low Power

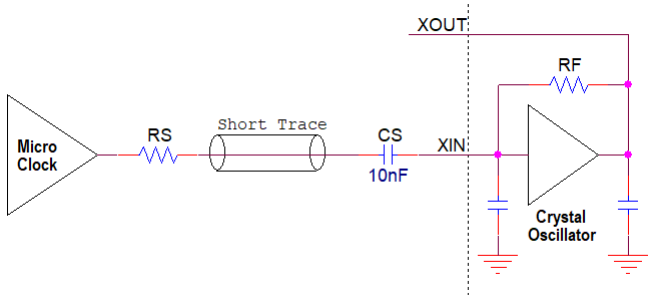
The MicroClock devices have special features for lowering power but it is also important to optimize the circuit design around the MicroClock device for low power. For example, clock output loading affects how much power is used by the output driver.

Clock Trace Length: An important part of the clock output loading is the clock trace. The longer the clock trace, the bigger the loading from the clock trace and the bigger the supply current in the clock output driver. The clock trace can be viewed as a transmission line (50Ω) or as a capacitance to ground. The MicroClock family of clock generators are designed for Wearable applications where clock traces are always relatively short. Power consumption is extremely important in Wearable applications, and fortunately, the small size helps minimize the supply current.

Clock Amplitude: One of the programmable features of the MicroClock device is to optimize for power is the programmable clock amplitude. The bigger the clock amplitude, the bigger the supply current consumption of the clock driver. A standard LVCMOS driver will swing rail-to-rail. With V_{DD} = 1.8V, this means 1.8Vpp clock amplitude. OUT2 and OUT3 on the device can be reduced to 1.2V, 1.1V or 1.0V. Of course, the target clock input needs to be able to deal with the smaller amplitude.

- **Overdriving a crystal oscillator pin**: Most crystal oscillator pins work best when overdriven with a smaller amplitude, so this is a win-win situation where the lower amplitude lowers the device's power consumption while it also works better for the crystal oscillator input. The recommendation is to set 1.0V amplitude and AC couple the output to the crystal oscillator input pin.

Figure 2. Driving a Crystal Oscillator Input Pin



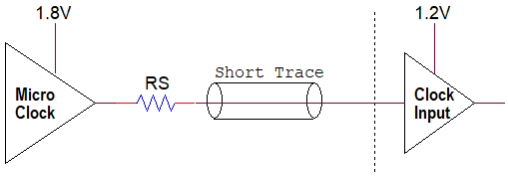
Keep the trace from the device output to crystal oscillator input pin as short as possible to minimize trace parasitic capacitance. When the trace is shorter than about 1 inch or 2.5cm, there is no need to design the trace as a transmission line and RS will not be needed. When designing the clock trace as a 50Ω transmission line, the proper value for RS is 22Ω to match the device output to the trace impedance.

Most crystal oscillators have resistor RF integrated but when RF is not integrated, add RF = 100kΩ between the XIN and XOUT pins.

Also consider the DC bias settling time when selecting a value for CS. When CS = 10nF and RF = 1MΩ, the DC bias settling time is about 1nF × 1MΩ = 10ms. In case the crystal oscillator is 32.768kHz and overdriven with a 32.768kHz clock from the MicroClock device, the value for RF can be very high, possibly > 10MΩ. For 32.768kHz, it is recommended to use CS = 100pF.

- **Driving a clock input of lower voltage logic**: This is also win-win. Select the amplitude that is closest to what the clock input logic needs. This is valid for both high frequencies and low frequencies, like 32.768kHz.

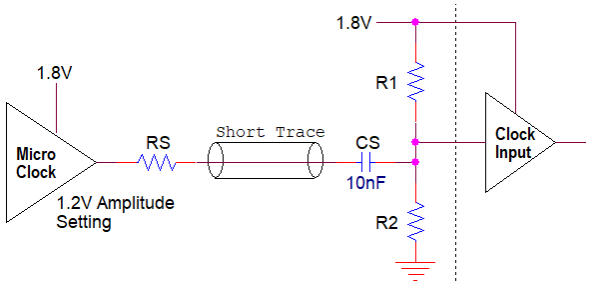
Figure 3. Driving a CMOS Input Pin with Lower V_{DD}



The same recommendations are applicable for the trace length and the value of RS.

- **Driving a 1.8V clock input with a lower amplitude**: It is possible to drive a 1.8V input with 1.2V amplitude when AC coupling and re-biasing the clock input to 0.9V. The swing at the clock input will now be 17% to 83%. Most CMOS inputs can handle signal swings down to 30% to 70%, so there is still enough margin.

Figure 4. Driving CMOS Input of Same V_{DD} but with Low Amplitude



Use R1 = R2 to re-center the clock waveform at 50% of V_{DD} = 1.8V. A good value for R1 = R2 is 100kΩ for 1MHz and higher clock frequencies. It is not recommended to use this method for 32.768kHz. The additional DC bias in R1 and R2 will be more than the supply current savings at the device output driver. For 32.768kHz, it is recommended to use the circuit in Figure 3 and set the amplitude to what the clock input requires.

The same recommendations are applicable for the trace length and the value of RS as mentioned above. The effort of setting a lower amplitude and adding components to re-bias the clock input may only be worth it in the case where a relatively long trace is needed, so the power savings are significant.

VCO Frequency: The power consumption of the VCO in the PLL depends upon the frequency of the VCO. Timing Commander™ software can estimate the power consumption of a certain configuration and will be helpful with optimizing the MicroClock device configuration for saving power. The general rule is, the lower the VCO frequency, the lower the power consumption. But there is also the rule of, the higher the VCO frequency, the better the jitter performance. In case there are jitter requirements, a compromise needs to be found between jitter performance and power consumption.

Output Loading:

- **Capacitive Loading**: Output clock traces have parasitic capacitance and the target clock input will have an input capacitance as well. Minimize the output clock trace length for the lowest power. The supply current used to drive an output capacitance is IDRIVER = C × F × V. “C” is the total capacitance seen by the clock output driver, “F” is the clock frequency and “V” is the peak-to-peak amplitude of the clock signal.
  - **Example 1**: 20mm clock trace with 2pF parasitic capacitance and 3pF clock input capacitance. The clock frequency is 10MHz and the clock amplitude is 1.2V. This results in IDRIVER = 5E - 12 × 10E + 6 × 1.2 = 0.06mA.
  - **Example 2**: 100mm clock trace with 10pF parasitic capacitance and 3pF clock input capacitance. The clock frequency is 50MHz and the clock amplitude is 1.8V. This results in IDRIVER = 13E - 12 × 50E + 6 × 1.8 = 1.2mA.

  Example 1 uses a short clock trace, a low clock frequency and reduced output amplitude setting to minimize the supply current consumption of the output driver. With example 2, all three parameters are made worse and the result is a much higher supply current in the output driver.

  Note that when driving a crystal oscillator input pin, the pin capacitance can be quite large when the crystal load capacitance is on the chip (e.g. 10pF–20pF). When external capacitors are used from the crystal pins to ground, do not assemble these capacitors when overdriving the crystal oscillator input pin with a MicroClock device output.

- **Driving a 50Ω Clock Trace**: The math is different but the results are not very different from using the trace capacitance. The theory is that every time the clock makes a transition from low to high, the output driver needs to drive 100Ω from 1.8V, which is 18mA. The 100Ω is from the driver output impedance in series with the clock trace impedance, both 50Ω. The 18mA needs to be driven for as long as it takes for the pulse to travel to the end of the clock trace and for the reflection to travel back to the driver. As soon as the reflection arrives back at the driver, the drive current drops back to zero.
  - **Example**: 100mm clock trace with 50Ω impedance and 50MHz clock frequency. It takes about 1.14ns for a pulse to travel up and down that trace. The period length of 50MHz is 20ns so the average supply current in the clock driver is 18mA × 1.14 / 20 = 1.03mA.

  The formula for the average clock driver supply current is as follows: IDRIVER = 2t × F × V_{DD} / (2Z).

  “Z” is the clock trace impedance, “F” is the clock frequency and “t” is the time it takes for a pulse to travel from the driver to the end of the clock trace. The clock pulse velocity with a micro-strip trace on FR4 will be about 1.75E + 8 meter/second. This value was used in the example above.

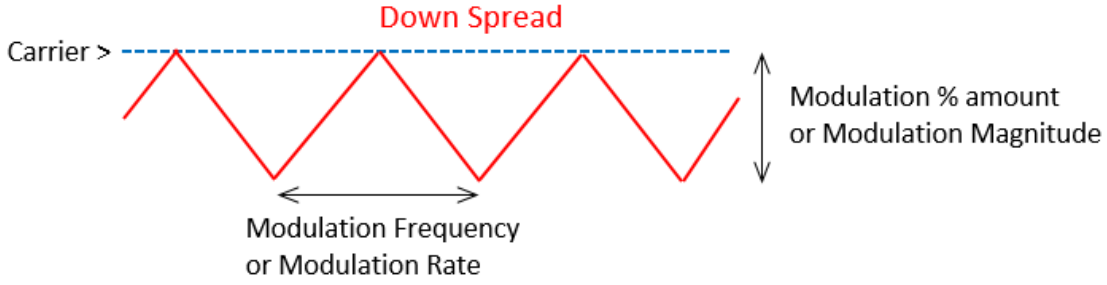
  The clock driver supply current of this example is a little bit lower than with example 2 at capacitive loading. The reason is the missing 3pF input capacitance of the target input. When adding its C × F × V = 0.27mA, we are very close to the example 2 result.

Using Spread Spectrum with the 5L1503S or 5X1503S

Spread spectrum modulation can be used to reduce electromagnetic interference (EMI). When applying spread spectrum modulation to a system clock, not only the EMI from the clock itself is reduced but also the EMI from all signals derived from that clock is reduced. This makes spread spectrum a very powerful tool for reducing the EMI of a system. Spread spectrum can be used to reduce cost for a system, replacing expensive shielding with a spreading clock.

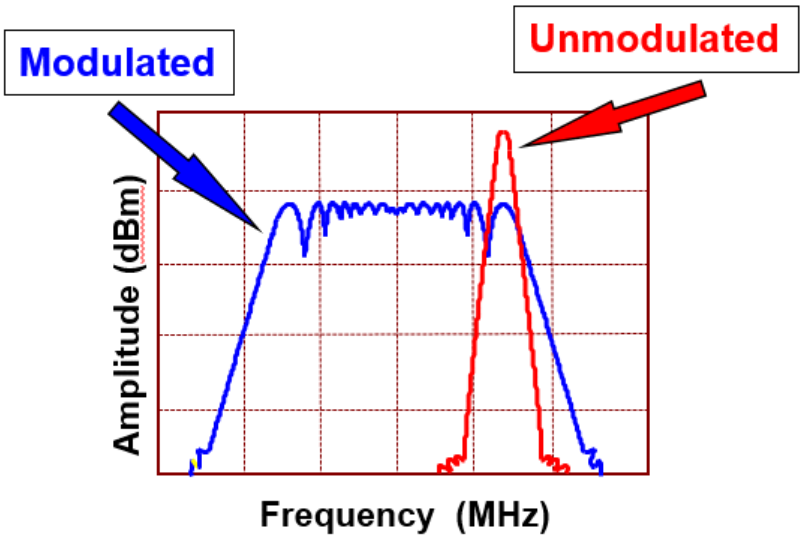
A clock signal is essentially a square wave. A square wave consists of a number of harmonics in the frequency spectrum. Theoretically, the perfect square wave only has odd harmonics (3rd, 5th, 7th, etc.), but when the duty cycle is not a perfect 50%, even harmonics will also be present (2nd, 4th, 6th, etc.). The power in the clock signal is concentrated in narrow harmonics that peak up to certain levels. Spread spectrum modulation spreads out the power in the harmonics so they don't peak up as high.

Figure 5. Spread Spectrum Modulation Waves



Spread spectrum modulation is frequency modulation. The frequency of the clock is moved up and down with a triangular modulation wave. The amount of clock frequency movement is called the magnitude or spread percentage. The frequency of the triangular modulation wave is called the modulation rate. Common modulation rates are between 30kHz and 33kHz. MicroClock ICs use down spread where the frequency is only moving below the carrier frequency. This is to avoid passing over a system maximum clock when applying the modulation.

Figure 6. Frequency Spectrum of One Harmonic of a Clock Wave



When the clock is not modulated, the frequency spectrum consists of harmonics that are narrow, like the red curve in Figure 6. Adding spread spectrum modulation, widens the peak at every harmonic, like the blue curve in Figure 6. Because each peak has a specific power level, making the peak wider also makes it less high. Adding spread spectrum to a clock lowers the ability of the clock to cause EMI.

The amount of EMI reduction is frequency dependent and the EMI reduction is bigger for the higher harmonics of the clock.

A quick formula for the EMI reduction is as follows: R(dB) = 10 × LOG(SS × FH/100kHz).

“R(dB)” is the EMI reduction in dB, “SS” is the peak-to-peak magnitude of the spread spectrum and “FH” is the frequency of the clock harmonic. 100kHz is the bandwidth that EMI test equipment uses.

Example: 100MHz clock with -0.5% of spread spectrum.

- 5th harmonic (500MHz): R(dB) = 10 LOG(0.005 × 500/0.1) = 14dB EMI reduction.
- 10th harmonic (1GHz): R(dB) = 10 LOG(0.005 × 1000/0.1) = 17dB EMI reduction.

Revision History

Revision Date	Description of Change
July 12, 2019	Initial release.

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