INTRODUCTION

Double-Density is IDT’s FCT-T family of 16, 18, and 20 bit bus interface components. The family is functionally compatible with the other 16 bit families, but offers users power savings, higher speeds, and excellent guaranteed low noise operation with a choice of output drive characteristics. The components are available in a 64ma drive version for use in backplane driving where line termination exists, a balanced drive 24ma version with internal series line termination for quiet operation, and a 3.3V version for use in applications requiring the lower supply voltage.

Although IDT’s Double-Density family is more forgiving than the older eight bit families, the decoupling must be properly executed to achieve optimum results. The three versions of the Double-Density components (64ma, 24ma, and 3.3V) have similar switching speeds and therefore have similar decoupling needs despite having different device parameters and output specifications. Because of this, the techniques for decoupling which are addressed herein apply uniformly across all versions of the Double-Density family.

When setting goals for decoupling a circuit, a designer should focus his attention on reducing the radiated emissions to meet the FCC limitations for the geographical area in which his circuit will be used. When this has been accomplished, the low noise levels needed to prevent cross talk and false switching will probably have been achieved. If the circuit contains low-level analog signals, additional decoupling will probably be necessary.

SELECTING THE CAPACITOR PACKAGE

The effectiveness of decoupling capacitors is often degraded by the series resistance and inductance inherent in the capacitor. The use of chip capacitors reduces the inductance due to the capacitor leads and through hole placement, making chip capacitors the optimum choice where that package style can be used. If the use of chip capacitors is not possible, the package should allow the capacitor to fit close to the board with very short lead lengths. With through hole capacitors the excess lead should be trimmed as close to the board surface as possible.

PC BOARD POWER AND GROUND PLANE

IDT’s Double-Density devices are packaged in a 48- or 56-pin SSOP, TSSOP, or TVSOP, with multiple power and ground pins as shown in Figure 1. Unlike older logic families with corner Vcc and ground pins, Double-Density packages have eight ground pins and 4 Vcc pins which are equally spaced on both sides of the package. By providing multiple, short, parallel paths for current, the lead inductance is lowered, reducing the effects of simultaneous switching noise. This also reduces the effects of inductance in the board metalization by decentralizing the current path.

When laying out a circuit board for use with Double-Density, the designer should use full ground and power planes with all ground and power pins on all devices connected to the proper plane. No power or ground pins on any Double-Density device should be left floating. The board should have a large capacitor near the power entry point on the board to stabilize any power surges from the power distribution system. If the board has an effective power distribution system, decoupling Double-Density should be easier than decoupling corner Vcc and ground packages.

Capacitors have a circle of influence around them meaning that pins and components that are in the immediate proximity of the capacitor will be effectively decoupled while those components that are further away will be less affected. This characteristic is modeled in Figure 2.

While the number of capacitors per component will vary depending upon the decoupling needs of the circuit and the cost sensitivity of the design, it is suggested that the designer use at least one ceramic capacitor per IC on the board. In cost sensitive applications it may be possible to reduce the overall number of capacitors to less than one per component. In noise
敏感电路（例如 A/D 应用程序）可能需要不止一种电容类型。 tantalum 电容在高频模拟情况中工作良好，已经包括陶瓷电容。

如果电路板只有一面有组件，电容可以放在设备的两端（考虑电源的方向），并确保有稳固的连接到电源和接地平面，如图 4 所示。这将为板设计者提供直接访问到包装的两侧，以避免布线干扰。

如果使用多个电容，电容可以放在设备的两端，或者如果这会导致布线冲突，则电容可以位于包装的相邻角落，如图 5 所示。

电容相对于电源的放置
电容应放置在电路板和被去耦组件之间。由于所有电荷的最终来源是电源入口，因此将电容置于组件和入口点之间可以确保电容在到达组件之前接收和稳定电压。如果电容和组件位置颠倒，电荷将直接从入口点流向组件，而不是通过电容。这将使噪声更容易到达组件，并使噪声产生的噪声传播到电路板上。

图 3. 电容放置在双组件侧的电路板上

图 4. 电容放置在单组件侧的电路板上

图 5. 双电容放置在双侧组件侧

图 2. 所有电容都有一个“影响范围”

电容相对于组件的放置
电容应尽可能靠近被去耦的组件。没有必要为每个 Vcc 提供单独的电容，但是电容应牢固地连接到电源和接地平面，为所有电容和接地引脚提供一个短的导电路径。相对于组件，最佳放置位置是在电路板的反面，中心位置，如图 3 所示。

电源和接地引脚在 SSOP 包装中，靠近设备输出将产生比靠近设备输入或使能引脚更频繁的噪声。由于这些引脚通常靠近包装的中心，因此将电容放置在电路板的反面，中心位置，可以提供从电容到引脚的最短路径，从而获得最佳去耦。

图 2. 所有电容都有一个“影响范围”

图 3. 电容放置在双侧组件的电路板上

图 4. 电容放置在单侧组件的电路板上

图 5. 双电容放置在组件侧的电路板上

电源相对于电源入口的放置
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A model can be considered as a single capacitive element with no inductance or resistance. As the noise frequency increases to levels above 50MHz the influence of the inductance and resistance increases to the point that the inductance becomes the dominating component of the capacitor's impedance. If noise issues are critical, the designer may be required to use two capacitors to cover both the high and low frequency components of the spectrum.

Capacitors that are operating near their characteristic frequency will resonate at that frequency and provide good noise filtration with no inductive kick. Using this characteristic, designers frequently use a 0.01uf or a 0.001uf capacitor to filter out high frequency noise. The characteristic frequency of the capacitor can be obtained by contacting the capacitor manufacturer. Typically ceramic capacitors have a characteristic frequency in the 20-40MHz range. Tantalum capacitors typically work best at frequencies above 80MHz and have decreasing effectiveness at lower frequencies.

While picking capacitors at the resonant frequency of the circuit will prove beneficial to noise suppression, the selection of smaller valued capacitors will not. The value of the capacitor should always be at the resonant frequency or have a larger capacitance value. If small valued capacitors are used, it will be necessary to have good low frequency decoupling through additional larger valued capacitors located near the component.

**FREQUENCY CONSIDERATIONS**

IDT's Double-Density components have very high internal switching speeds, but the lead inductance, packaging, and board placement will absorb most of the high frequency components above 120MHz before the noise can enter the power distribution system or radiate. The frequencies most likely to cause problems by reaching the power distribution system are in the 60-80MHz range (40-120MHz on a broader scale) and therefore the decoupling effort should be focused on this range.

Capacitors can be modeled as a capacitor in series with an inductor and a resistor as shown in Figure 7. With typical ceramic capacitors at low noise frequencies (<10MHz), the model can be considered as a single capacitive element with no inductance or resistance. As the noise frequency increases to levels above 50MHz the influence of the inductance and resistance increases to the point that the inductance becomes the dominating component of the capacitor's impedance. If noise issues are critical, the designer may be required to use two capacitors to cover both the high and low frequency components of the spectrum.

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**USING CAPACITORS WITH DIFFERING INTERNAL STRUCTURES**

When using capacitors of different values and different types on the same board in close proximity to one another, it is possible for the two capacitors to begin interacting with one another. With different frequency responses, the two capacitors will respond with different timings to voltage spikes with the result being an instantaneous difference in the internal voltages between the two capacitors. The two capacitors can then begin oscillating by passing charge between themselves through their characteristic series inductors as modeled in Figure 8. The end result will be a reduction in the effective decoupling that takes place and the possible addition of a noise source on the board.
Additionally, two capacitors with highly different dielectric constants in close proximity on the same board may affect each other because the high dielectric constant part will dampen the high frequency resonance of the low dielectric constant capacitor and the end result will be reduced noise suppression.

To effectively handle the problem of capacitors with differing internal structures, be sure the two types are not placed in close proximity to one another as shown in Figure 9. This can be done by placing the different capacitors at opposite ends of the device or equally spaced on the back side of the board. If these choices are not feasible, the capacitors can be spaced in opposing corners of the device. The key to placement is to avoid having the Vcc pins of two capacitors adjacent or having the Gnd pins of two capacitors adjacent.

Figure 9. Exercise care when positioning two capacitors with differing frequency response in close proximity to one another.

CONCLUSIONS

To properly decouple IDT's Double-Density parts do the following:

1) Select a capacitor that will meet the needs of the component. A 0.1uf ceramic is a good starting point. A 0.01uf ceramic may be better in situations which have good low frequency decoupling elsewhere on the board but are experiencing high frequency noise.

2) For best results use at least one capacitor per IC. More may be necessary in noisy situations, fewer may be possible with careful component and capacitor placement.

3) Place the capacitor as close to the component as possible. On the reverse side of the board is best. At either end of the component is also good.

4) Make sure that there is a good connection between all ground pins on the component and the capacitor. This should be in the form of a solid ground plane under the device. The same is true for the Vcc pins.

5) Place the capacitor between the component and the power entry point on the board if possible.

6) In critical situations two or more capacitors of different values may be used. In this case select a larger capacitor to provide low frequency stability and a smaller capacitor to give a series resonance to higher frequencies. Examples may be a 0.1uf or a 1uf ceramic along with a 0.001uf or a 0.01uf.

7) If capacitors of different internal structures are used, they should not be placed in close proximity to one another. Capacitors of different types that are close to one another may resonate between themselves and negate any positive effect of using two capacitors.