Interfacing the RC32438 with DDR SDRAM Memory

Application Note AN-371

Notes

By Kasi Chopperla and Harold Gomard

Revision History

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October 29, 2003: Added Passive DDR Termination Scheme for Lightly Loaded Systems section.

Introduction

The RC32438 is a high performance, general-purpose, integrated processor that incorporates a 32-bit CPU core with a number of peripherals including:

- *A memory controller supporting DDR SDRAM*
- *A separate memory/peripheral controller interfacing to EPROM, flash and I/O peripherals*
- *Two Ethernet MACs*
- *32-bit v.2.2 compatible PCI interface*
- *Other generic modules, such as two serial ports, I^2C, SPI, interrupt controller, GPIO, and DMA.*

Internally, the RC32438 features a dual bus system. The CPU bus interfaces directly to the memory controller over a 32-bit bus running at CPU pipeline speed. Since it is not possible to run an external bus at the speed of the CPU, the only way to provide data fast enough to keep the CPU from starving is to use either a wider DRAM or a double data rate DRAM.

As the memory technology used on PC motherboards transitions from SDRAM to DDR, the steep ramp-up in the volume of DDR memory being shipped is driving pricing to the point where DDR-based memory subsystems are primed to drop below those of traditional SDRAM modules. Anticipating this, IDT opted to incorporate a double data rate DRAM interface on its RC32438 integrated processor.

DDR memory requires a VDD/2 reference voltage and combination series and parallel terminations that SDRAM does not have. The board layout requirements for DDR are substantially more rigorous.

The purpose of this application note is to help designers select the proper components and design effective layouts to minimize the difficulty of using DDR memory. This application note will outline some of the key considerations a designer should be aware of when designing embedded applications that use this technology. It is assumed that the reader is already familiar with the basic concepts of DDR technology.

Interfacing with DDR Memory

The key features of the RC32438 DDR memory controller include:

- *Support for up to 2GB of DDR SDRAM*
- *Support for devices with densities of 64Mb, 128Mb, 256Mb, 512Mb, and 1Gb*
- *16-bit and 32-bit data bus width options to allow interfacing to 8, 16, or 32 bit external memory devices*
- *Data bus multiplexing support to allow interfacing to standard x64 DDR DIMM and SODIMM form factors*
- *Creation of differential clocking signals for external memory subsystem*
- *Automatic refresh generation.*

Notes

DDR Loading

In order to support maximum speeds, reasonable DDR loading constraints must be followed. In particular, IDT recommends that for 266MHz operation no more than four discrete DDR chips be connected to the data bus and that no more than two discrete DDR chips be connected to each pair of clocks. It is not recommended to use a SODIMM or DIMM at this frequency.

For 200MHz operation, it is recommended that no more than four discrete DDR chips be connected. SODIMMs or DIMMs are not recommended, even at this slower speed. However, if SODIMMs or DIMMs are used, they should contain a maximum of 8 chips and the design should include quickswitches and a clock driver. An additional clock driver is needed because eight chips require at least four pairs of clocks to meet the maximum load requirement of two chips per clock while the RC32438 supplies only 2 pairs of clocks.

x64 Memory Configurations

The standard DDR DIMMs that are available in the market come in 64-bit widths. It is possible to tie together some of the control and data signals on a 64-bit DIMM module to form two banks of 32-bit DDR DRAM. Historically, most x32 memory controllers have accomplished this by using the data mask (DQM) signals to select the desired bank of data lines. However, since DDR memory does not drive the data mask signals (DMs on DDRs) during read cycles, this approach is not possible for DDR-based DIMMs.

To support data bus multiplexing, external bus switches must be placed between the RC32438 and external DDR memory banks. These bus switches are used to isolate unused data bits and strobes from the RC32438, allowing 16-bit or 32-bit data quantities to be read from a 64-bit bus. The RC32438 DDROEN[3:0] pins are output enables for these buffers.

Since nearly all embedded designs use directly soldered DRAMs, rather than DIMMs, this is only a consideration for a very small subset of designs. However, in the event the designer wishes or needs to implement a x64 DDR data path, Figures 1 and 2 below provide examples of how this multiplexing may be accomplished for 64-bit wide DIMMs with the RC32438 processor in DDR x32 mode and in DDR x16 mode.

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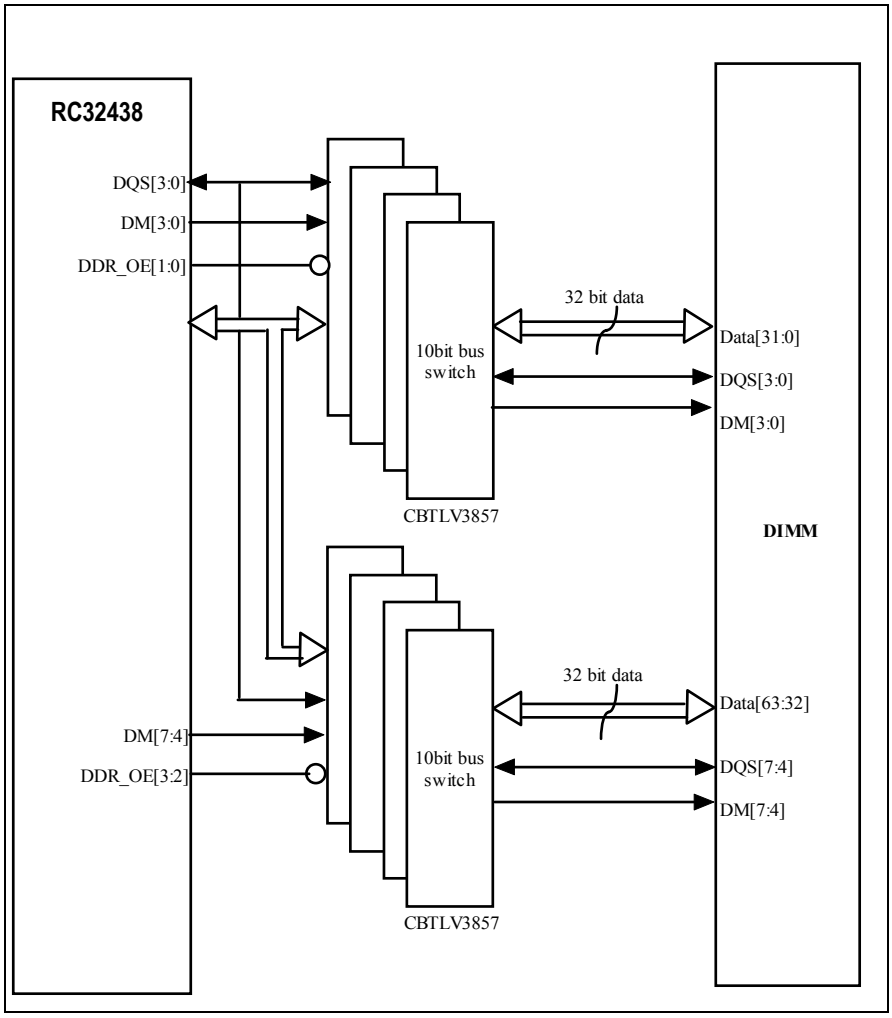

Figure 1 Data Bus Muxing for 64-bit DIMMs with RC32438 in DDR x32 Mode

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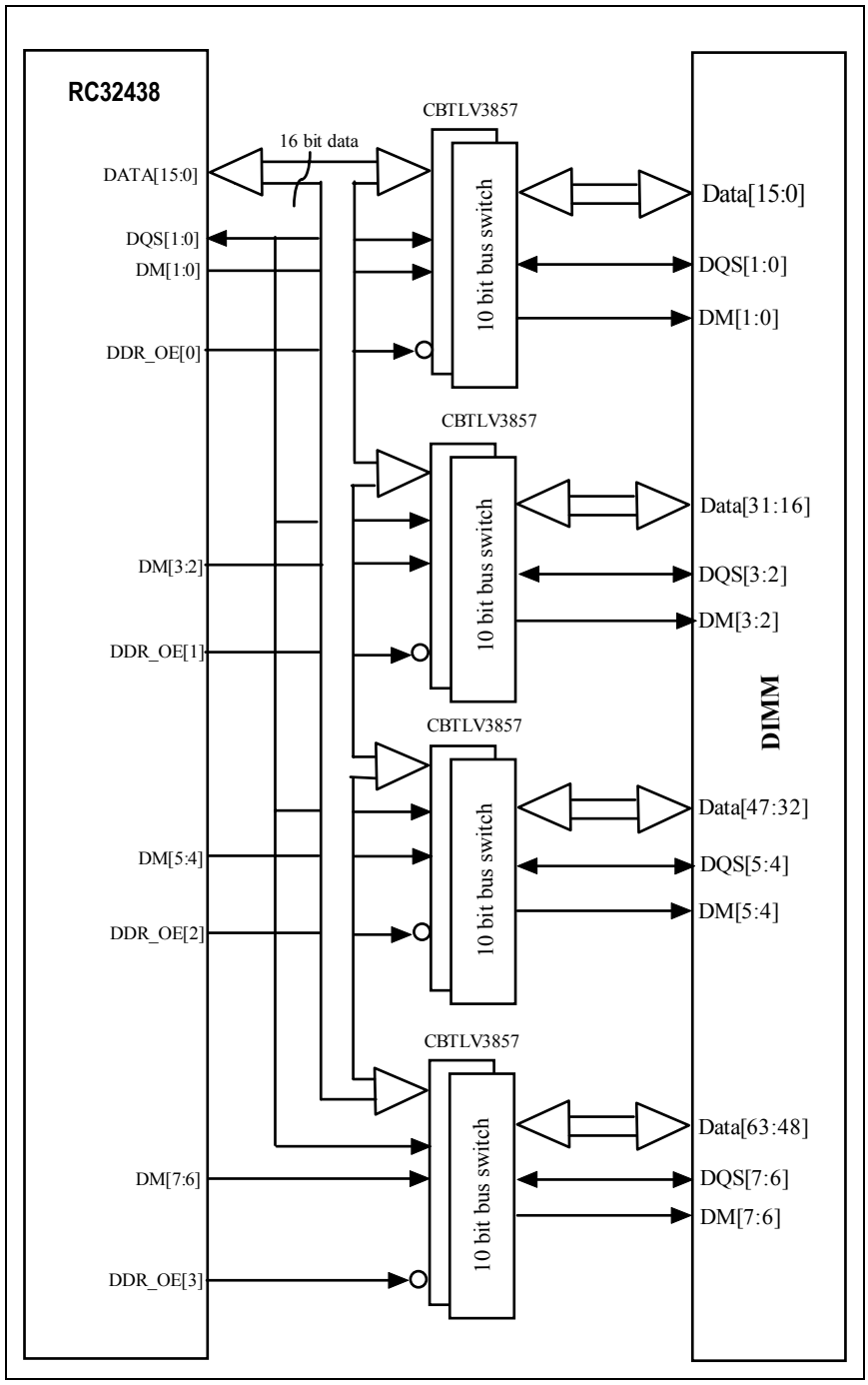

Figure 2 Data Bus Muxing for 64-bit DIMMs with RC32438 in DDR x16 Mode

Critical Design Considerations

There are three major issues to consider when designing DDR-based subsystems:

- *Resistive signal termination schemes*
- *PCB signal routing requirements*
- *Generation and supply of required reference voltages.*

All three issues are critical to producing a reliable DDR-based memory subsystem, so designers must carefully address each.

Notes

Resistor Terminations

There are several SSTL-2 approved termination methods that can be used with DDR. The choice is very much design-dependent. Generally, single-series/single-parallel terminations work well with uni-directional signals, such as address lines. For bi-directional signals, double-series/double-parallel terminations usually produce slightly better results. However, it should be noted that since the double-series and/or double-parallel termination schemes require resistors or resistor packs on both ends of the signal, they invariably result in increased component counts, which slightly increases board cost.

Therefore, for most applications, IDT recommends that a single-series single-parallel termination scheme be used for both data and command signals. For clock signals, a pull-up resistor is not recommended. A single-series resistor between 10 and 33 ohms (associated with a common mode resistor[1] to eliminate any noise due to the differential pair between 100 and 150 ohms) will provide the best results. Three different termination schemes are displayed in Figure 3.

These schemes have several benefits:

- *Reduced cost*
- *Simpler signal routing*
- *Reduced reflections*
- *Better signal bandwidth and settling.*

The range for the series resistor is between 10 and 33 ohms and the range for the parallel pull-up is between 25 and 56 ohms.[2]

The SSTL-2 Class II specification recommends a series resistor of 25 ohms and dual-parallel terminations of 50 ohms. Resistor packs specifically designed to meet this requirement are widely available. While other termination schemes will often produce superior noise margin, this configuration is usually adequate. However, it should be noted that IDT's DDR drivers are slightly below the strength defined for Class II drives. As a result, the total amplitude of the signal swing will be slightly reduced because the driver has to counter the 25 ohm parallel termination with less than the drive strength specified by Class II. Although this will not cause a problem for most designs, IDT strongly recommends that designers wishing to lock themselves into this type of configuration through commercially available resistor packs first simulate the design using a signal integrity software package.

In general, regardless of which termination scheme is chosen, it is highly recommended that the board designer run signal integrity simulations. This allows the designer to determine the optimal resistor values for the specific board routing and memory configuration in question, resulting in a design with superior noise margins. Because the noise margins for SSTL-2 based drivers are very tight, any extra margin that can be eked out through tweaking the terminations is well worth pursuing.

1. The common mode resistor should be used only on chip-based designs since the DIMMS/SODIMMS usually implement it directly on the module. It should be noted that DIMMS/SODIMMS also implement series termination for bi-directional signals (Data/Data-strobe) directly on the module, thereby eliminating any design dilemma.

2. When using double-parallel termination schemes, the values for the double-parallel pull-ups need to be doubled, since putting pull-ups in parallel effectively halves the pull-up value.

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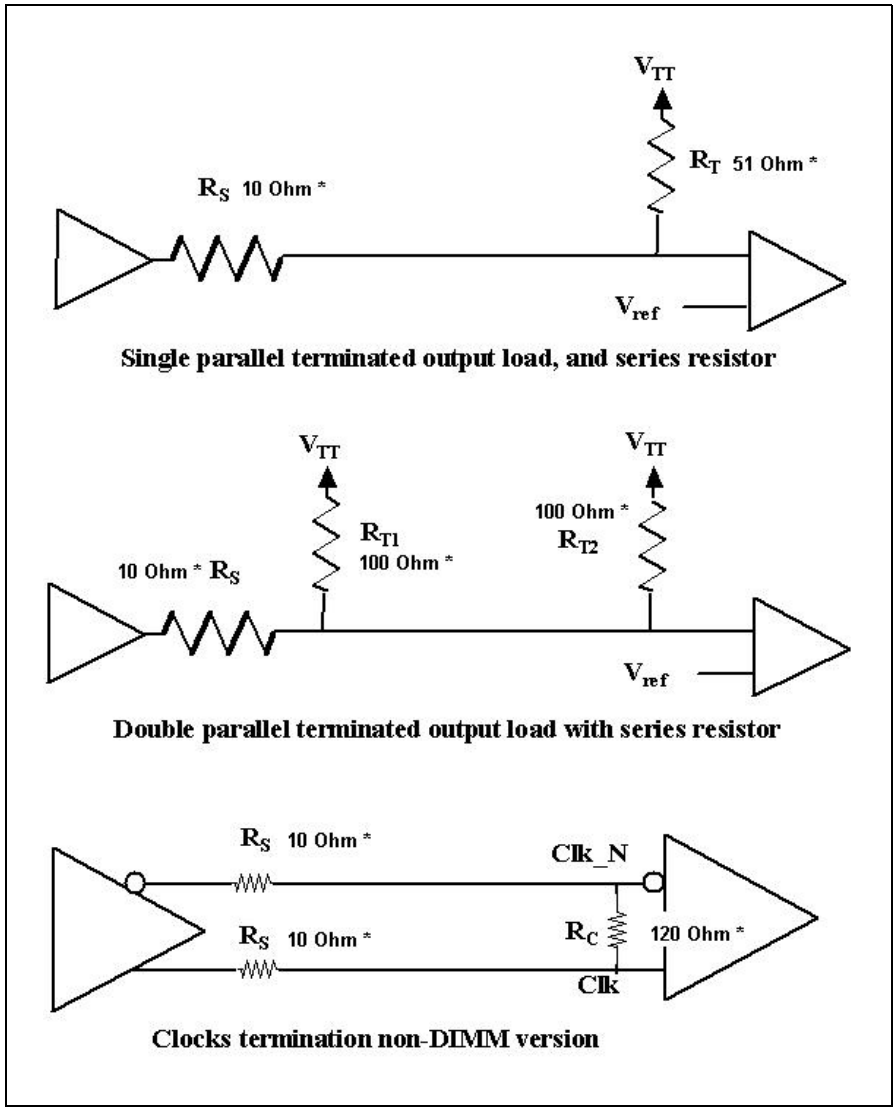

Figure 3 Termination Circuit Examples

***** Termination value recommended by IDT

PCB Routing

Proper routing of all DDR signals is absolutely essential. If proper attention is not paid to this requirement, the DDR memory subsystem is unlikely to operate at the maximum supported DDR memory subsystem frequency.

In an effort to guarantee that all designs featuring the RC32438 are able to operate at the highest possible frequencies, IDT strongly urges that the following layout guidelines be rigorously enforced:

DDR Clock Guidelines

- *Trace width: 10 mils.*
- *Trace space: 5 mils.*
- *Trace space to other signal group: 30 mils.*
- *Clock signals should be routed as a differential pair in a point to point topology.*
- *Match exactly the DDRCKP[0] and DDRCKN[0] trace lengths (a trace length of ± 20 mils is acceptable). Do the same for DDRCKP[1] and DDRCKN[1]. This trace matching is necessary to meet the*

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*DDR SDRAM's input clock crossing voltage (Vix = 0.5*VDD ± 0.2 V). Match the loads between DDRCKP[0] and DDRCKN[0]. Do the same for DDRCKP[1] and DDRCKN[1].*

- *Match the trace lengths and loads between the two sets of DDR output clocks (i.e., the trace length and load of DDRCKP[0] should be equal to the trace length and load of DDRCKP[1]). If this is not possible, the system designer must do a careful board timing analysis to ensure that all DDR timing parameters are met for both sets of DDR clocks. For example, if DDRCKP[1] has a higher load and/or longer trace length than DDRCKP[0], the designer must ensure that DDR input hold times (i.e., tIH in the Jedec DDR Specification) are met with respect to DDRCKP[1], while input setup times (i.e., tIS in the Jedec DDR Specification) must be met with respect to DDRCKP[0]. As long as the DDRCKP[0] and DDRCKP[1] loads are identical, a trace length mismatch up to ± 100 mils is acceptable.*
- *It is recommended that each DDR clock output pin be loaded by no more than four DDR input pins. Board designers must do careful simulations using IBIS models of the RC32438 drivers and DDR SDRAM receivers, as well as accurate models of the board traces and terminations, to ensure smooth clock waveforms at the DDR pins.*

DDR Address, Chip-Select, and Command Guidelines

- *Trace width: 5 mils.*
- *Trace space: 15 mils.*
- *Trace space to other signal group: 20 mils.*
- *These signals should be routed in a Daisy Chain topology.*
- *For systems with light loads (i.e., boards with one discrete DDR SDRAM chip), make the DDR address, chip-select, and command[1] traces longer than the DDR clock traces (up to 1 inch longer is acceptable). For these systems, the DDR clock loads approximate the address, chip-select, and command loads. Therefore, it is important to follow this recommendation in order to meet DDR input hold times.*
- *For systems with heavy loads (i.e., boards with a DDR SODIMM), make the DDR address, chip-select, and command traces about the same length as the DDR clock traces (the trace length mismatch is linear with the load mismatch). For these systems, the DDR clock loads are lower than the address, chip-select, and command loads, which helps meet the DDR input hold time margins. Following this recommendation should result in good DDR input setup and hold time margins. If the DDR address, chip-select, and command traces are longer than the DDR clock traces, the DDR input setup time margins will decrease.*

DDR Data, Data-Strobe, and Data-Mask Guidelines

- *Trace width: 5 mils.*
- *Trace space: 15 mils.*
- *Trace space to other signal group: 20 mils.*
- *These signals should be routed in a Daisy Chain topology and preferable be on the same layer with no vias.*
- *Match the DDRDQS[3:0] and DDRCKP[1:0] trace lengths. This will maximize the DDRDQSx to DDRCKPx setup and hold margins (i.e., tDSS and tDSH in the Jedec DDR Specification), as well as the 'write command to first DQS latching transition' margin (tDQSS in the Jedec DDR Specification). A trace length mismatch up to ± 200 mils is acceptable.*

1. Refers to the signals DDRADDR[13:0], DDRBA[1:0], DDRCSN[1:0], DDRRASN, DDRCASN, DDRWEN, and DDRCKE.

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- *Match the DDRDATA[31:0] and DDRDQS[3:0] trace lengths. In the single data strobe mode (SDS = 1)[1], the trace length of DDRDQS[0] must closely match the trace lengths of DDRDATA[31:0]. If not in single data strobe mode (SDS = 0), matching must be done between the following pairs (a trace length mismatch up to ± 50 mils is acceptable):*

  DDRDQS[0] ==> DDRDATA[7:0]

  DDRDQS[1] ==> DDRDATA[15:8]

  DDRDQS[2] ==> DDRDATA[23:16]

  DDRDQS[3] ==> DDRDATA[31:24]

- *DDRDQS[3:0] traces should be routed away from other signals to prevent crosstalk.*
- *For systems that do not use data bus multiplexing mode (DBM = 0)[1], match the DDRDM[3:0] traces with the DDRDATA[31:0] lines. Specifically, match the following pairs:*

  DDRDM[0] ==> DDRDATA[7:0]

  DDRDM[1] ==> DDRDATA[15:8]

  DDRDM[2] ==> DDRDATA[23:16]

  DDRDM[3] ==> DDRDATA[31:24]

- *For systems that use data bus multiplexing mode (DBM = 1), match the DDRDM[7:0] traces with the DDRDATA[31:0] lines. The following table shows which DDRDM bits correspond to which DDRDATA bits.*

DDRDM	DDRDATA
DDRDM[0, 4]	DDRDATA[7:0]
DDRDM[1, 5]	DDRDATA[15:8]
DDRDM[2, 6]	DDRDATA[23:16]
DDRDM[3, 7]	DDRDATA[31:24]

- *Board designers must do careful simulations using IBIS models to ensure the above is true[2]. Although an ideal configuration may not be achievable, the more the board layout deviates from the ideal, the less margin exists to meet DDRDM hold times with respect to DDRDQS (tDH in the Jedec DDR specification). Failure to meet the DDRDM hold times with respect to DDRDQS would require a decrease in the DDRCKP frequency in order to make the system operational.[3]*
- *Keep the read data access loop time (DDRCKP => DDRDATA) below one DDRCKP period. For example, if the DDRCKP period is 8ns, the board designer must ensure that the delay from DDRCKP (at the RC32438 pins) to DDRDATA (at the RC32438 pins) for a read transaction is below 8ns. This implies that the sum of the DDRCKP board flight time and the DDRDATA board flight time plus the DDR read data access time (tAC in the Jedec DDR Specification) has to be below one DDRCKP period.*

1. See SDS bit in the DDRC register.
2. These simulations should take into account IBIS models of the RC32438 drivers/receivers and DDR SDRAM drivers/receivers, as well as accurately model the effects of an FET bus switch in open state. Trace lengths and terminations must also be modeled accurately.
3. The RC32438's DDR Controller architecture is such that both setup and hold time margins with respect to DDRDQSx increase as the DDRCKP frequency decreases.

Notes

General PCB Considerations

- *Do not route DDR signals on any layer that is not directly adjacent to a common reference plane.*
- *If DIMM modules are being used, place series resistors close to the first DIMM. This simplifies routing and reduces controller congestion.*
- *Place termination resistors on a top layer VTT island which is at the end of the bus (VTT must be a power plane).*
- *Place the VTT generator as close as possible to the termination resistors.*

Termination and Reference Voltage Generation (VTT and Vref)

The I/O interface standard (SSTL_2) used on DDR memories uses a reference voltage to maintain the DDR signals near their switching level to increase switching speed. This is achieved by minimizing timing skew due to asymmetric logic highs versus logic lows, noise on Vref or VTT, offset of VTT relative to Vref or drift of Vref or VTT over temperature or noise.

This reference voltage (Vref) must meet several requirements in order for the DDR subsystem to operate reliably at the maximum supported DDR frequencies. The Vref requirements are:

– *Vref must track the midpoint of the signal voltage swing (generally VDDQ/2) within 3% over all valid voltage, temperature, and noise level conditions. See Figure 4 below.*

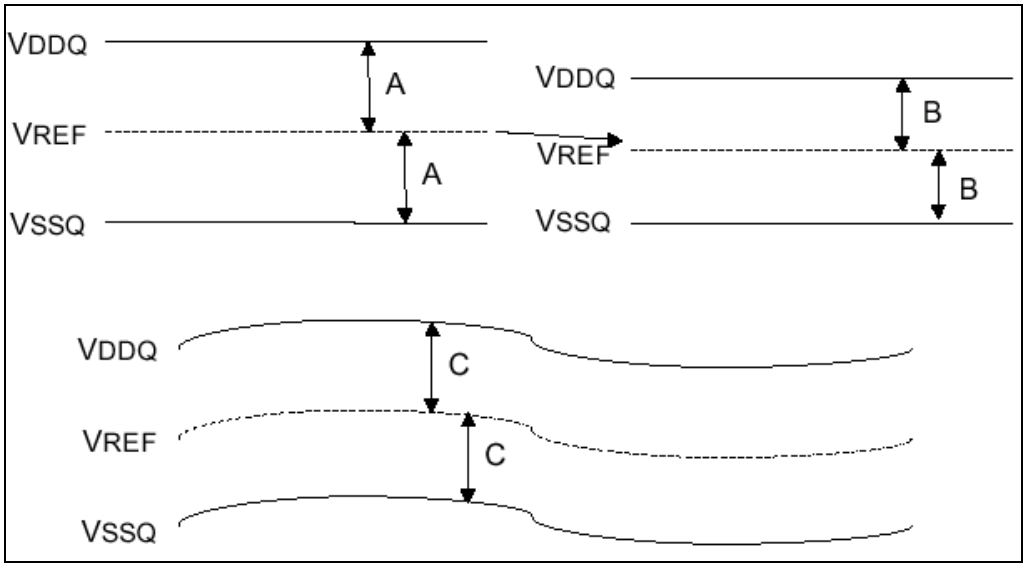

Figure 4 Vref tracking of VDD

– *Vref must use a distributed decoupling scheme to minimize capacitor ESL and localize the transient currents and returns.*

– *Vref must be isolated from other nets in order to comply with requirement #1.*

– *Vref must be decoupled from both VDD and VSS with balanced decoupling capacitors. (Again, this is necessary to meet requirement #1.)*

These requirements can be met in several ways. The easiest way is to use a component specifically designed for this purpose. One such solution is Fairchild Semiconductor's LP2995 switching regulator. It can source or sink up to 3A of current while regulating an output VTT voltage to within 3% or less. It also provides a Vref output which fits our design bill well. One can use a simple 1% resistor divider to get the required Vref voltage at low cost and with great accuracy.

One possible implementation scheme, which successfully validated on both our validation and evaluation platforms, is shown in Figure 5. However, there are many other solutions available from other vendors which may provide comparable or even superior performance.

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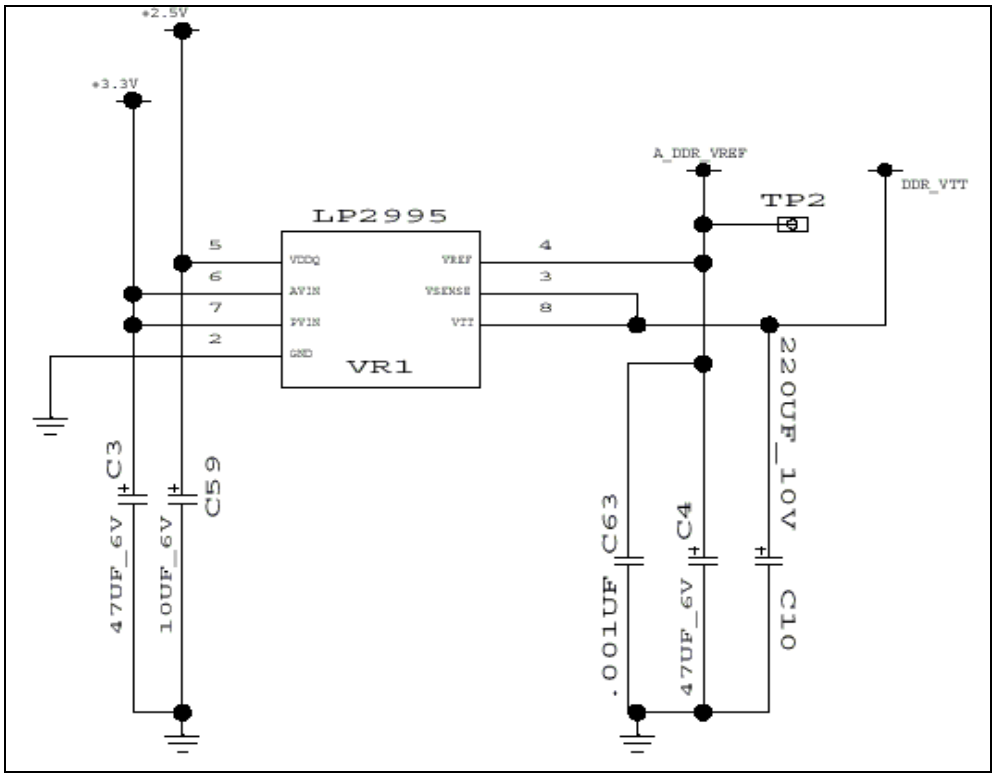

Figure 5 VREF and VTT Generation Scheme

Passive DDR Termination Scheme for Lightly Loaded Systems

In the case of very lightly loaded DDR-based systems, e.g., one or two DDR chips with the RC32438 device and short traces (less than 3.5 inches), it is possible to implement a passive DDR termination scheme. In the case of a passive termination scheme:

- All pull-up terminations to DDR_VTT are optional. As a result, the designer may remove the LP2995 voltage regulator, which generates DDR_VTT, and its associated circuitry from the design.
- However, VREF (Voltage reference at +1.25V) is still required by the RC32438 processor as well as all DDR chips. Because VREF is usually generated by the LP2995, if the LP2995 is removed, an alternate source must be implemented. A simple divider bridge using 20K resistors in parallel with 0.1uf caps between +2.5V and GND can be used (see Figure 6).
- VREF does not need to be a power plane, since a thick trace (30mils+) is sufficient. The divider bridge should be close to the DDR chip and the CPU.
- Series terminations are still required, however, and designers should follow the recommendations made earlier in this application note.
- Extra care should be taken regarding trace length matching, board layout, and noise prevention. Clocks, traces, and data strobes should be routed away from all other signals.

The removal of the DDR_VTT resistor packs and the voltage regulator circuitry results in a simpler board design/layout as well as some cost reduction.

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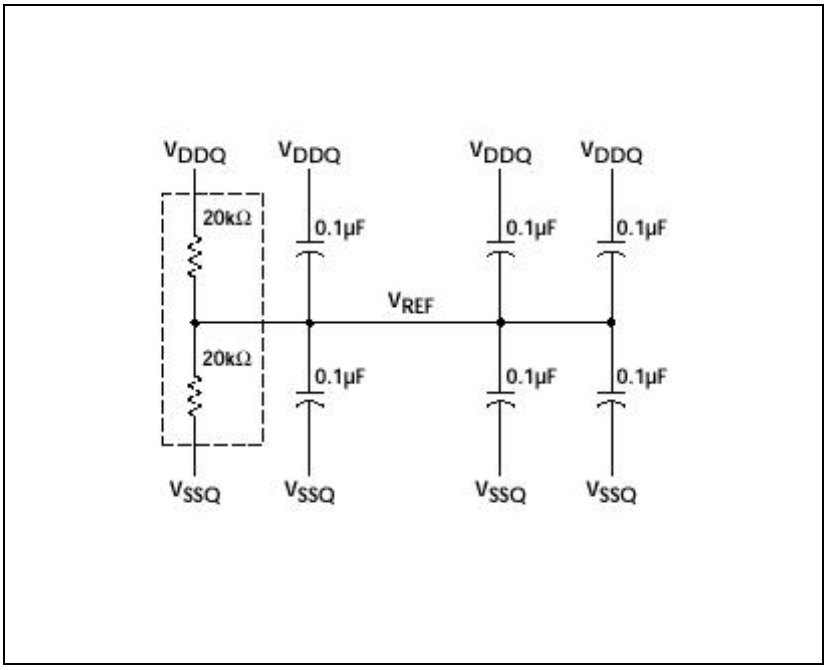

Figure 6 VREF Generation Scheme

Note: VDDQ = +2.5V

Conclusion

Successfully designing a DDR-based system is not difficult. There are adequate margins in the system to allow it to operate over all specified operating voltages, temperature ranges, and noise levels with some room to spare. However, deviations from the optimal layout, termination, or reference supply may radically reduce that margin. Hence, it is imperative that designers do their best to adhere to these guidelines. Extra care taken during the design and layout phase will result in reduced or eliminated iterations, superior system reliability, and better production yields for the finished product.