INTRODUCTION

The SuperJET system interface discussed in this document is based on IDT’s 8 channel SuperJET transceiver (82P2288). These interface options are also applicable to the quad (82P2284), dual (82P2282) and single (82P2281) transceiver products. The SuperJET family of devices provides a wide variety of different modes on the system interface so that it can easily and gluelessly work with microprocessors, FPGAs, Time Slot Interchange Devices, Mappers, and other devices.

The purpose of this application note is to go over many of the different modes which the system interface can be programmed and the effect it has on the I/O direction, transmit edges, sample edges, clocks and signal priority.

![Diagram of SuperJET Signal Names and Terminology]

Figure 1. SuperJET Signal Names and Terminology
1 SYSTEM INTERFACE PIN SUMMARY

1.1 IN NON-MULTIPLEXED MODE
Refer to Table 1 for the receive system interface pin and Table 2 for the transmit system interface pin.

Table 1: Receive System Interface Pin Names in Non-Multiplexed Mode

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSDn</td>
<td>Receive Side System Data</td>
</tr>
<tr>
<td>RSIGn</td>
<td>Receive Side System Signaling</td>
</tr>
<tr>
<td>RSFSn</td>
<td>Receive Side System Frame Pulse</td>
</tr>
<tr>
<td>RSCKn</td>
<td>Receive Side System Clock</td>
</tr>
</tbody>
</table>

Table 2: Transmit System Interface Pin Names in Non-Multiplexed Mode

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSDn</td>
<td>Transmit Side System Data</td>
</tr>
<tr>
<td>TSIGn</td>
<td>Transmit Side System Signaling</td>
</tr>
<tr>
<td>TSFSn</td>
<td>Transmit Side System Frame Pulse</td>
</tr>
<tr>
<td>TSCKn</td>
<td>Transmit Side System Clock</td>
</tr>
</tbody>
</table>

1.2 IN MULTIPLEXED MODE
Refer to Table 3 for the receive system interface pin and Table 4 for the transmit system interface pin.

Table 3: Receive System Interface Pin Names in Multiplexed Mode

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MRSD</td>
<td>Multiplexed Receive Side System Data</td>
</tr>
<tr>
<td>MRSIG</td>
<td>Multiplexed Receive Side System Signaling</td>
</tr>
<tr>
<td>MRSFS</td>
<td>Multiplexed Receive Side System Frame Pulse</td>
</tr>
<tr>
<td>MRSCCK</td>
<td>Multiplexed Receive Side System Clock</td>
</tr>
</tbody>
</table>

Table 4: Transmit System Interface Pin Names in Multiplexed Mode

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MTSD</td>
<td>Multiplexed Transmit Side System Data</td>
</tr>
<tr>
<td>MTSIG</td>
<td>Multiplexed Transmit Side System Signaling</td>
</tr>
<tr>
<td>MTFSFS</td>
<td>Multiplexed Transmit Side System Frame Pulse</td>
</tr>
<tr>
<td>MTSCCK</td>
<td>Multiplexed Transmit Side System Clock</td>
</tr>
</tbody>
</table>
2 BACKPLANE CLOCK MODE

The system interface can be set in Non-Multiplexed mode or Multiplexed mode.

In Non-Multiplexed mode, the system interface can work in Master mode (the system interface clock and frame pulse output from the device) or Slave mode (the system interface clock and frame pulse input to the device).

In Multiplexed mode, the system interface can only work in Slave mode.

Refer to Table 5 and Table 6 for the clock / data rate in different operation modes. The related registers configuration is listed in Table 7.

Table 5: System Interface Clock & Data Rate in E1 Mode

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>Clock Rate</th>
<th>Data Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Multiplexed</td>
<td>Single Clock</td>
<td>2.048 MHz</td>
</tr>
<tr>
<td>Slave</td>
<td>Single Clock</td>
<td>2.048 MHz</td>
</tr>
<tr>
<td></td>
<td>Double Clock</td>
<td>4.096 MHz</td>
</tr>
<tr>
<td>Multiplexed</td>
<td>Slave</td>
<td>Single Clock</td>
</tr>
<tr>
<td></td>
<td>Double Clock</td>
<td>16.384 MHz</td>
</tr>
</tbody>
</table>

Table 6: System Interface Clock & Data Rate in T1/J1 Mode

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>Clock Rate</th>
<th>Data Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Multiplexed</td>
<td>Master</td>
<td>T1 Mode T1 Rate</td>
</tr>
<tr>
<td>Slave</td>
<td>T1 Mode T1 Rate</td>
<td>Single Clock</td>
</tr>
<tr>
<td></td>
<td>T1 Mode E1 Rate</td>
<td>Single Clock</td>
</tr>
<tr>
<td></td>
<td>T1 Mode E1 Rate</td>
<td>Double Clock</td>
</tr>
<tr>
<td>Multiplexed</td>
<td>Slave</td>
<td>T1 Mode E1 Rate</td>
</tr>
<tr>
<td></td>
<td>Double Clock</td>
<td>16.384 MHz</td>
</tr>
</tbody>
</table>

Table 7: Related Registers Configuration

<table>
<thead>
<tr>
<th>Operation</th>
<th>Configuration Registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Multiplexed / Multiplexed mode selection</td>
<td>RMUX (b3, 10H)</td>
</tr>
<tr>
<td>Master / Slave mode selection</td>
<td>RMODE (b0, X47H)</td>
</tr>
<tr>
<td>Single / Double clock selection</td>
<td>CMS (b1, X46H)</td>
</tr>
<tr>
<td>T1 mode E1 rate mapping mode selection</td>
<td>MAP[1:0] (b2~1, X47H)</td>
</tr>
<tr>
<td>Frame pulse active level selection</td>
<td>FSINV (b4, X48H)</td>
</tr>
<tr>
<td></td>
<td>for Receive Path</td>
</tr>
<tr>
<td></td>
<td>RMUX (b0, 10H)</td>
</tr>
<tr>
<td></td>
<td>TMODE (b0, X43H)</td>
</tr>
<tr>
<td></td>
<td>CMS (b1, X48H)</td>
</tr>
</tbody>
</table>
3 T1 TO E1 / E1 TO T1 MAPPING IN T1 MODE E1 RATE

There are three mapping modes:
- G.802 mode;
- One Filler Every Four Channels mode;
- Continuous Channels mode.

In Receive side, T1/J1 format will map to E1 format. See Figure 2 to Figure 4.

In Transmit side, E1 format will map to T1/J1 format. See Figure 5 to Figure 7.
Figure 5. E1 To T1/J1 Format Mapping - G.802 Mode

Figure 6. E1 To T1/J1 Format Mapping - One Filler Every Four Channels Mode

Figure 7. E1 To T1/J1 Format Mapping - Continuous Channels Mode
4 OPERATION OF SINGLE CLOCK MODE

4.1 CLOCK/DATA SAMPLE/UPDATE

The FE bit selects the active edge of (M)RSCKn/(M)TSCKn to update/sample the pulse on (M)RSFSn/(M)TSFSn. The DE bit selects the active edge of (M)RSCKn/(M)TSCKn to update/sample the data on (M)RSDn/(M)TSDn and (M)RSIGN/(M)TSIGN.

Figure 8 shows how to set FE and DE in Receive System Interface Slave mode. In this mode, RSCKn/MRCK and RSFSn/MRFS input clock and frame pulse from external, and RSDn/MRSD output data. If the RSCKn/MRCK rising edge samples the RSFSn/MRFS at middle, then set FE to ‘1’. If the RSCKn/MRCK falling edge samples the RSFSn/MRFS at middle, then set FE to ‘0’. If set DE to ‘1’, the RSDn/MRSD will be updated after RSCKn/MRCK rising edge. If set DE to ‘0’, the RSDn/MRSD will be updated after RSCKn/MRCK falling edge.

Figure 8. Receive Clock Slave Mode (Single Clock)
Figure 9 shows how to set FE and DE in Receive System Interface Master mode. In this mode, RSCKn and RSFSn output clock and frame pulse, and RSDn output data. If set FE to '1', RSFSn will be updated after RSCKn rising edge. If set FE to '0', RSFSn will be updated after RSCKn falling edge. If set DE to '1', RSDn will be updated after RSCKn rising edge. If set DE to '0', RSDn will be updated after RSCKn falling edge.
Figure 10 shows how to set FE and DE in Transmit System Interface Slave mode. In this mode, TSCKn/MTSCK and TSFSn/MTSFS input clock and frame pulse from external, and TSDn/MTSD input data from external. If the TSCKn/MTSCK rising edge samples TFSn/MTSFS at middle, then set FE to ‘1’. If the TSCKn/MTSCK falling edge samples TFSn/MTSFS at middle, then set FE to ‘0’. If the TSCKn/MTSCK rising edge samples TSDn/MTSD at middle, then set DE to ‘1’. If the TSCKn/MTSCK falling edge samples TSDn/MTSD at middle, then set DE to ‘0’.

Figure 10. Transmit Clock Slave Mode (Single Clock)
Figure 11 shows how to set FE and DE bits in Transmit System Interface Master mode. In this mode, TSCKn and TSFSn output clock and frame pulse, and TSDn input data. If set FE to ‘1’, TSFSn will be updated after TSCKn rising edge. If set FE to ‘0’, TSFSn will be updated after TSCKn falling edge. If the TSCKn rising edge samples TSDn at middle, then set DE to ‘1’. If the TSCKn falling edge samples TSDn at middle, then set DE to ‘0’.

**Figure 11. Transmit Clock Master Mode (Single Clock)**
4.2 TIMESLOT/CHANNEL OFFSET & BIT OFFSET

Timeslot/channel offset and bit offset are both supported in all operation modes. Figure 12 and Figure 13 show some examples of TS/CH offset and bit offset in receive system interface.

**Figure 12. TS/CH Offset & Bit Offset - Example 1**

BOFF[2:0] = 010, TSOFF[6:0] = 0000000

**Figure 13. TS/CH Offset & Bit Offset - Example 2**

BOFF[2:0] = 001, TSOFF[6:0] = 0010000

In Multiplexed mode, the TS/CH offset of each link should be set to different value to avoid data conflict. For example:
- Set TSOFF of Link 5 to 0;
- Set TSOFF of Link 6 to 1;
- Set TSOFF of Link 7 to 2;
- Set TSOFF of Link 8 to 3;
5 OPERATION OF DOUBLE CLOCK MODE

The SuperJET device can operate with either a single-bit / single-clock mode of operation or a single-bit / double-clock mode of operation. In the double clock mode of operation, the FE bit determines if the frame sync is sampled on the rising edge (FE = 1) or falling edge (FE = 0). Since each "bit cycle" now contains four edges the EDGE bit and DE bit together select one of the four edges to sample data.

Below are two drawings showing two possible frame selections and the data sample edges for those cycles. It should be noted that double clock mode is not supported in Master Mode or in the T1/J1 rate (1.544Mbps clock and data) in Slave Mode.

Table 8: CMS in RBIF Operation (b1, X46H) & in TBIF Operation (b2, X42H)

<table>
<thead>
<tr>
<th>CMS</th>
<th>RSCKn</th>
<th>MRSCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.048 MHz</td>
<td>8.192 MHz</td>
</tr>
<tr>
<td>1</td>
<td>4.096 MHz</td>
<td>16.384 MHz</td>
</tr>
</tbody>
</table>

Table 9: EDGE in RBIF Bit Offset (b3, X4AH) & in TBIF Option (b3, X45H)

<table>
<thead>
<tr>
<th>EDGE Bit</th>
<th>Edge Selection of RSCKn / MRSCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>first active edge</td>
</tr>
<tr>
<td>1</td>
<td>second active edge</td>
</tr>
</tbody>
</table>

Table 10: Edge Selection Based on EDGE, FE & DE Bits

<table>
<thead>
<tr>
<th>EDGE Bit</th>
<th>FE = DE</th>
<th>FE ≠ DE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1st Edge</td>
<td>2nd Edge</td>
</tr>
<tr>
<td>1</td>
<td>3rd Edge</td>
<td>4th Edge</td>
</tr>
</tbody>
</table>

Figure 14. Data Sample Edge When FE = 1

Figure 15. Data Sample Edge When FE = 0
6 SUPERJET ST-BUS® EXAMPLE

6.1 RECEIVE DIRECTION

Figure 16. Receive Slave Mode

<table>
<thead>
<tr>
<th>System Side</th>
<th>Line Side</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSCKn</td>
<td>SuperJET</td>
</tr>
<tr>
<td>TSDn</td>
<td>TTIPn</td>
</tr>
<tr>
<td>TSFSn</td>
<td>TRINGn</td>
</tr>
<tr>
<td>TSIGn</td>
<td></td>
</tr>
</tbody>
</table>

SuperJET

Receive

Transmit

Figure 17. ST-BUS® Receive Timing aka System Side RX

Table 11: Receive Slave & Multiplexed Modes

<table>
<thead>
<tr>
<th>Input Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSFSn / MRSFS</td>
<td>input to SuperJET</td>
</tr>
<tr>
<td>RSCKn / MRSCK</td>
<td>input to SuperJET</td>
</tr>
<tr>
<td>RSDn / MRSD</td>
<td>output from SuperJET</td>
</tr>
</tbody>
</table>

Frame pulse is sampled on the falling edge of clock, so:
FE (b2, X46H) = 0;
Frame pulse active state is low, so:
FSINV (b4, X48H) = 1;
Data is transmitted on the falling clock edge, so:
DE (b3, X46H) = 0;
So for ST-BUS® we want double clock, so:
Data needs to be updated on the first active edge, so:
EDGE (b3, X4AH) = 0;
CMS (b1, X46H) = 1;
RSCKn = 4.096 MHz;
MRSCK = 16.384 MHz.
Summary:
FE (b2, X46H) = 0;
FSINV (b4, X48H) = 1;
DE (b3, X46H) = 0;
EDGE (b3, X4AH) = 0;
CMS (b1, X46H) = 1.
6.2 TRANSMIT DIRECTION

Figure 18. Transmit Slave Mode

Table 12: Transmit Slave & Multiplexed Modes

<table>
<thead>
<tr>
<th>TSFSn / MTSFS</th>
<th>input to SuperJET</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSCKn / MTSCK</td>
<td>input to SuperJET</td>
</tr>
<tr>
<td>TSDn / MTSD</td>
<td>input to SuperJET</td>
</tr>
</tbody>
</table>

Frame pulse is sampled on the falling edge of clock, so:
FE (b3, X42H) = 0;
Frame pulse active state is low, so:
FSINV (b1, X42H) = 1;
Data is sampled on the rising clock edge, so:
DE (b4, X42H) = 1;
So for ST-BUS® we want double clock, so:
EDGE (b3, X45H) = 0;
CMS (b2, X42H) = 1;
TSCKn = 4.096 MHz;
MTSCK = 16.384 MHz.
Summary:
FE (b3, X42H) = 0;
FSINV (b1, X42H) = 1;
DE (b4, X42H) = 1;
EDGE (b3, X45H) = 0;
CMS (b2, X42H) = 1.

Figure 19. ST-BUS® Transmit Timing aka System Side TX
### 7 SUPETJET GCI EXAMPLE

#### 7.1 RECEIVE DIRECTION

**Figure 20. Receive Slave Mode**

Table 13: Receive Slave & Multiplexed Modes

<table>
<thead>
<tr>
<th>RSFSn / MRSFS</th>
<th>input to SuperJET</th>
</tr>
</thead>
<tbody>
<tr>
<td>RSCKn / MRSCK</td>
<td>input to SuperJET</td>
</tr>
</tbody>
</table>

Frame pulse is sampled on the falling edge of clock, so:
- FE (b2, X46H) = 0;

Frame pulse active state is high, so:
- FSINV (b4, X48H) = 0;

Data is transmitted on the falling clock edge, so:
- DE (b3, X46H) = 0;

So for GCI we want double clock, so:
- CMS (b1, X46H) = 1;
- RSCKn = 4.096 MHz;
- MRSCK = 16.384 MHz.

Summary:
- FE (b2, X46H) = 0;
- FSINV (b4, X48H) = 0;
- DE (b3, X46H) = 0;
- EDGE (b3, X4AH) = 0;
- CMS (b1, X46H) = 1.

**Figure 21. Receive Timing aka System Side RX**
### 7.2 TRANSMIT DIRECTION

**Figure 22. Transmit Slave Mode**

- **SuperJET**
  - TSEn
  - TSFSn
  - TSIgn
- **System Side**
  - TSDn
  - TSCKn
  - RSFSn
  - RSig
  - RSCKn
  - RSDn
- **Line Side**
  - TSDn
  - TSCKn
  - TSFSn
  - RSDn
  - RSig
  - RSCKn

#### Table 14: Transmit Slave & Multiplexed Modes

<table>
<thead>
<tr>
<th>TSFSn / MTSFS</th>
<th>input to SuperJET</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSCKn / MTSCK</td>
<td>input to SuperJET</td>
</tr>
<tr>
<td>TSDn / MTSDD</td>
<td>input to SuperJET</td>
</tr>
</tbody>
</table>

Frame pulse is sampled on the falling edge of clock, so:
- FE (b3, X42H) = 0;
- Frame pulse active state is high, so:
  - FSINV (b1, X42H) = 0;
- Data is sampled on the falling clock edge, so:
  - DE (b4, X42H) = 0;
- So for GCI we want double clock, so:
- Data needs to be sampled on the second active edge, so:
  - EDGE (b3, X45H) = 1;
  - CMS (b2, X42H) = 1;
  - TSCKn = 4.096 MHz;
  - MTSCK = 16.384 MHz.

Summary:
- FE (b3, X42H) = 0;
- FSINV (b1, X42H) = 0;
- DE (b4, X42H) = 0;
- EDGE (b3, X45H) = 1;
- CMS (b2, X42H) = 1.

**Figure 23. GCI Transmit Timing aka System Side TX**
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