Board Timing Adjustment Using Hyperlynx Software

Application Note
AN-433

Notes

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Background

Because of ever higher clock frequencies, general board timings, such as setup and hold times, must be calculated more accurately than ever. When designing systems, this basic issue now requires more attention and more resources because timing margins have been significantly reduced.

More specifically, a board designer should not only base his timing calculation on receiver IC capacitances but should also take PCB traces into account because these traces start to behave like a transmission line at high frequencies (>100MHz). Fixed capacitance load-based timings generally used in component data sheets are no longer sufficient to perform accurate board timing analysis. A board designer should correct/adjust these theoretical timings with respect to his specific system. The development of DDR memory is a perfect example of this trend, and simulation has become de facto necessity to insure timing integrity in such systems.

IDT has successfully used Hyperlynx simulation software on several designs. This Application Note describes the process of correcting data sheet figures through simulation. Data sheet timing values include both the logic delays and the delay through the I/O driver, but they fail to account for external factors, such as real load or PCB traces. Accordingly, for any given signal path, the following two primary delays must be be determined in order to obtain actual timing values:

- The compensation time, Tcomp, is due to the load difference between the standard data sheet load (timings are measured under fixed loading condition) and the actual board load, such as receivers, traces, and terminations. This compensation (which could be positive or negative) is equivalent to load derating and corrects the timing on the driver side.
- The pin-to-pin board flight time, Tpin, is due to the signal propagation along the trace. This compensation (which is always positive) corrects the timing on the receiver side.

Once compensated for these two delays has been determined, data sheet output delays can be corrected, and system setup and hold times can be properly calculated. For each load change, a separate correction is necessary because both timing correction factors are load-dependant.

Timing Correction

Integrated circuit delays presented in data sheets are specified at a fixed test load which varies from one manufacturer to another and from one product to another. For example, the timings for the RC32355 device (a member of the IDT™ Interprise™ family of integrated communications processors) are measured under the following load: a 50 Ohms series resistor and a 25pF capacitor.

To simulate signal propagation and generate timing delays, IBIS model (I/O Buffer Information Specification) are usually used. An IBIS model describes the part I/O buffer, but does not provide any information about internal logic delays. Therefore, IBIS-based simulation should only be used in addition to the data sheet figures rather than replacing them: both sets of data are needed to determine accurate timing parameters.

Figure 1 displays the simulation circuit on Hyperlynx/Linesim. The IBIS model is IDT's RC32355 processor, and the signal analyzed is the SDRAM clock.

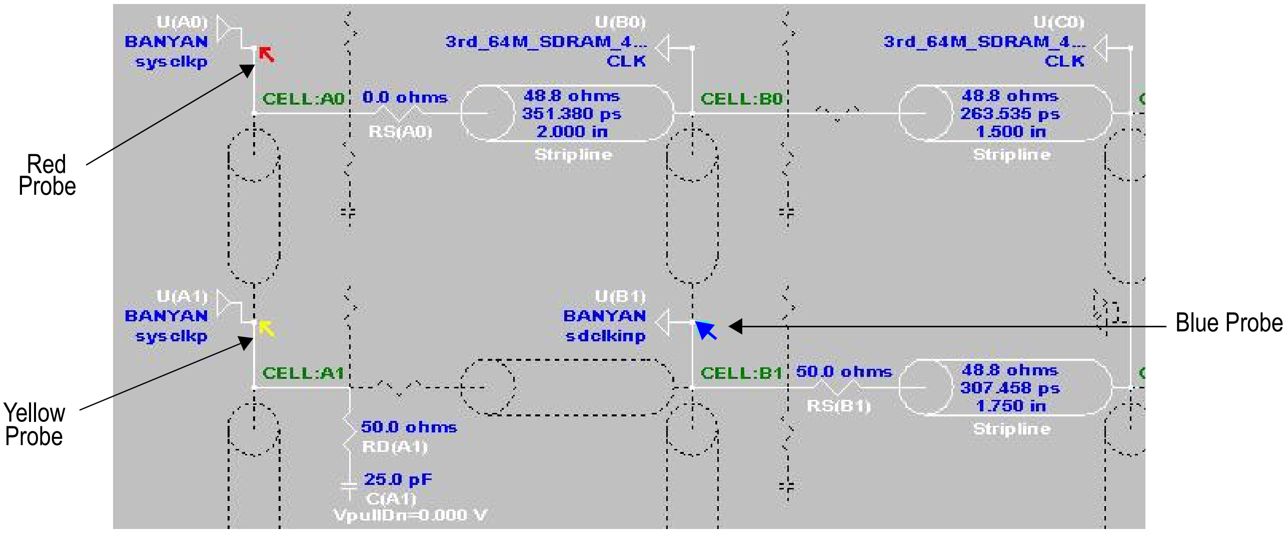


Figure 1 Hyperlynx/Linesim Simulation Circuit

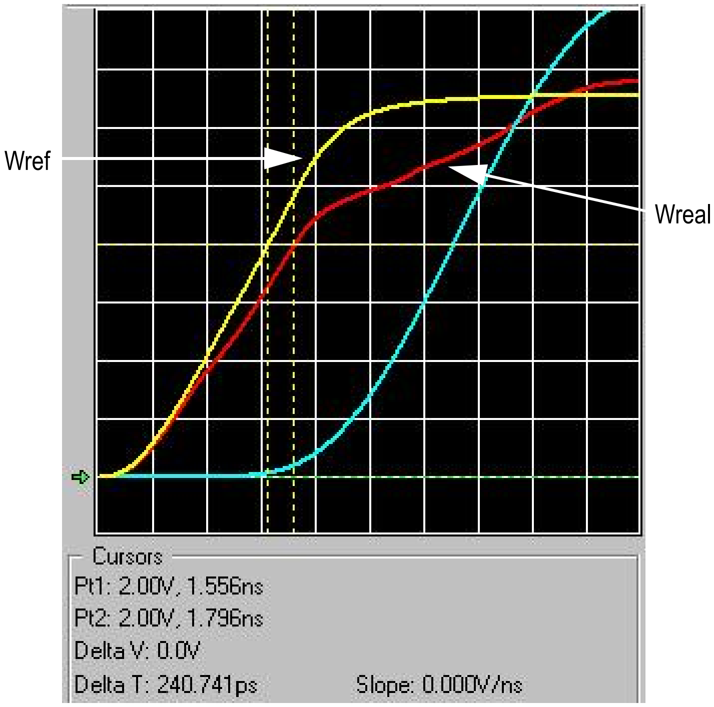
Figure 1 shows two distinct circuits:

- The RC32355 SDRAM clock pin drives a 25pF capacitor associated with a 50 Ohm resistor, termination, which accounts for the theoretical data sheet test load. The yellow probe monitors the driving edge reference.
- The RC32335 SDRAM clock pin drives a SDRAM clock path (5 inches of traces + 2 SDRAM chips + RC32355 sysclkin input pin) extracted from an existing design. The two probes, red and blue, monitor the driving waveform under real load and the receiving waveform at the end of the line, respectively.

Compensation Time

Compensation time (Tcomp) is defined as the delay between the time the driving edge, probed at the output pin, crosses the Measurement Voltage threshold (1.8V in our case) at the manufacturer's standard test load and the time it crosses at the actual load. Tcomp may therefore be negative or positive depending on whether the actual load is smaller or bigger than the standard test load. Tcomp is explicitly displayed in Figure 2 as the difference between the yellow waveform (Wref) and the red waveform (Wreal).

When Tcomp is known, a board designer can apply it to all the lines with the same output driver and the same load. If one of these two parameters differs, Tcomp must be measured again, as it is the driver characteristics and load characteristics which determine it.



Pt1: 2.00V, 1.556ns
Pt2: 2.00V, 1.796ns
Delta V: 0.0V
Delta T: 240.741ps Slope: 0.000V/ns

Figure 2 Compensation Time

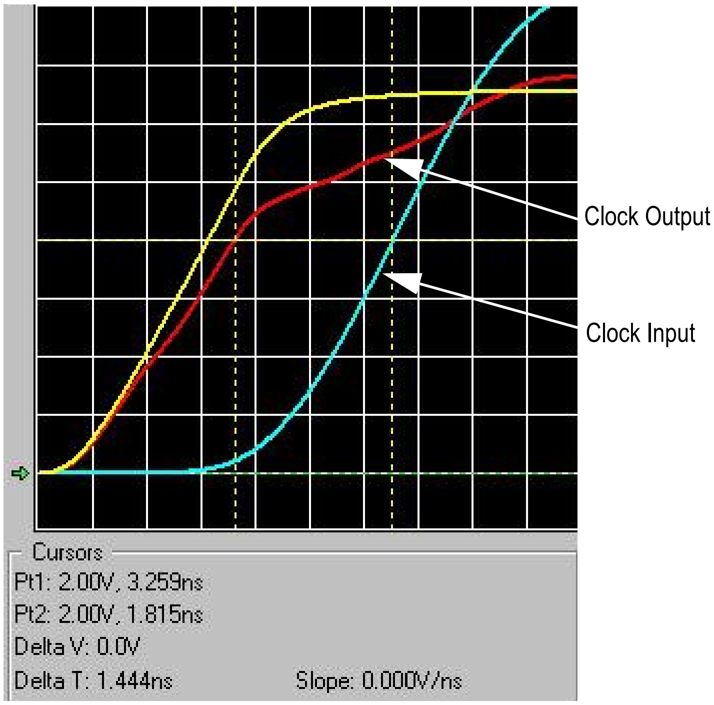
The yellow waveform (Wref) represents the driving edge (Rising in this case) at the output pin, when the RC32355 I/O buffer model drives the IDT standard load (the standard load serves as the basis for determining the timing values found in the data sheet). The red waveform (Wreal) represents the driving edge (Rising in this case) at the output pin, when the RC32355 I/O buffer model drives the actual board load.

Here, the actual load delays the real driving waveform by 240ps with respect to the reference driving waveform. In certain cases, when the reference load is high (35pF+) and the actual load small (one single chip system), the real driving waveform can precede the reference driving waveform.

Pin-to-Pin Delay (Flight Time)

The pin-to-pin delay (Tpin) is caused by the signal propagation along the trace. Delay depends on the trace length, the receiver loads, and the termination scheme.This delay becomes difficult to calculate if the signal is driven to multiple loads not connected through a Daisy-chain topography, i.e., the trace forks at multiple places. In such cases, simulation software, such as Hyperlynx, comes in handy, because any complex routing scheme can me modelized and the associated delay easily extracted.

Figure 3 shows the simulated pin-to-pin delay between the RC32355 SDRAM clock output (red waveform) and the RC32355 SDRAM clock input (blue waveform) at the end of the line.



Cursors
Pt1: 2.00V, 3.259ns
Pt2: 2.00V, 1.815ns
Delta V: 0.0V
Delta T: 1.444ns Slope: 0.000V/ns

Figure 3 Pin-to-Pin Delay Time

The delay caused by the signal propagation is merely the length of the line divided by the speed of the signal in the line: T(line) = Length/vel. The signal propagation delay is always positive and its value can range from pico-seconds to nano-seconds. For example, 1 inch of FR4 trace roughly accounts for a 180ps delay. The receiver input capacitance associated with trace length and number of terminations can range from a simple RC filter to a more complex pattern, and it is this filter which determines the amount of delay in the system. This RC filter tends to slow down the signal transition time during both falling and rising edges, resulting in further delay at the receiving side. In our example, we measured a total 1.45ns pin-to pin delay due to the two SDRAM input loads, the 5 inches of traces, the 50 Ohms series termination, and the RC32355 input load.

Conclusion

To determine overall delay, one should add both delays previously described, Tcomp and Tpin. The result should be added or subtracted, depending on its sign, to the timing value found in the data sheet. In our example, the SDRAM clock will arrive at the processor input with an extra 1.7ns delay, and this delay must be taken into account in the hold/setup time calculations.

> **Note:** The same type of delay (loads, trace length, etc.) also applies to other signals, such as commands, addresses, and data lines. These signals are likely to be delayed in a different way, because of layout and load-driving strength differences, and will, therefore, require separate timing corrections. When timing for both the clock and the “other” signals just mentioned has been adjusted as described above, then setup and hold times on the receiving end can be accurately analyzed.