DUAL-PORT INTERRUPT EXPANSION

APPLICATION NOTE AN-70

by John C. Mein, Field Applications Engineering

Synopsis: This tech note describes a simple technique to obtain additional interrupts from each side of a dual-port when expanding in width.

Many of today's dual- ports offer the capability of allowing one side to have an interrupt generated to the other side. This allows the signaling of messages such as data ready, data overflow, etc. This is a handy feature used quite often. IDT'S dual-ports offer two interrupts per part — one to each side when operated in stand alone mode. When expanding in depth or width additional interrupts can be obtained—exactly how many more depends on how the expansion is accomplished.

A feature available in many dual-ports is depth expansion capability. One simply uses external address decoding to select one of multiple dual-ports (usually all masters). An example of this scheme is offered by the IDT 7005 8kx8 dual-port and shown in Figure 1.

This depth expansion results in two interrupts being available on either side. For side A to generate an interrupt to side B, side A must write anything to location 1FFF (8191 decimal). This generates the interrupt to side B which is cleared only by side B reading the same location 1FFF. Side B can likewise generate an interrupt to side A—the only difference is the memory location is now 1FFE (8190 decimal). Another set of interrupts also resides at locations 3FFF (16383 decimal) and 3FFE (16382 decimal).

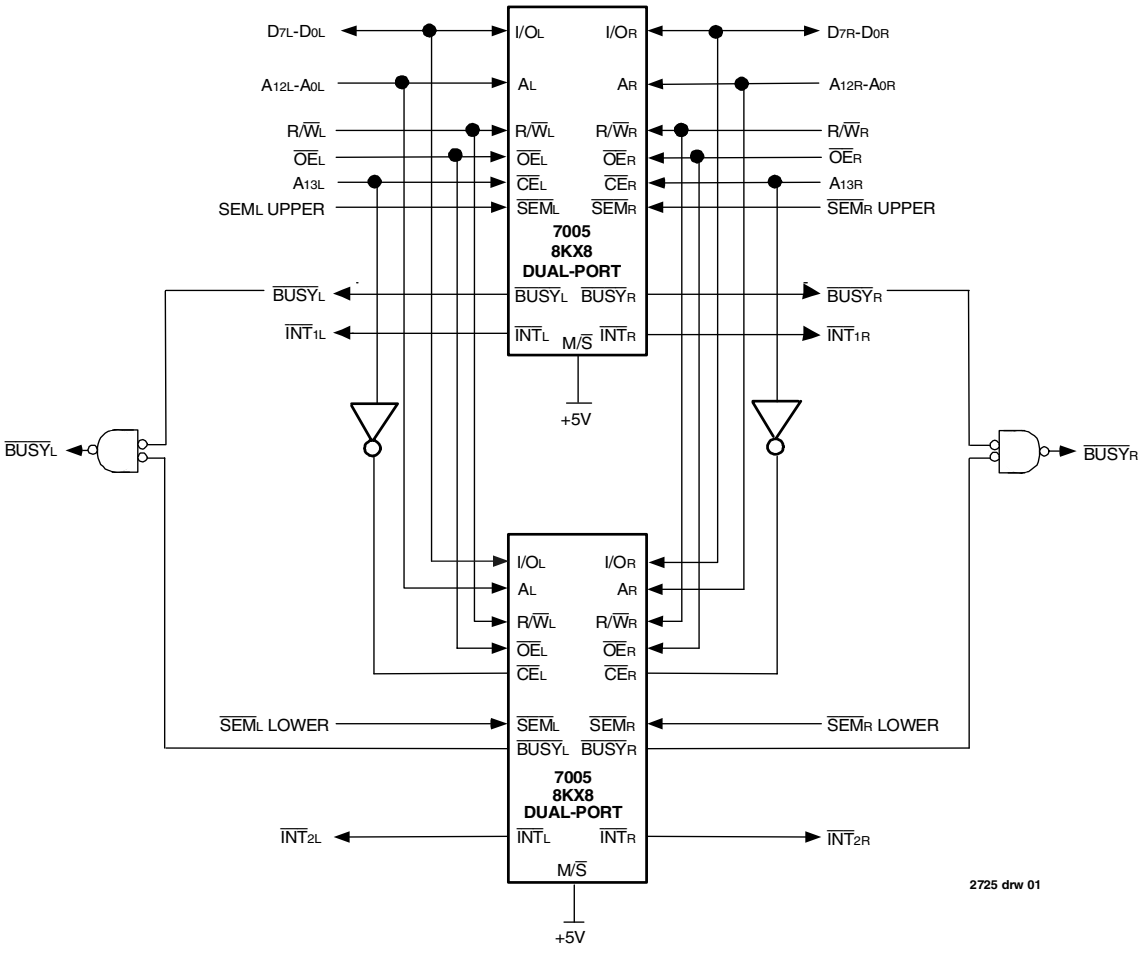

Figure 1. Depth Expansion of the IDT7005 8k x 8 Dual-Port

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Figure 2 shows a typical system consisting of two 8kx8 dual-ports expanded in width. Here one must be careful to have address arbitration done by only one chip (the master) and having the other chips (the slaves) follow the master. This is easily accomplished using separate master and slave chips on earlier devices (such as the IDT7130/7140, IDT7132/7142, IDT7133/7143, and the IDT71321/421) or on the newer devices (such as the IDT7005/7006 and the IDT7024/7025) by connecting the M/$\overline{S}$ pin appropriately. All address lines are tied in parallel and only one interrupt for each side (since the address mapping is the same for both chips) is used. The other interrupts are not connected.

However, when expanding in width, one can have extra interrupt lines (one per chip) generated by simply inverting any address line between the two (or more) dual-ports. As shown in Figure 3 we have inverted address line A12. The only item one needs to be careful about is to insure you correctly calculate the new address location for the additional interrupts. For this example, instead of the interrupts being at only 1FFF and 1FFE they are now also at FFF (4095 decimal) and FFE (4094 decimal). It would also be possible to map the interrupts to be contiguous in the address map (i.e. map them to be at FFE, FFF, 1000, and 1001).

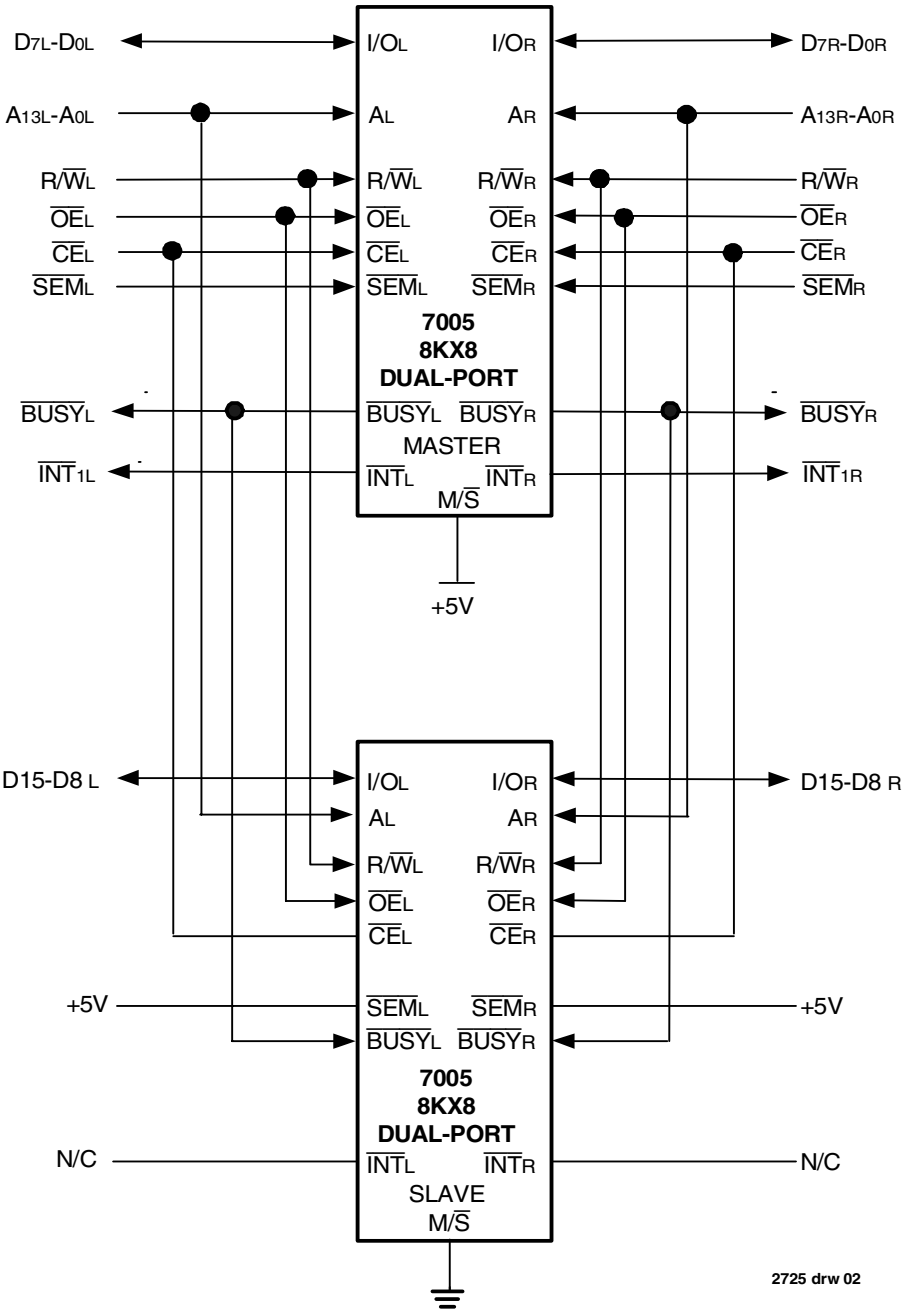

Figure 2. Normal Width Expansion of the IDT7005 8k x 8 Dual-Port

Another way to accomplish this would be to separate the chip enables for each dual-port. Then, to enable an interrupt, just enable and write to the appropriate dual-port. The advantage of this technique is that no additional address decoding delay is inserted.

The same methodology can be applied to multiple width expansions. For instance, using a 7006 16kx8 dual-port for a 32 bit system (resulting in a 16kx32 memory) would result in four interrupts for each side for a total of 8 (compared with only two by the normal expansion method).

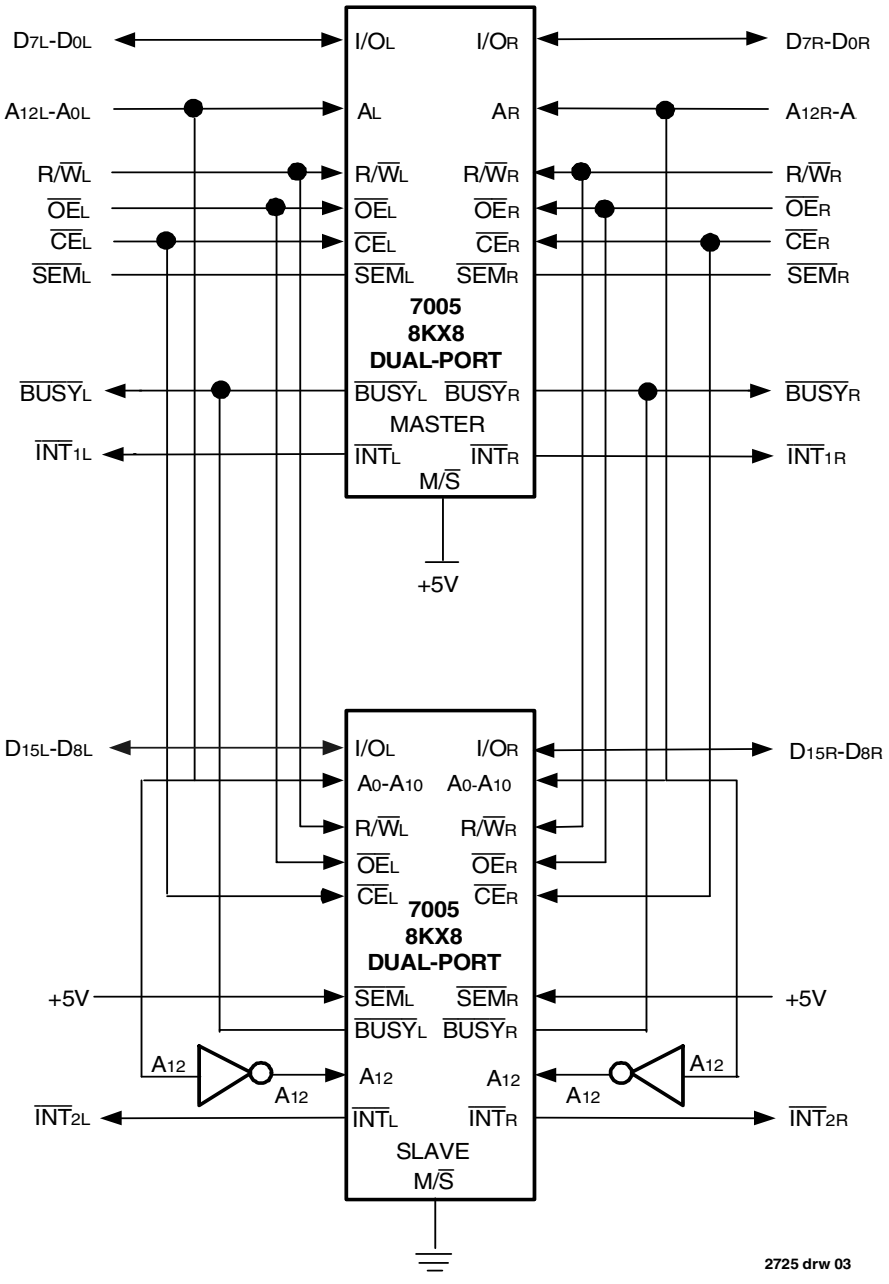

Figure 3. Width Expansion with More Interrupts

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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