

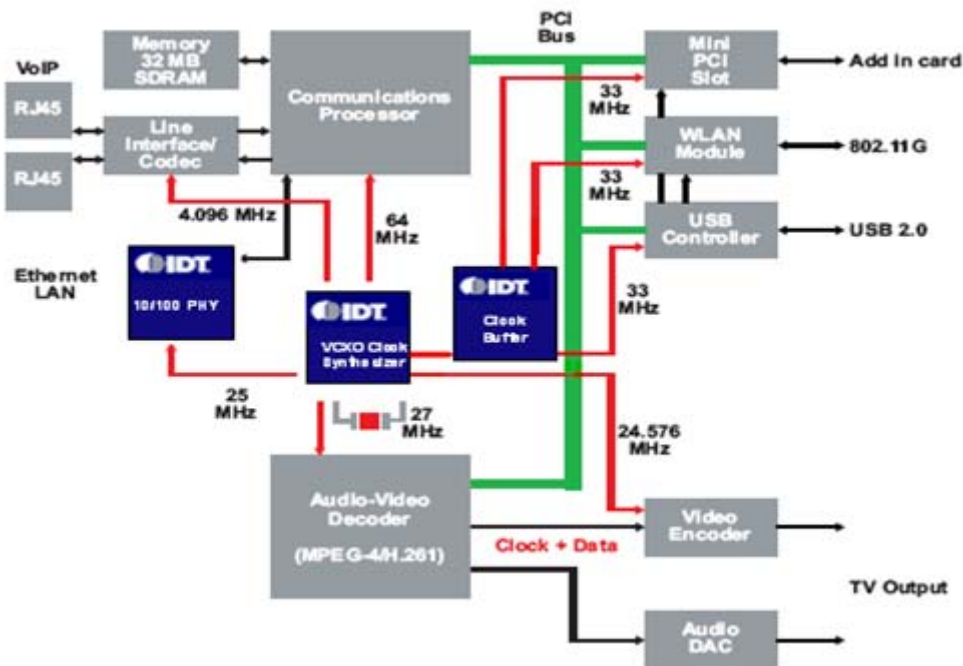
## Introduction

High performance clock buffers are widely used in digital consumer and communications applications for distribution of clock signals. A critical parameter for these buffers is additive phase noise that can degrade system performance and reliability. This application note briefly explains the theory behind measuring additive phase noise for IDT clock buffers and summarizes the additive phase jitter results for several widely used IDT clock buffers. Other AC parameters of interest for buffers are input to output propagation delay and output to output skew.

In synchronous systems where timing and performance of the system is dependent on the clock, integrity of the clock signal is important. Designers must optimize board layout, use clean power supplies and follow recommended decoupling and termination schemes for the outputs in order to meet the EMI and timing budgets for their application.

IDT has a large variety of low skew clock distribution devices to meet all your application needs. Figure 1 shows a typical set top box application where an IDT clock buffer is used to distribute 33MHz PCI clocks to multiple PCI slots.

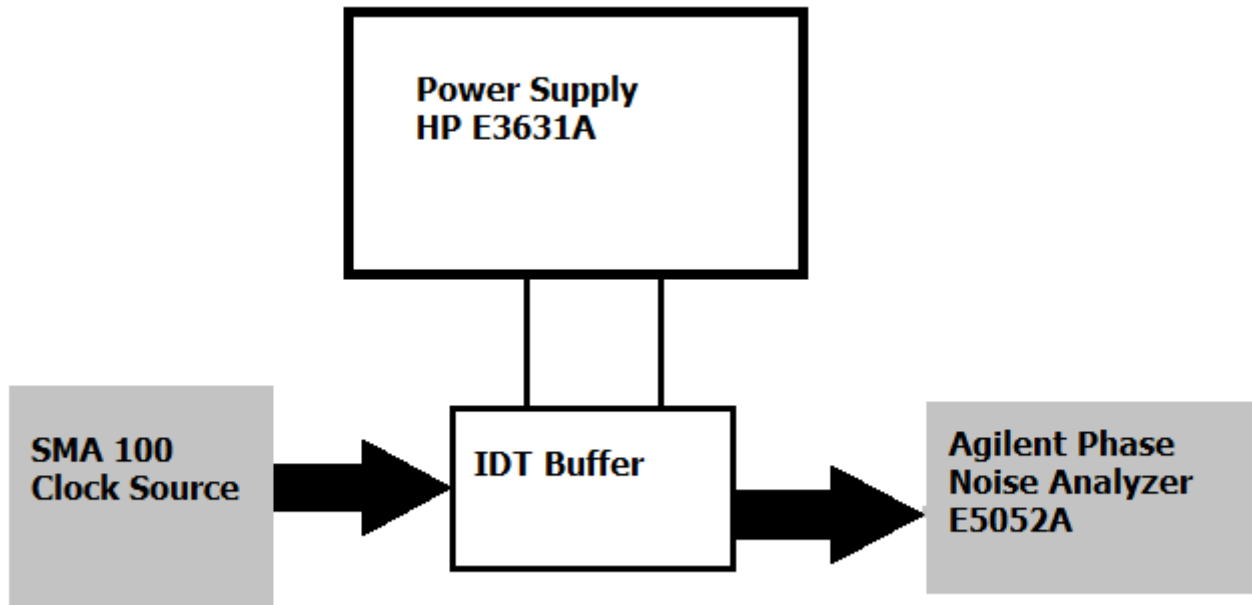
**Figure 1. Set Top Box Application Diagram Using an IDT Clock Buffer**



## Phase Noise Measurement

The Agilent 5052A Phase Noise analyzer is used to take phase noise plots and the RMS jitter is calculated over an offset range for a center carrier frequency.

**Figure 2. Test Setup for Additive Jitter Measurements**



## Additive Phase Noise

Any component in a signal chain has some amount of noise at its output that is generated internally (not including the contribution due to the external reference noise at the input). It is useful to measure the phase noise at the output of a device in such a way that the phase noise of any external source is canceled out. The phase noise so measured is specified as the additive phase noise of the device. It is the amount of phase noise that the device (clock buffer in our case) adds to the signal chain. IDT clock buffers have ultra low additive phase jitter thereby allowing system designers to distribute multiple copies of a clean clock to other devices on their system. The clock signal integrity is maintained thereby eliminating the need for additional jitter cleaning components. By considering the phase noise contribution due to the buffer alone, it is then possible to foretell the degree to which the buffer impacts the total system phase noise when used in conjunction with components such as oscillators and clock sources, each of which contribute to the phase noise of the total system. In many cases, the phase noise of one element in the chain dominates the system phase noise.

## Additive Jitter

Additive jitter is defined as the added amount of jitter to the input signal caused by the device itself and can be calculated as:

$$\text{Total Additive Jitter} = \text{sq root} ((\text{output clock jitter})^2 - (\text{input clock rms jitter})^2)$$

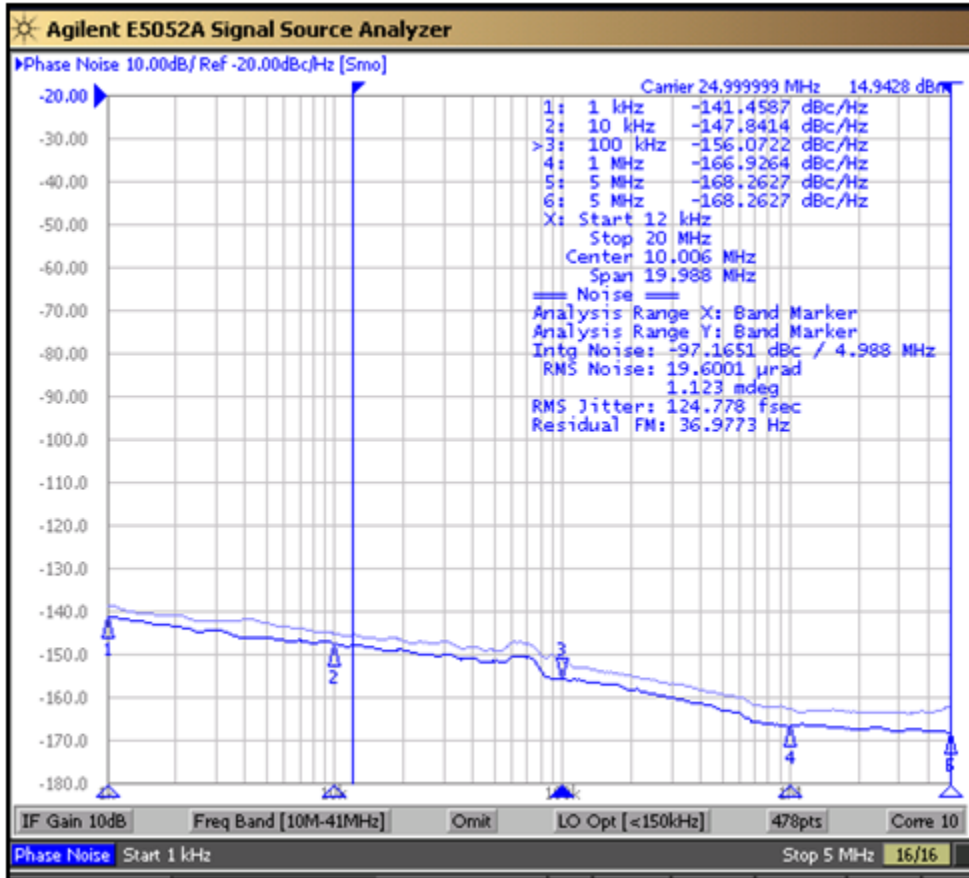
It assumes that the noise processes are random and the input noise is not correlated to the output noise. Additive jitter must be measured with a clock source where phase noise is below the noise floor of the buffer itself.

The input clock reference source used for phase jitter measurements is a SMA100A clock generator which is very low phase noise. The measured phase noise of the input clock to the IDT buffers used varies over frequencies. Below are phase noise measurements of frequency equal to 25MHz. The RMS jitter is measurement over the offset range of 12kHz to 20MHz. The average phase noise RMS Jitter measured on the SMA clock source is 80fs. We will use this value for our calculations of additive jitter in this applications note. This value represents the input clock RMS Jitter for the below formula.

### Additive Phase Noise Results

Measurements for Additive Phase Noise were taken on five of the most commonly used IDT Clock Buffers at three frequencies: 25MHz, 100MHz and 125MHz. All measurements contained in this report were taken at room temperature and at the nominal voltage.

Figure 3. Phase Noise on ICS553 25MHz Clock Output and 25MHz Input Clock Source



### Summary of Additive Jitter Results

The additive phase noise measurement results presented in this application note confirm ultra low additive phase jitter across IDT’s family of clock buffers. The additive phase jitter varies minimally over the buffer input frequency range and operating voltage range. All measurement data is in femto seconds (fs).

Table 1. Summary of Additive Jitter on Commonly Used IDT Clock Buffers

MHz	Range	IDT2305NZ	ICS551	ICS553	IDT74FCT3807	IDT5T30533
25	12kHz–20MHz	120.11	101.07	89.87	312.50	404.54
100	12kHz–20MHz	53.23	76.51	48.37	82.53	52.84
125	12kHz–20MHz	69.23	87.11	55.38	267.24	176.09



## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
  - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
  - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.