Introduction

This application note will discuss the different serial programming methods available for the F1975 and F1978 6-Bit, 75-Ohm Digital Step Attenuators (DSA): Conventional Serial Programming and Direct Serial Programming. The F1975 uses Conventional Serial Programming. The F1978 can use either method; however, the Direct Serial Programming method can result in higher current consumption and unintended output swings.

Both programming methods utilize the three standard serial interface signals. The three control signals are Clock (CLK in Figure 1), Data (DATA), and Latch Enable (LE). The Clock signal allows the device to have a specific timing, and it is always a square wave. The DATA signal defines what each data bit will be, and it is either a logic HIGH or logic LOW. For both the F1975 and F1978, the data word is 6 bits wide with each bit clocked into a serial shift register on the clock's rising edge. The Latch Enable (LE) is used differently for each method and is described in the following sections. In the diagrams, V_{MODE} refers to the signal line on the F1975 or F1978 that configures the device in either Serial (logic HIGH) or Parallel (logic LOW) Mode.

Conventional Serial Programming

Conventional Serial Programming utilizes the LE signal to "latch" the loaded data word in the shift register into the active register when the LE pin transitions from logic LOW to logic HIGH. The content of the active register defines the device attenuation state. With this programming scheme, the DSA attenuation state update is completed in a single programming event. As long as LE is logic LOW, the DSA attenuation state will not change but the device will allow the data bits to be clocked into the shift register. Figure 1 shows a Conventional Serial Programming timing diagram for the F1975. The diagram also shows an example transition from 8.5 dB (Data = 010001_{BIN}) to 9.0 dB (Data = 010010_{BIN}). As shown, the DSA attenuation state changes to the desired programmed value, in this example 9.0 dB, only after LE is toggled from LOW to HIGH.

After the data word in the shift register has been latched into the active register, the LE signal must be dropped LOW. This allows shifting new data into the shift register without uploading it to the active register until the next time LE goes HIGH.

Figure 1. Conventional Serial Programming Timing Diagram with Example Device Attenuation State Change from 8.5 dB to 9.0 dB
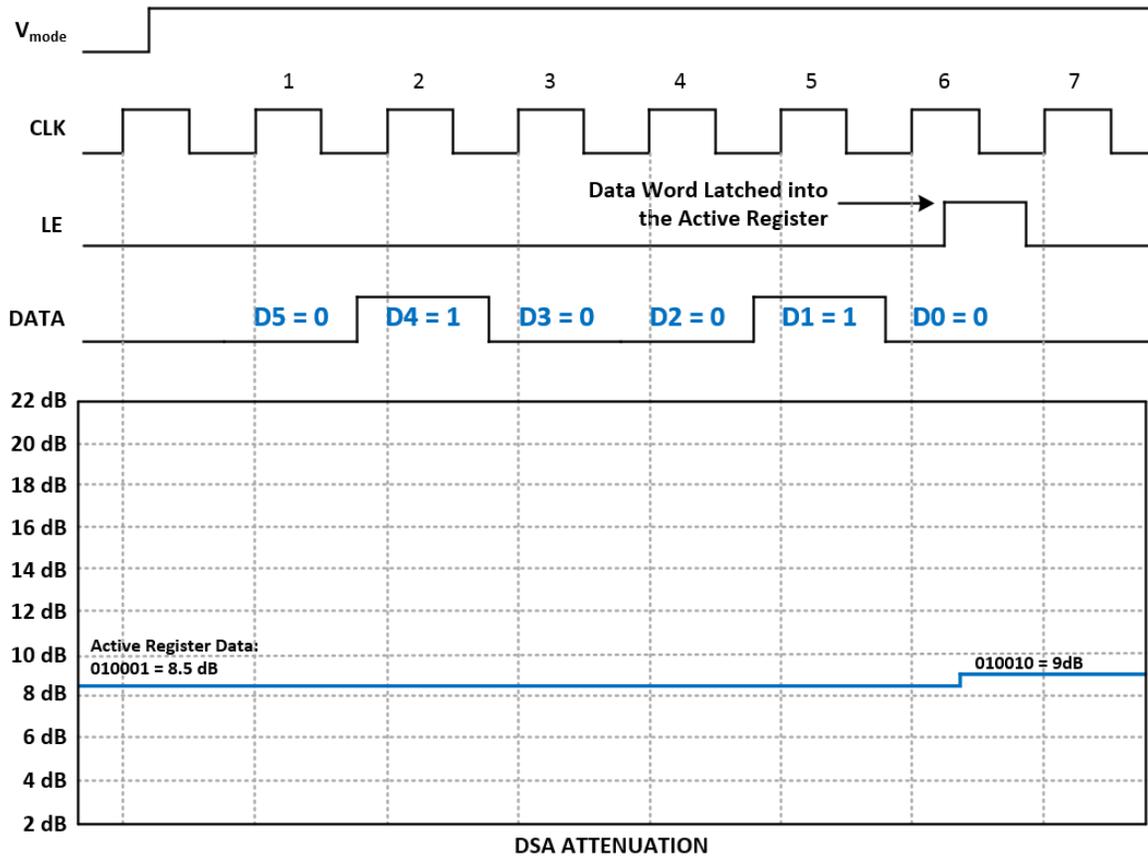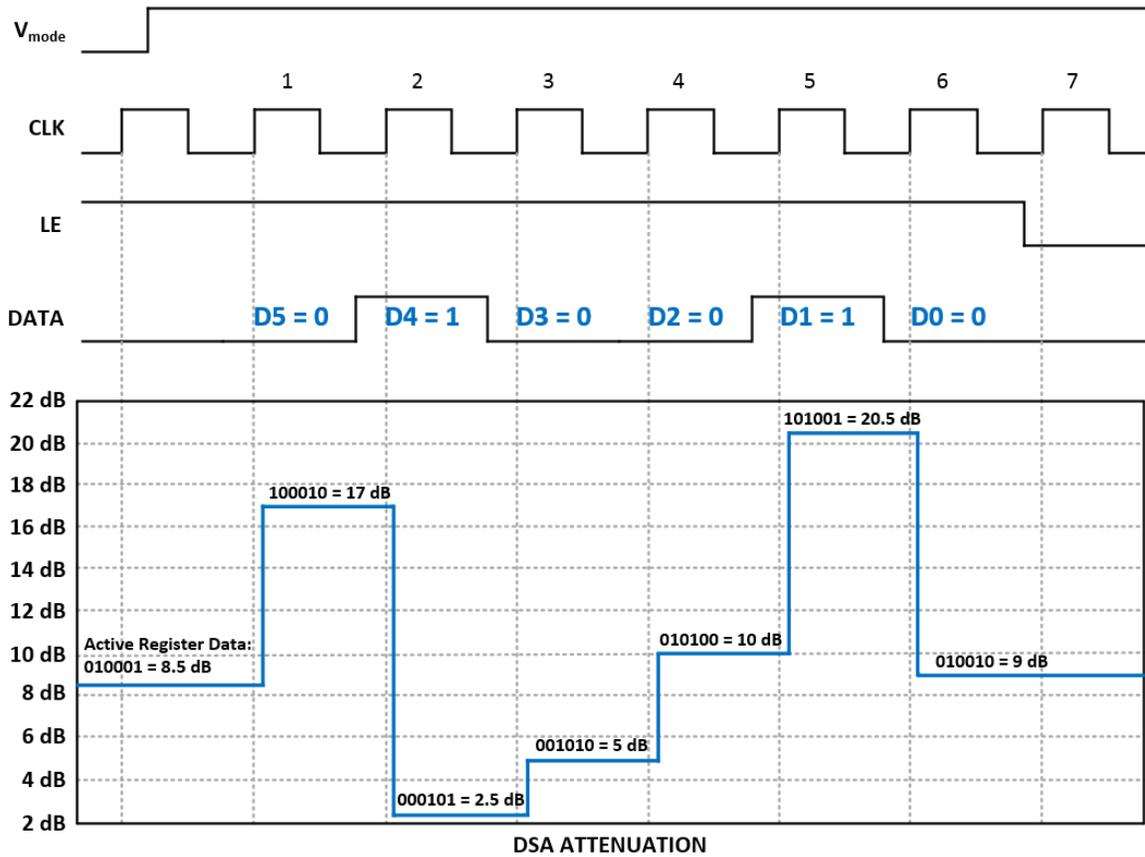

F1978 Direct Serial Programming

The F1978 allows using Direct Serial Programming method. Direct Serial Programming is similar to Conventional Serial Programming because when LE is LOW, the F1978 allows data to be clocked into the shift register (without changing the attenuation) and it will be latched into the active register (thus changing the attenuation) when LE goes from LOW to HIGH. However, for Direct Serial Programming, the LE signal can be statically maintained at a logic HIGH to continue programming the device with subsequent attenuation values. With this programming scheme, the F1978 will change the attenuation state as each subsequent data bit is clocked into the device. Figure 2 shows an example of the Direct Serial Programming timing diagram for the F1978. The diagram depicts an attenuation state change from 8.5 dB (data = 010001_{BIN}) to 9.0 dB (Data = 010010_{BIN}). The diagram displays the updated DSA attenuation state as each data bit is clocked into the device. In contrast to the Conventional Serial Programming method, which updates the DSA attenuation state in one clock cycle, the Direct Serial Programming method requires a full six clock cycles to enter a next data point, and there are attenuation swings (18 dB for this example) before the device settles to the final desired attenuation value.

It is critical to note that as long as LE is HIGH, any data bit clocked into the shift register will be immediately loaded into the active register and therefore update the DSA attenuation state as demonstrated in Figure 2. To prevent undesired DSA attenuation state changes, LE should be set to logic LOW after the final data bit of the desired attenuation state code is clocked into the device. Note that data bits will always be clocked into the shift register independent of the setting of LE.

One concern, as shown in the example in Figure 2, is the potentially large attenuation state swings when switching from one desired setting to another. This may result in undesired and possibly damaging power level changes in the system.

Figure 2.   F1978 Direct Serial Programming Timing Diagram with Example Device Attenuation State Change from 8.5 dB to 9.0 dB

Conclusion

There are different serial programming methods available for the F1975 and F1978. Each scheme relies on the state of LE as to when a data bit or data word is loaded into the device's active register, which in turn sets the DSA attenuation state. With the Conventional Serial Programming method, which can be used for both the F1975 and F1978, toggling LE from logic LOW to logic HIGH changes the DSA attenuation state in a single programming event. Bringing LE to logic LOW locks out any changes to the shift register for additional clock signals. This method is the typical programming method used in the industry.

With the Direct Serial Programming method, which is only available for the F1978, LE is held at a constant logic HIGH while data is clocked into the device. This results in a DSA attenuation state change on each clock cycle as a data bit is clocked in. Although both methods are available for the F1978 for system design and device programming flexibility, it is recommended that the Conventional Serial Programming scheme be used to prevent undesired swings in power level when switching between desired DSA attenuations settings. For more detailed information on the F1975 or F1978, including serial programming timing specifications, see the F1975 or F1978 product datasheets.

Revision History

Revision Date	Description of Change
May 1, 2017	First release of document.