Introduction

The IDT 82P338XX/9XX Synchronization Management Unit (SMU) for IEEE 1588 and Synchronous Ethernet (SyncE) provides tools to manage timing references. It has several different modes to align the output clocks, to control the skew, clock sources and timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks. This document focuses on clock alignment with a SYNC input.

SYNC Input Signals

Any of the 82P338XX/9XX clock inputs can be configured as a SYNC input. The SYNC input must be associated with a reference clock(s). The IN[3:14]_SYNC_SEL[3:0] bits associates a SYNC input with the applicable reference clock.

There is no specific setting to determination if the SYNC input is a Framing Pulse (FP) or Synchronizing Pulse (SP). It's determined on the overall configuration of the SYNC input, as described in this section, and understanding how the SYNC input is being used to generate the SYNC output and the clock outputs, as described in the following sections.

Support for the SYNC input must be set via the DPLL{1:2}_EXTSYNC_EN bit (default b'0, or disabled). All SYNC inputs must have the same frequency (1PPS, 2kHz, 4kHz or 8kHz), matching the setting in the DPLL{1:2}_SYNC_FREQ[1:0] bits. If the SYNC input is to be used solely as a SYNC, then the SYNC input should be disabled as a clock source for the DPLL; this is done by setting DPLL{1:2}_IN[1:14]_PRIORITY[3:0] to b'0000 (input is disabled for auto reference selection).

By default, the falling edge of the SYNC input is expected to be aligned with the rising edge of the input reference clock (see Figure 2). The rising edge of the SYNC input can be set to align with the rising edge of the input reference clock by setting the DPLL(1:2)_SYNC_EDGE bit to b'1 (see Figure 3). The phase relationship of the SYNC input to the reference clock can be in the range of 0.5UI early to 1UI late. How the SYNC input is sampled is described in the next section.

Figure 2. SYNC Input – Falling Edge (Default)
The frequency of the output clocks that are synchronous to the SYNC input must be equal to or higher than the associated reference clock (post divided, if applicable). If it is desired to have lower frequency output clocks, then a re-alignment must be triggered on the initial LOCK of the DPLL or when the DPLL comes out of HOLDOVER. Refer to Alignment of Output Dividers for details.

The SYNC input is also used to generate the FRame SYNC (FRSYNC) or Multi-FRame SYNC (MFRSYNC) output signal; refer to SYNC Output Signals for details.

**Sampling of SYNC input**

The sampling of the SYNC input is determined by the phase offset programmed via IN[1:14]_SYNC_PHASE[1:0] bits, and illustrated in Figure 4 through Figure 7. Typically, the "On Target" and "1 UI Late" options are used for SP applications; and the "0.5 UI Early" and "0.5UI Late" options are used for FP applications.
When the SYNC input is sampled by the input reference, the SYNC input must be within a valid window, as illustrated in the figures above. The sampling window size is captured in the table below.

### Table 1. SYNC Input Sampling Window Size

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_W$</td>
<td>SYNC input sampling window size</td>
<td></td>
<td></td>
<td>$1\mu s^{[a]} - 6\text{ns}$</td>
</tr>
</tbody>
</table>

[a] A UI is in reference to the DPLL’s PFD frequency configuration.

How the phase offset affects the SYNC output and/or the output clocks is captured in section **SYNC Output Signals**.

### Alignment of Fractional Input Divider

If an input reference clock has been divided down, then the divided clock edge would be in unknown position with respect to original reference clock. For example, if we divide the clock by 6, then the resulting clock could align to any of 6 input clock cycles. To ensure that the divided down reference clock is always in the same position, the input fractional dividers are synchronized by the SYNC input.
When the input reference is being divided down by the fractional divider, the SYNC input must meet specific setup/hold timing in relationship to the reference input. This setup/hold time is independent of the SYNC input sampling described previously, but does affect the SYNC input sampling with the resulting divided down reference input. The setup and hold times are captured in the table below.

**Table 2. Input Fractional Divider SYNC Input Setup & Hold Times**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_S )</td>
<td>SYNC input to IN( 3:14 ) Setup time</td>
<td>3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_H )</td>
<td>SYNC input to IN( 3:14 ) Hold time</td>
<td>0.5</td>
<td></td>
<td></td>
<td>UI[( a )]</td>
</tr>
</tbody>
</table>

[a] A UI is in reference to the DPLL's PFD frequency configuration.

Figure 9. Input Fractional Divider SYNC Input Setup/Hold

When using the fractional divider, the SYNC input must be configured to use the rising edge, by setting DPLL\{1:2\}_SYNC_EDGE bit to b'1 (as illustrated in Figure 9). The synchronizing of the input fractional dividers will occur on the next cycle of the original input reference clock. This means that a static 1UI offset needs to be accounted for. For example, if a 38.88MHz clock is divided down to 6.48MHz, the static offset would be approximately 25.72ns. This is illustrated in Figure 10 below.

**Figure 10. Fractional Input Divider Example – 38.88MHz divided down to 6.48MHz**

The static 1UI offset can be accounted for using the input skew adjustment registers. This adjustment is done post-phase detector, thus, will affect the alignment of the SYNC output and output clocks.
The sampling of the SYNC input will now be based on the divided down clock. However, with the setup/hold requirements for the input divider, the sampling range is limited on the SYNC input, as shown in Figure 12.

**Figure 12. Fractional Input Divider – SYNC Input Sampling**

As illustrated in Figure 12, the SYNC input will always appear to be ‘early’ in relationship with the divided down clock. For this reason, it is recommended to set the phase offset for the SYNC input to "0.5UI early" when using the fractional input divider to account for this.

**SYNC Output Signals**

From a high level, it can be said that a SYNC output is a re-sampled version of the SYNC input. The SYNC output aligns to the first edge of the associated reference clock that occurs after the edge of the SYNC input.

Both DPLL1 and DPLL2 can generate Frame SYNC (FRSYNC) and Multi-Frame SYNC (MFRSYNC) signals. The selection of which signal is assigned to the associated FRSYNC and MFRSYNC output pins is controlled by the FR_PATH_SEL bit and MFR_PATH_SEL bit, respectively.

Support for the FRSYNC output and MFRSYNC output is controlled via the FR_PDN bit & MFR_PDN bit, respectively. By default, the FRSYNC output is 8kHz and the MFRSYNC output is 2kHz. If the FRSYNC output is to be used as a SP (1PPS), then the output should be changed via DPLL{1:2}_8K_1PPS_SEL bit. If the MFRSYNC output is to be used as a SP (1PPS), then the output should be changed via DPLL{1:2}_2K_1PPS_SEL bit.

By default, the falling edge of the [M]FRSYNC output is aligned with the rising edge of the input reference clock (see Figure 13). The [M]FRSYNC output can be inverted by setting the DPLL{1:2}_8K_1PPS_INV bit or DPLL{1:2}_2K_1PPS_INV bit to b’1. The input-to-output delay of the SYNC output to the input reference clock edge is captured in the data sheet.
Based on the SYNC input sampling configuration (IN{1:14}_SYNC_PHASE[1:0] bits), the SYNC output and clock outputs will have different phase relationships with the rising edge of the reference input, as captured in Figure 15 through Figure 18. The input-to-output delay of the SYNC output and the clock outputs to the input reference clock is captured in the data sheet.
Figure 15. SYNC Output Alignment – On Target (Default)

Ref Input

SYNC Input

Output Clock

SYNC Output

Input-to-Output Delay

Figure 16. SYNC Output Alignment – 0.5 UI Early

Ref Input

SYNC Input

Output Clock

SYNC Output

Input-to-Output Delay
The SYNC output is a 50/50 clock by default. The FRSYNC output can be changed to a pulse based on the UI of OUT1 via DPLL{1:2}_FRSYNC_PULSE bit. In this case, OUT1 must be a clock coming from the same DPLL as the FRSYNC signal. The MFRSYNC output can be changed to a pulse based on the UI of OUT8 [1] via DPLL{1:2}_MFRSYNC_PULSE bit. In this case, OUT8 must be a clock coming from the same DPLL as the MFRSYNC signal.

[1] 82P33x31/x41 devices do not have control of OUT8, as it is internally routed to APLL3. This means that the MFSYNC output cannot be pulsed.
By default, the SYNC output pulse is aligned with the rising edge of OUT1/8 output reference clock. The SYNC output pulse can be set to align with the falling edge of OUT1/8 output reference clock by setting the DPLL{1:2}_FR_MFRSYNC_PUL_POS bit to b’1.

Alignment of Output Dividers

The output clocks are aligned with the rising edge of the input reference clock. The output clocks can be inverted by setting the OUT{1:8}_INV bit. The input-to-output delay of the output clocks to the input reference clock edge is captured in the data sheet.

Although the goal of a SYNC input is to align all output clock edge with a common edge of the input reference clock, it would be undesirable to continuously reset the output dividers. For this reason, the output dividers were designed to only be reset during an input reference clock switch. Each of the clock outputs has the ability to disable the synchronization of the output dividers; controlled via OUT{1:8}_SYNC_EN bit. The resetting of the output dividers is automatically controlled by the device; and is triggered within the first 2 seconds of a reference input switch. The alignment of the output clocks to the input reference clock is captured in the previous Figure 15 through Figure 18.

This resetting of the output dividers works for most cases, unless there are output clocks less than the frequency of the input reference clock (post-divided, if applicable). In this case, during initial acquiring of an input reference clock (i.e. coming out of FREERUN or HOLDOVER), the divider reset must be manually triggered to re-align the outputs of the lower frequency clocks. Details of this are captured in the document "Procedure to align output clocks with input Frame Pulse for 82P338xx/9xx".

Application Examples

Using SYNC input as a Frame Pulse (FP)

As a FP, the SYNC input is "framing" the input reference clock. This means that the pulse width is typically 1UI of the input reference clock. Because it is a framing pulse, the input reference clock should not be divided down internally (i.e. direct to PFD). The reason is that dividing the clock changes the period from the original reference, which was used to determine the framing pulse width.

Figure 19. FP Example – 0.5 UI Early

By default, the FP will only be used once the DPLL has locked to the reference input clock. This is controlled by the DPLL{1:2}_AUTO_EXTSYNC_EN bit when DPLL{1:2}_EXTSYNC_EN = b’1 (enabled). In a MS/SL configuration, the SLAVE device must set DPLL{1:2}_SYNC_BYPASS bit must be set to b’1 for the slave to use the SYNC input.
Using SYNC input as a Sync Pulse (SP)

As a SP, the SYNC input is identifying an edge of the input reference clock to align all clocks to. Because the SP is synchronous to the reference clock, the input clock can be divided down internally with the fractional input divider [1]. The output dividers are also aligned by the SP to the reference input edge. Although 1PPS is the most common SP, 2k/4k/8k can be used as well. In either case, the pulse width must be wide enough to support a divided down reference clock (typically in µs or ms).

Figure 20. SP Example - On Target

Since the input and output dividers are aligned to the SYNC input, it is recommended to disable DPLL{1:2}_AUTO_EXTSYNC_EN by setting to b'0 (always use SYNC input). In a MS/SL configuration, the SLAVE device must set DPLL{1:2}_SYNC_BYPASS bit must be set to b'1 for the slave to use the SYNC input.

When using the fractional input divider, it will apply a static 1UI offset to the divided down reference clock (as described in section Alignment of Fractional Input Divider). It is recommended to apply an input skew offset to the reference input to account for the 1UI static offset. Note that this skew configuration only affects the feedback/output clocks, and does not change the setup/hold times used for the input divider.

[1] The high frequency input divider (IN{8:3}_HF_DIV[1:0]) and integer input divider (IN{3:14}_PRE_DIVN_CNFG[14:0]) are not aligned by the SYNC input.
Figure 21. Example with Input Divider - 0.5UI Early, -1UI Input Skew

For questions related to device configurations, please contact IDT application support at support-sync@idt.com
### Revision History

Table 3. Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>November 10, 2016</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   * **Standard**: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   * **High Quality**: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or disaster to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.IDT.com/go/support

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.