Purpose
This application note outlines the basic guidelines to use the IDT Wafer Level Chip Scale Package (WLCSP) to ensure consistent Printed Circuit Board (PCB) assembly necessary to achieve high yield and reliability. The recommendations are proven to work under the given conditions. However, variances in the manufacturing equipment, processes and PCB designs may lead to a combination where other process parameters yield superior performance. It is also possible that a significant deviation from the recommended guidelines show inferior yield and reliability performance. Reference data is provided for these packages with respect to MSL ratings, board level thermal cycling and drop test performance.

Scope
This application note is written generically to cover typical Wafer Level Chip Scale Packages (WLCSP). It should be noted that device specific information is not provided. This document serves only as a guideline to help develop a workable solution. Actual experience and development efforts are still required to optimize the process per individual device and application requirements.

Package Description
The process of assembling WLCSP is very similar to direct chip attach method, eliminating the need of individually assembling the units in packages after dicing from a wafer. This process is essentially an extension of the chip fabrication process where the device interconnects and protections are accomplished using the traditional fab processes and equipment. The final solution is a device with an array pattern of bumps or solder balls formed on the chip with a pitch compatible with traditional PCB assembly processes. WLCSP is essentially a true Chip Scale Package (CSP) with the final package the same size as the chip. Figure 1 is an actual image of an IDT WLCSP package. It differs from other ball-grid array, leaded and laminate-based CSPs because no bond wires, leads or substrate interconnections are required.

Figure 1. Actual Image of an IDT WLCSP Package

WLCSP Configurations and Dimensions
IDT WLCSP packages range from 2x2 to 12x12 bump array, with a standard pitch of 0.40mm and a standard solder ball diameter of 268um. The physical outlines (POD) of WLCSP packages are dynamic since those depend on actual die sizes. Therefore, users of devices in these packages must exercise greater care in utilization than those in more standardized packages. Refer to Table 1 for details regarding standard solder ball arrays at 0.40mm pitch. Typical package height is 0.6mm nominal with 0.65mm being the maximum. 0.55mm max and 0.4mm max package heights are also available.

IDT ships WLCSP in tape-and-reel (T&R) format. Tape-and-reel requirements are based on the EIA-481 standard. Pin 1identifiers are present on both sides of IDT WLCSP package to help with the assembly process.
Table 1. WLCSP Package Offerings

<table>
<thead>
<tr>
<th>Solder Ball Array</th>
<th>Maximum I/O</th>
<th>Bump Pitch (mm)</th>
<th>Minimum Die Size (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 x 2</td>
<td>4</td>
<td>0.4</td>
<td>0.8mm x 0.8mm</td>
</tr>
<tr>
<td>3 x 3</td>
<td>9</td>
<td>0.4</td>
<td>1.2mm x 1.2mm</td>
</tr>
<tr>
<td>4 x 4</td>
<td>16</td>
<td>0.4</td>
<td>1.6mm x 1.6mm</td>
</tr>
<tr>
<td>5 x 5</td>
<td>25</td>
<td>0.4</td>
<td>2.0mm x 2.0mm</td>
</tr>
<tr>
<td>6 x 6</td>
<td>36</td>
<td>0.4</td>
<td>2.4mm x 2.4mm</td>
</tr>
<tr>
<td>7 x 7</td>
<td>49</td>
<td>0.4</td>
<td>2.8mm x 2.8mm</td>
</tr>
<tr>
<td>8 x 8</td>
<td>64</td>
<td>0.4</td>
<td>3.2mm x 3.2mm</td>
</tr>
<tr>
<td>9 x 9</td>
<td>81</td>
<td>0.4</td>
<td>3.6mm x 3.6mm</td>
</tr>
<tr>
<td>10 x 10</td>
<td>100</td>
<td>0.4</td>
<td>4.0mm x 4.0mm</td>
</tr>
<tr>
<td>11 x 11</td>
<td>121</td>
<td>0.4</td>
<td>4.4mm x 4.4mm</td>
</tr>
<tr>
<td>12 x 12</td>
<td>144</td>
<td>0.4</td>
<td>4.8mm x 4.8mm</td>
</tr>
</tbody>
</table>

a. Die size includes saw street.
b. Rectangular array is also available.

**WLCSP Construction**

Figure 2 below outlines a typical representation of a WLCSP package with Redistribution Layer (RDL) and Under Bump Metallization (UBM) structures. A WLCSP die has a first layer of organic dielectric (Polyimide 1), a metal redistribution layer (RDL) to re-route the signal path from the I/O to a new desired location, and a second polyimide layer (Polyimide 2) to cover the RDL metal, which in turn is patterned into the solder ball array. To prevent diffusion and enable solder wetting, an under-bump metallization (UBM) layer is deposited on the RDL. The solder ball is a lead-free alloy. Backside wafer lamination, a protective polymer film, is optional for WLCSP products. This polymer material offers both mechanical contact (i.e. SMT assembly pick & place) and UV light protection to the die backside.

**Figure 2. Cross section schematic of IDT WLCSP Package with RDL**
**PCB Design Guidelines**

For optimal electrical performance and highly reliable solder joints, the solder joint dimensions on the chip and the PCB side should be well-balanced and ideally within 5% tolerance of each other.

The PCB pads can be of either Solder Mask Defined (SMD) type or Non-Solder Mask Defined (NSMD) type. Figure 3 shows the top view of the two pad types.

**Figure 3. SMD vs. NSMD Copper Pads**

SMD pads are defined by the solder mask opening on the board. For SMD pads, the opening of the solder mask is smaller than the underlying copper pad for soldering to the associated bump. NSMD pads have solder mask opening larger than the copper pad. There are many factors influencing whether the PCB designer should use SMD or NSMD pads. Either type can successfully be used with WLCSP packages. However IDT recommends using NSMD pads. Cross-sectional view of the solder joint using the two pad types is shown in Figure 4. Also shown in Figure 5 is a cross-section of an actual recommended joint using NSMD pads.

**Figure 4. Sectional View of WLCSP Mounted on NSMD (left) and SMD (right) Pads**
Figure 5. Cross-section of a Good Quality Joint Using NSMD Pad

Key PCB design considerations for NSMD type pads
- Solder mask is recommended between all pads, with the clearance around the copper pad and solder mask of 50μm nominal to account for the registration tolerance of the solder mask.
- Limiting the thickness of the metal pad to not exceed 30μm is critical to assure a balanced joint.
- To prevent solder thieving, each NSMD copper pad should be connected by only one signal trace, with the trace width being no more than 60% the diameter of the pad and having a fillet radius at the point it meets the pad, also known as “tear dropping”. This prevents a stress riser that would otherwise occur at the pad/trace intersection.

Table 2. Design Guidelines for NSMD Pads

<table>
<thead>
<tr>
<th>Description</th>
<th>0.4mm &amp; 0.5mm pitch WLCSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder Ball Diameter</td>
<td>268um +/- 60um</td>
</tr>
<tr>
<td>PCB Pad Shape</td>
<td>Round</td>
</tr>
<tr>
<td>PCB Pad Diameter</td>
<td>205um +/- 20um</td>
</tr>
<tr>
<td>PCB Pad Surface Finish</td>
<td>OSP</td>
</tr>
<tr>
<td>PCB Pad Thickness</td>
<td>30um max</td>
</tr>
<tr>
<td>Solder Mask Opening</td>
<td>305um +/- 30um</td>
</tr>
<tr>
<td>Stencil Fabrication</td>
<td>Laser cut stainless steel with Ni plating and electropolishing; chemical etch method not recommended</td>
</tr>
<tr>
<td>Stencil Thickness</td>
<td>0.100mm to 0.125mm</td>
</tr>
<tr>
<td>Stencil Aperture</td>
<td>5° tapered, trapezoidal square 0.25 x 0.25mm (+/- 0.025mm)</td>
</tr>
</tbody>
</table>
Key PCB Design Considerations for SMD Type Pads

- It is critical to ensure good solder mask coverage and no metal pad edge is exposed.
- Ensure that the metal pad is clear of any solder mask related residue.

Table 3. Design Guidelines for SMD Pads

<table>
<thead>
<tr>
<th>Description</th>
<th>0.4mm &amp; 0.5mm pitch WLCSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Solder Ball Diameter</td>
<td>268um +/- 60um</td>
</tr>
<tr>
<td>PCB Pad Shape</td>
<td>Round</td>
</tr>
<tr>
<td>PCB Pad Diameter</td>
<td>340um +/- 35um</td>
</tr>
<tr>
<td>PCB Pad Surface Finish</td>
<td>OSP</td>
</tr>
<tr>
<td>PCB Pad Thickness</td>
<td>NA</td>
</tr>
<tr>
<td>Solder Mask Opening</td>
<td>240um +/- 25um</td>
</tr>
<tr>
<td>Stencil Fabrication</td>
<td>Laser cut stainless steel with Ni plating and electro-polishing; chemical etch method not recommended</td>
</tr>
<tr>
<td>Stencil Thickness</td>
<td>0.100mm to 0.125mm</td>
</tr>
<tr>
<td>Stencil Aperture</td>
<td>50 tapered, trapezoidal square 0.25 x 0.25mm (+/- 0.025mm)</td>
</tr>
</tbody>
</table>

Via-In-Pad Structures

Via-in-pad structures will generally be determined by the design requirements. Via-in-pad designs typically result in voids and inconsistent solder joints after reflow, leading to early failures. These voids are formed due to the entrapment of air in via barrel. The size of a typical void can be same as via diameter and up to a depth of 30% the solder ball height. If via-in-pad structures must be used, it is recommended to use filled vias. As with any PCB, the quality and experience of the vendor is very important with via-in-pad designs.

Board Material

IDT's WLCSP can be assembled on standard epoxy glass substrates. High temperature FR-4 which has smaller CTE (coefficient of thermal expansion) is preferable because it enhances package reliability as compared to standard FR-4. The actual CTE of PCB board is also affected by numerous factors such as number of metal layers in PCB, trace density, laminate material, operating environment etc. Ideally, the glass transition temperature of the substrate should be above the operating range of the intended application temperature.

Thinner boards are more flexible and result in greater reliability during thermal cycling. Moreover, they provide improved thermal fatigue life in comparison to thicker boards. Standard board thickness currently used in the industry ranges from 0.4mm to 2.3mm. The thickness is selected depending on the required robustness of the assembly.

Different bond pad surface finishes have significant effect on assembly yield and reliability. Organic Surface Preservative (OSP) is recommended as the most appropriate finish. Electroless Nickel Immersion Gold (ENIG) is a popular choice due to the higher substrate shelf-life, improved corrosion resistance and better thermal stability of solder joint. Immersion gold, immersion silver, solder on pad are also acceptable alternatives.

Stencil Design Guideline

Due to the relatively fine pitch and small terminal geometry used on WLCSP, optimizing the paste printing process is critical to ensure the reliability of solder joints. In-process inspection for paste height, percent pad coverage, and registration accuracy to solderable land pattern is highly recommended.
Stencils should be laser cut stainless steel with Nickel plating or electroformed Cobalt or Chromium hardened Nickel for repeatable solder paste deposition from ultra-small apertures required by small pitch packages. It is recommended to inspect the stencil openings for burs and other quality issues prior to use. Both square and round shaped apertures have been used successfully, however square shaped aperture openings provide more consistent paste printing and transfer efficiency when compared to round openings. Corners may be rounded to prevent clogging.

Common stencil thicknesses for WLCSP are 0.1mm and 0.125mm. Stencil aperture area ratio of >0.66 and aspect ratio >1.5, with 0.25mm x 0.25mm square openings (25 micron corner radius) is recommended for good solder paste deposition repeatability. Aperture aspect ratio is defined as the aperture opening area divided by the aperture side wall surface area. When these stencil design requirements conflict with other required SMT components in a mixed technology PCB assembly, a step-down stencil or two-print stencil process may be required.

**PCB Assembly Guidelines**

**Assembly Process Flow**

The assembly procedure for IDT WLCSP packages is compatible with industry standard surface mount procedures, as exemplified in IPC-CM-770 and IPC-A-610 class 2 standards. ESD protection should be used in all process steps. A typical WLCSP assembly process flow is shown in Figure 6 below.

**Figure 6. Typical WLCSP Assembly Process Flow**

IDT WLCSP packages do not require underfill and have been qualified without it. IDT recommends WLCSP assembly without any underfill. Use of underfill in application, if desired by the end-user, should involve careful selection of the material so as to avoid problems caused by a mismatched material choice.

Since IDT WLCSP is qualified as MSL1 at +260°C per JEDEC J-STD-020, no bake is required before assembly.

**Solder Paste Material**

Use of Type 4 (25 to 36 micron solder sphere particle size) or finer solder paste is recommended. It is also recommended that a low halide (<100ppm halides), no-Clean rosin/resin flux system be used to eliminate post-reflow assembly cleaning operations.

**Component Placement (Handling)**

The WLCSP package is relatively small in size. For better accuracy, it is recommended to use automated fine-pitch placement machines with vision alignment instead of chip-shooters to place the parts. Local fiducials are required on the board to support the vision systems.

WLCSP devices are brittle and fragile structures and hence pick-and-place systems using mechanical centering are not recommended due to the high potential for mechanical damage. Ensure that minimal pick-and-place force is used to avoid damage, with all vertical compression forces controlled and monitored. Z-height control methods are recommended over force control. IDT highly recommends the use of low-force nozzle options and compliant tip materials to further avoid any physical damage to the WLCSP device. Figure 7 below shows mechanical damage to the WLCSP device due to improper handling.
Figure 7. Mechanical Damage to WLCSP Device Due to Improper Handling

For manual handling, use only vacuum pen with compliant tip material. A sample pen type is shown in Figure 8 below.

Figure 8. Manual Handling of WLCSP Device Using a Vacuum Pen

All assemblers of WLCSP components are encouraged to conduct placement accuracy studies to provide factual local knowledge about compensations needed for this package type. IDT cannot anticipate the range of placement equipment and settings possible for package placement and therefore cannot make a generic recommendation on how to compensate for WLCSP interchangeability.

Reflow Profile

Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. The actual profile depends on several factors, including complexity or products, oven type, solder type, temperature difference across the PCB, oven and thermocouple tolerances, etc. All IDT’s WLCSP devices are qualified at Moisture Sensitivity Level 1 at 260°C. The maximum temperature at the component body should not exceed this level.

A typical reflow profile for lead-free paste is shown in Figure 9, based on IPC/JEDEC J-STD-020D. The furnace should have a nitrogen purge, with the oxygen content of the furnace monitored and kept below 100 ppm.
Actual reflow temperature settings need to be determined by the end-user, based on the size of thermal load.

**Pack and Ship**

To prevent damage to the WLCSP component, care must be taken in handling, packing, and shipping WLCSP assemblies, especially when the WLCSP is mounted without epoxy encapsulation. The assembly site's packing specifications for PCB mounted with WLCSP must be reviewed and optimized.

**WLCSP Reliability**

WLCSP reliability can be divided into two categories namely, board level reliability (BLR) and component level reliability. The board level reliability is usually characterized by determining the solder joint life. The reliability results in this section utilized the board layout guidelines discussed before.

**BLR Test Structure Description**

The WLCSP package has a relatively shorter solder joint life compared to leaded or laminate substrate based packages. The solder joint reliability has been tested for reliability by IDT to understand solder joint life and failure mechanism. Samples of WLCSP in daisy chain format were used to study the solder joint reliability. BGA pairs were routed together in the WLCSP RDL layer, with a complementary pattern designed on the test PCB to provide one electrical circuit (net) through the package when the package is attached to the test PCB. Test points on the PCB exterior to the package allow one to isolate which pair of solder joints failed during testing.

**Temperature Cycling Reliability Results**

Assembled PCBs can be temperature cycled at a variety of temperature ranges. The most common test condition for small devices is JEDEC Condition 'G' (-40°C to 125°C), with equally split ramp-up, hot-zone dwell, ramp-down and cold-zone dwell times for a typical frequency of one cycle per hour. This test refers to JESD22-A104D, condition G.

Board level temperature cycle was performed with the following test conditions:

- Temperature range: -40 °C to +125 °C
- Duration of exposure: 15 minutes exposure in each temperature extreme
- Temperature ramp: 15 minutes
- Cycle time: 60 minutes
The test setup utilized has the capability of continuously monitoring the resistance through a daisy chain package and its complementary test PCB. Failure is defined as 20% increase in resistance over the initial resistance of the daisy chain. Daisy chain nets are tested (time zero testing) prior to temperature cycling. Most nets start with initial resistance of around 1Ω.

The solder joint reliability performance results during board level temperature cycle are shown in Table 4.

**Table 4. Board-level Temperature Cycle Results for IDT WLCSP**

<table>
<thead>
<tr>
<th>Array Size</th>
<th>Ball Pitch</th>
<th>Test Condition</th>
<th>Criteria</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>10x10</td>
<td>0.4mm</td>
<td>-40/125°C with 15 min dwell, 1 cycle/hour</td>
<td>5% failure &gt; 500 cycles, S/S =60</td>
<td>Pass</td>
</tr>
<tr>
<td>12x12</td>
<td>0.4mm</td>
<td>-40/125°C with 15 min dwell, 1 cycle/hour</td>
<td>5% failure &gt; 500 cycles, S/S =60</td>
<td>Pass</td>
</tr>
</tbody>
</table>

**Mechanical Drop Test Reliability Results**

WLCSP parts were tested per JEDEC's JESD22-B111 Drop Test Specification. The drop test set-up, board layout, fixtures, and criteria are all based on the JESD22-B111. All drops are carried out in the Z direction (package down).

Drop test was performed with the following test conditions:

- Pulse shape: Half-sine waveform
- Impact acceleration: 1500 G (+/- 20%)  
- Pulse duration: 0.5 ms (+/- 30%)  
- Velocity change: 467 cm/s (+/- 10%)

The resistance at time zero and still state after the drop are recorded. Resistance data was collected in-situ throughout the dropping process, with maximum resistance data recorded during the drop. An event is defined as resistance greater than 1,000 ohms lasting for 1 microsecond or longer. Failure is defined as three or more events during five subsequent drops.

The solder joint reliability performance results during board level temperature cycle are shown in Table 5.

**Table 5. Board-level Drop Test Results for IDT WLCSP**

<table>
<thead>
<tr>
<th>Array Size</th>
<th>Ball Pitch</th>
<th>Test Condition</th>
<th>Criteria</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>10x10</td>
<td>0.4mm</td>
<td>1500G, 0.5ms half sine</td>
<td>10% failure &gt; 150 drops, S/S =60</td>
<td>Pass</td>
</tr>
<tr>
<td>12x12</td>
<td>0.4mm</td>
<td>1500G, 0.5ms half sine</td>
<td>10% failure &gt; 150 drops, S/S =60</td>
<td>Pass</td>
</tr>
</tbody>
</table>

**Cyclic Bending Test Reliability Results**

WLCSP parts were tested per JEDEC's JESD22-B113 Cyclic Bend Test Specification.

Cyclic bend test was performed with the following test conditions:

- Span for support Anvils: 110mm  
- Span for load Anvils: 75 mm  
- Temperature ramp: 15 minutes  
- Load profile: Sinusoidal  
- Cycle frequency: 1 Hz
An event is defined as resistance greater than 1,000 ohms lasting for 1 microsecond or longer. Failure is defined as the first event of intermittent discontinuity with resistance peak greater than the threshold value followed by at least 9 additional confirmation events within 10% of the cycles to first event.

The solder joint reliability performance results during board level temperature cycle are shown in Table 6.

### Table 6. Board-level Cyclic Bending Test Results for IDT WLCSP

<table>
<thead>
<tr>
<th>Array Size</th>
<th>Ball Pitch</th>
<th>Test Condition</th>
<th>Criteria</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>8x8</td>
<td>0.4mm</td>
<td>2mm, 1Hz</td>
<td>200k cycles</td>
<td>Pass</td>
</tr>
</tbody>
</table>

### Component Level Reliability Results

Typical component level package stresses were also performed on IDT WLCSP. Table 7 lists all component level package stresses, passing criteria and results.

### Table 7. Component-level Reliability Results for IDT WLCSP

<table>
<thead>
<tr>
<th>Test Items</th>
<th>Stress Condition</th>
<th>Method</th>
<th># of Lots</th>
<th>Duration</th>
<th>Qual Criteria per lot (#fails/SS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-Conditioning</td>
<td>Bake: 24 hrs, 125°C, MSL 1</td>
<td>J-STD-020</td>
<td>3</td>
<td>168 hrs</td>
<td>0/25</td>
</tr>
<tr>
<td>Temperature Cycle</td>
<td>-55°C to 125°C</td>
<td>JESD22-A104</td>
<td>3</td>
<td>700 cyc</td>
<td>0/77</td>
</tr>
<tr>
<td>Biased HAST</td>
<td>130°C / 85% R.H., Vcc oper max</td>
<td>JESD22-A110</td>
<td>3</td>
<td>96 hrs</td>
<td>0/77</td>
</tr>
<tr>
<td>UnBiased HAST</td>
<td>130°C / 85% R.H.</td>
<td>JESD22-A118</td>
<td>3</td>
<td>96 hrs</td>
<td>0/77</td>
</tr>
<tr>
<td>High Temperature Storage</td>
<td>150°C</td>
<td>JESD22-A103</td>
<td>3</td>
<td>1000 hrs</td>
<td>0/25</td>
</tr>
</tbody>
</table>

a. Pre-condition will be performed prior to Temperature cycle, Biased HAST, and UnBiased HAST.

### WLCSP Rework

Rework is not recommended. Should rework be necessary, procedures are identical to BGA. Rework profile should duplicate original reflow profile used in assembly. Rework system should include localized convection heating, bottom side heating and a pick-and-place device. System should also provide thermal profile capability.
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

- "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

- "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or disaster to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations and other laws and regulations administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters
TOYOSU FORESIA, 3-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.