



# Converting Designs Using the LXT381 to the IDT82V2058

Application Note, January 2002 (Ver 1.0) File No. IDT82V2058AN\_02

## 1. General description

The IDT82V2058 is a full featured octal E1 line interface unit that can function in a manner similar to Intel's (previously Level One) LXT381, octal E1 analog front end. Converting designs using the LXT381 to the IDT82V2058 is a straightforward process as long as care is taken regarding the points described below. The conversion process involves minimal hardware changes due to the fact that both devices offer a compatible pin arrangement. Functionally, the IDT82V2058 supports the same basic operation of the LXT381 AFE and boasts a number of additional features and control modes. The primary purpose of this application note is to describe the differences between the LXT381 and the IDT82V2058 and highlight the hardware considerations that come into play when converting an existing LXT381 design.

## 2. Clocks

There are some differences between the mode selection executed by clock pins on the LXT381 and IDT82V2048. The LXT381 does not offer a jitter attenuator and thus does not require an MCLK. Instead, this pin is called RPD (Receiver Power Down) and is supplied with a logic high or low. The IDT82V2058 offers a jitter attenuator and thus accepts a MCLK signal, however, if MCLK is not provided (as LXT381 designs will not), the device will use TCLK1 as the MCLK signal. As a result, similar operation can be achieved without an MCLK signal but, in this case, care must be taken to always supply TCLK1 for normal operation. Another distinction is that the IDT82V2058 does not offer RZ mode in the transmit path.

RPD/MCLK	TCLKn	Operation Mode of Transmit Path	
		LXT381	IDT82V2058
Low	Clocked	Receive Power Down (All) Transmit NRZ	Receive Power Down (All) Transmit NRZ
Low	Low	Receive Power Down (All) Transmit Power Down (channel n)	Receive Power Down (All) Transmit Power Down (channel n) <sup>1</sup>
Low	High	Receive Power Down (All) Transmit RZ	Receive Power Down (All) Transmit All Ones (channel n) <sup>1</sup>
High	Clocked	Receive Data Recovery Transmit NRZ	Receive Data Recovery Transmit NRZ
High	Low	Receive Data Recovery Transmit Power Down (channel n)	Receive Data Recovery Transmit Power Down (channel n) <sup>1</sup>
High	High	Receive Data Recovery Transmit RZ	Receive Data Recovery Transmit All Ones (channel n) <sup>1</sup>

<sup>1</sup> – If TCLK1 is not available (H/L) all transmitters will be in high impedance state

Table –1 RPD/MCLK and TCLK

### 3. Loopback Selection

In hardware mode, the status of LPn pin decides the loop back configuration of the corresponding port. For "No Loop back" setting, the LXT381 and IDT82V2058 are different.

	<b>LXT381</b>	<b>IDT82V2058</b>
No Loop back on Port n	LPn = Not connected	LPn = 0.5 * VDDIO

Table-2 Loopback Selection

### 4. External Components

There are some changes in external components that must be considered for the balance networks when converting designs from the LXT381 to the 82V2058. The transmit impedance on the line side and the receive transformer recommendations between the IDT82V2058 and LXT381 are slightly different. These differences are summarized in Figure-1 and Table-3 below.

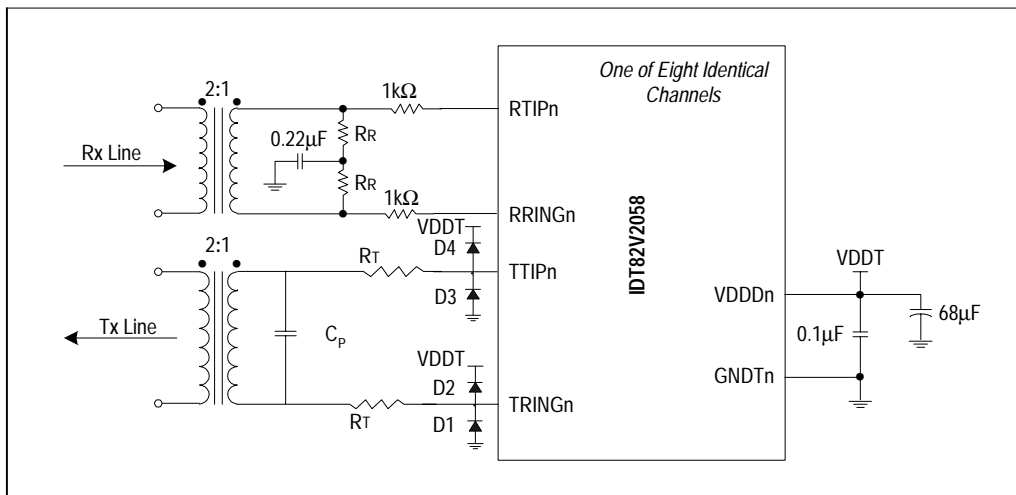


Figure-1 82V2058 Line Circuitry

Component	LXT381		IDT82V2058	
	75Ω Coax	120Ω Twisted Pair	75Ω Coax	120Ω Twisted Pair
R <sub>T</sub>	11Ω +/- 1%	11Ω +/- 1%	9.5Ω +/- 1%	9.5Ω +/- 1%
C <sub>T</sub>	560 pF typ.	560 pF typ.	2200 pF typ.	2200 pF typ.
R <sub>R</sub>	37.5Ω +/- 1%	60Ω +/- 1%	9.31Ω +/- 1%	15Ω +/- 1%
Rx Transformer Turns Ratio	1:1	1:1	1:2	1:2

Table-3 Component Value Differences