This application note describes the power dissipation and junction temperature calculation for LVCMOS clock buffers with series termination and parallel termination. ICS8701 is used as an example to describe the calculations. A similar approach can be used for calculating the power dissipation and junction temperature for other clock buffers with LVCMOS drivers.

**LVCMOS Power Dissipation for Serial Termination**

The total power dissipation $P_{d\_total}$ is composed of Static Power Dissipation $P_{d\_static}$ and Dynamic Power Dissipation $P_{d\_dynamic}$.

$$P_{d\_total} = P_{d\_static} + P_{d\_dynamic}$$

Where

- $P_{d\_static}$ is static power dissipation under DC conditions
- $P_{d\_dynamic}$ is dynamic power dissipation due to clocking.

**Static Power Dissipation**

Static power dissipation is the power dissipation when the part is not switching. There are two sections in the ICS8701 circuitry, core and output driver. The core circuitry draws current $I_{DDI}$ from the $V_{DD}$ supply. The output driver circuitry draws current $I_{DDO}$ from the $V_{DDO}$ supply.

The static power dissipation $P_{d\_static}$ is composed of Core static power dissipation, $P_{d\_core\_static}$ and output driver static power dissipation, $P_{d\_drive\_static}$

$$P_{d\_static} = P_{d\_core\_static} + P_{d\_drive\_static}$$

Where

- $P_{d\_core\_static} = I_{DDI} \times V_{DD}$
- $P_{d\_drive\_static} = I_{DDO} \times V_{DDO}$

Since the supply current $I_{DD}$ data provided in the data sheet is the sum of $I_{DDI}$ and $I_{DDO}$

$$I_{DD} = I_{DDI} + I_{DDO}$$

For $V_{DD} = V_{DDO}$, the total static power can be calculated as

$$P_{d\_static} = V_{DD} \times I_{DD}$$

**Dynamic Power Dissipation**

Dynamic power dissipation $P_{d\_dynamic}$ is composed of $P_{d\_drive\_dynamic}$ and $P_{d\_Rout}$. For ICS8701, frequency has a very small effect on the core supply current $I_{DDI}$. To simplify the calculation, using the worst case $I_{DDI}$ in the static power dissipation covers the core dynamic power dissipation. The dynamic core power dissipation is not required to be included in this section. Serial termination scheme is used as an example to calculate the dynamic power dissipation.
\[ P_{d\_dynamic} = P_{d\_drive\_dynamic} + P_{d\_Rout} \]

\[ P_{d\_output\_dynamic} \] is the power dissipation within the output driver circuitry and can be calculated as

\[ P_{d\_drive\_dynamic} = C_{pd} \times (V_{DD0})^2 \times F \times N_{out} \]

Where
- \( C_{pd} \) is Power dissipation capacitor per output
- \( F \) is driver clock frequency
- \( N_{out} \) is total number of outputs enable. For 8701, \( N_{out} = 20 \)
- \( V_{DD0} \) is output power supply voltage.

\( P_{d\_Rout} \) is power dissipation on the output impedance due to loading condition. For series termination as shown in Figure 1, the output current will hold the peak current for a short period of time. The duration depends on the time delay of the transmission line \( T_d \).

\[
P_{d\_Rout} = \left[ I_{\_load\_peak} \right]^2 \times R_o \times 2 \times (2 \times T_d / T) \times N_{load}
\]

**Figure 1**  LVCMOS output Series Termination

Figure 2 shows the timing diagram for the load current, related voltages on each point, and the power dissipation on \( R_o \). For \( T_d < \frac{1}{4} T \), (where \( T \) is clock period), during each clock period, the load current will hold the peak load current \( I_{\_load\_peak} \) for a duration of \( 2T_d \) for PMOS ON, NMOS OFF and additional \( 2T_d \) for PMOS OFF and NMOS ON. Calculating the power dissipation on the clock buffer chip due to the load current should not include the power dissipation on the loading. This element should only include power dissipation on the output resistor \( R_o \).

\[ P_{d\_Rout} = \left[ I_{\_load\_peak} \right]^2 \times R_o \times 2 \times (2 \times T_d / T) \times N_{load} \]
HiPerClockSTM Application Note

Power Dissipation
For High Speed LVCMOS Buffer
Integrated
Circuit
Systems, Inc.

\[
\begin{align*}
I_{\text{load \_peak}} &= \frac{V_{\text{DDO}}}{2\cdot Z_O} \\
P_{d\text{\_peak}} &= (I_{\text{load \_peak}})^2 \cdot R_O \\
\end{align*}
\]

For series termination, \( R_O + R_S = Z_O \), the peak load current is

\[
I_{\text{load \_peak}} = \frac{V_{\text{DDO}}}{2\cdot Z_O}
\]

The peak power dissipation on \( R_O \) is

\[
P_{d\text{\_peak}} = (I_{\text{load \_peak}})^2 \cdot R_O
\]

The peak power \( P_{d\text{\_peak}} \) will hold for \( 4\cdot T_d \) per clock period. Therefore the total average power dissipation for all \( N_{\text{load}} \) is

\[
P_{d\text{\_Rout}} = \frac{V_{\text{DDO}}^2}{(2\cdot Z_O)^2} \cdot R_O \cdot \frac{4\cdot T_d}{T} \cdot N_{\text{load}}
\]

Figure 2  Time Diagram for Voltage, Load Current and Power Dissipation on Rout

For series termination, \( R_O + R_S = Z_O \), the peak load current is

\[
I_{\text{load \_peak}} = \frac{V_{\text{DDO}}}{2\cdot Z_O}
\]

The peak power dissipation on \( R_O \) is

\[
P_{d\text{\_peak}} = (I_{\text{load \_peak}})^2 \cdot R_O
\]

The peak power \( P_{d\text{\_peak}} \) will hold for \( 4\cdot T_d \) per clock period. Therefore the total average power dissipation for all \( N_{\text{load}} \) is

\[
P_{d\text{\_Rout}} = \frac{V_{\text{DDO}}^2}{(2\cdot Z_O)^2} \cdot R_O \cdot \frac{4\cdot T_d}{T} \cdot N_{\text{load}}
\]
Where

- \( T_d \) is the time delay for the transmission line
- \( T \) is clock period
- \( Z_O \) is characteristic impedance of the transmission line.
- \( N_{\text{load}} \) is number of output being loaded with series termination

### Summary

### Power Dissipation

To calculate Power Dissipation for series terminations

\[
P_{\text{total}} = P_{\text{static}} + P_{\text{dynamic}}
\]

\[
= P_{\text{core\_static}} + P_{\text{drive\_static}} + P_{\text{drive\_dynamic}} + P_{\text{Rout}}
\]

Where,

\[
P_{\text{core\_static}} = I_{DD} \cdot V_{DD}
\]

\[
P_{\text{drive\_static}} = I_{DO} \cdot V_{DO}
\]

\[
P_{\text{drive\_dynamic}} = C_{pd} \cdot F \cdot (V_{DO})^2 \cdot N_{out}
\]

For transmission line delay \( T_d \) less than \( \frac{1}{4} T \), clock time period

\[
P_{\text{Rout}} = \frac{V_{DO}}{(2 \cdot Z_O)^2} \cdot R_O \cdot 2 \cdot (2 \cdot T_d/T) \cdot N_{load}
\]

### Junction Temperature

Junction temperature, \( T_j \), is the temperature at the junction of the bond wire and bond pads and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockSTM devices is 125°C

\[
T_j = T_A + \theta_{AJ} \cdot P_{\text{Total}}
\]

Where,

- \( T_A \) is ambient temperature
- \( \theta_{AJ} \) is thermo resistance

### Example:

For ICS8701 with series termination,

All outputs enabled and loaded with one to one series termination.

- \( Z_O = 50 \) Ohm, \( T_d = 1 \) nsec,
- Clock frequency, \( F = 100 \) MHz (or time period, \( T = 10 \) nsec)

\[
R_S = Z_O - R_O = 50 \text{ Ohm} - 7 \text{ Ohm} = 43 \text{ Ohm}
\]

\[
V_{DD\text{max}} = V_{DDO\text{max}} = 3.465 \text{V}
\]

\[
V_{DO\text{max}} = 2 \cdot Z_O \cdot R_O \cdot 2 \cdot (2 \cdot T_d/T) \cdot N_{load}
\]

\[
Junction Temperature
\]

\[
T_j = T_A + \theta_{AJ} \cdot P_{\text{Total}}
\]

Where,

- \( T_A \) is ambient temperature
- \( \theta_{AJ} \) is thermo resistance

### Example:

For ICS8701 with series termination,

All outputs enabled and loaded with one to one series termination.

- \( Z_O = 50 \) Ohm, \( T_d = 1 \) nsec,
- Clock frequency, \( F = 100 \) MHz (or time period, \( T = 10 \) nsec)

\[
R_S = Z_O - R_O = 50 \text{ Ohm} - 7 \text{ Ohm} = 43 \text{ Ohm}
\]

\[
V_{DD\text{max}} = V_{DDO\text{max}} = 3.465 \text{V}
\]
To calculated maximum static power dissipation, the power supply current $I_{DD}$ given in the data sheet is combination of core power current $I_{DDI}$ and driver power current $I_{DDO}$.

$$P_{\text{core\_static\_max}} = V_{DD\text{max}} \times I_{DD\text{max}}$$

$$= 3.465V \times 95mA$$

$$= 329.2mW$$

The core static power and the driver static power can be calculated separately using $I_{DDI}$ and $I_{DDO}$. The $I_{DD\text{max}}$ current can be split to $I_{DDI\text{max}} = 50mA$, $I_{DDO\text{max}} = 45mA$.

$$P_{\text{core\_static\_max}} = I_{DDI\text{max}} \times V_{DD\text{max}} = 50mA \times 3.465V = 173.3mW$$

$$P_{\text{drive\_static\_max}} = I_{DDO\text{max}} \times V_{DDO\text{max}} = 45mA \times 3.465V = 155.9mW$$

$$P_{\text{static}} = P_{\text{core\_static\_max}} + P_{\text{drive\_static\_max}} = 329.2mW$$

**Dynamic power dissipation**

$$C_{pd\text{\_max}} = 15pF$$

$$Pd_{\text{dynamic\_max}} = C_{pd\text{\_max}} \times F_{clk} \times (V_{DDO\text{\_max}})^2 \times N_{\text{out}}$$

$$= 15pF \times 100MHz \times (3.465V)^2 \times 20$$

$$= 360mW$$

$$Pd_{Rout} = \frac{[V_{DDO}/(2 \times Z_0)]^2 \times R_0 \times 2 \times (2 \times Td/T) \times N_{\text{load}}}{7 \times 2 \times (2 \times 1nsec/10nsec) \times 20}$$

$$= 67.2mW$$

$$Pd_{\text{total}} = 756.4mW$$

**Junction Temperature**

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{AJ}$ must be used. Assuming a moderate airflow of 200 linear feet per minute and a multi-layer board, the appropriate value for ICS8701 is $42.1^\circ C/W$ shown in the data sheet. The $T_j$ for an ambient temperature of $T_A = 70^\circ C$ for this example is

$$T_j = T_A + P_{\text{Total}} \times \theta_{AJ}$$

$$= 70^\circ C + 0.756 W \times 42.1^\circ C/W$$

$$= 101.8^\circ C$$

$T_j$ should be kept below $125^\circ C$.

Figure 3 and Figure 4 show charts of the power dissipation and junction temperature for ICS8701 under the following environment:

Transmission line delay $T_d = 1ns$

$V_{DD} = 3.465V$

$V_{DDO} = 3.465V$

$Z_0 = 50\ Ohm$

$R_0 = 43\ Ohm$
Power Dissipation vs Frequency

![Power Dissipation vs Frequency Graph]

Figure 3  ICS8701 Power Dissipation for Series Termination vs Clock Frequency

Junction Temperature vs Frequency

![Junction Temperature vs Frequency Graph]

Figure 4  Junction Temperature vs Clock Frequency
LVCMOS Power Dissipation for Parallel Termination

Figure 5 shows a parallel termination that configure for characterization. In actual application, the Figure 6 is an equivalent termination of the Figure 5. Both circuit and have equal result of power dissipation on the buffer. This section, Figure 5 is used for calculation.

![Figure 5 LVCMOS Driver Standard Parallel Termination](image)

To calculate Power Dissipation for parallel terminations

\[
P_{d\_total} = P_{d\_static} + P_{d\_dynamic} = P_{d\_core\_static} + P_{d\_drive\_static} + P_{d\_drive\_dynamic} + P_{d\_Rout}
\]

The \( P_{d\_core\_static}, P_{d\_drive\_static} \) and \( P_{d\_drive\_dynamic} \) are same as the results obtained from serial termination.
**Pd_Rout** is power dissipation on the output impedance due to loading condition. For parallel matched load termination with characteristic impedance \( Z_O \), the driver “sees” the loading impedance of \( Z_O \). The power **Pd_Rout** dissipates at PMOS when the output is logic high, and the power dissipated at NMOS when the output is logic low.

\[
Pd_Rout = \left(\frac{V_{DDO}}{2}/(Rout+Z_O)\right)^2 \times R_O \times N_load
\]

Where

- \( R_O \) is output impedance the LVCMOS driver.
- \( Z_O \) is characteristic impedance of the transmission line.
- \( N_load \) is number of output being loaded with series termination

To calculate **Pd_Rout** for Parallel termination

\[
Pd_Rout = \left(\frac{3.465V}{2}/(7 \text{ Ohm} + 50 \text{ Ohm})\right)^2 \times 7 \times 20
\]

= 129.3 mW

For frequency \( F=100\text{MHz} \), the total power dissipation is

\[
Pd_{total} = Pd_{static} + Pd_{dymanic} + Pd_{out}
\]

= 329.2 mW + 360 mW + 129.3 mW

= 818.5 mW

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \( \theta_{AJ} \) must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value for ICS8701 is 42.1 °C/W shown in the data sheet. The \( T_j \) for an ambient temperature of \( T_A = 70 \) °C for this example is

\[
T_j = T_A + P_{Total} \times \theta_{AJ}
\]

= 70 °C + 0.819 W * 42.1 °C/W

= 104.4 °C

\( T_j \) should be kept below 125 °C.

Figure 7 and Figure 8 show charts of the power dissipation and junction temperature for ICS8701 under the following environment:

- \( V_{DD} = 3.465V \)
- \( V_{DDO} = 3.465V \)
- \( Z_O = 50 \text{ Ohm} \)
- \( R1 = 50 \text{ Ohm} \)
Power Dissipation vs Frequency

Figure 5  ICS8701 Power Dissipation for Parallel Termination vs Clock Frequency

Junction Temperature vs Frequency

Figure 6 Junction Temperature for Parallel Termination vs Clock Frequency

Written By: Ming Lim
Any comments, please send e-mail to ming@icst.com
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depend on the product's quality grade, as indicated below.

   - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations determined and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.