PCB-Design for Improved EMC

Guideline for Applications with Renesas Microcontroller

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1 INTRODUCTION

1.1 OVERVIEW

This application note is intended for hardware and/or PCB designers with a basic knowledge on PCB design for improved EMC. Basically, the background of most design rules is explained, but a detailed explanation would have overloaded the structure of an application note. There is plenty of literature on the market treating system design for EMC, shielding, cabling etc. Therefore, these aspects of EMC are only striven with this document. This application note targets on detailed aspects of PCB design in the vicinity of Renesas microcontroller.

Today with increasing tendency most automotive, consumer and industrial applications include typically one or more microcontroller. Often several electronic modules build an application system and of course several applications and/or systems may be operating vicinal. Due to the increasing number of electronic applications their density in any given environment is increasing. Therefore, - as shown by curve 1 in Figure 1-1 - the environmental electromagnetic noise observed over long time at a given place, rises. Functionality of electronic equipment will not be affected as long as at any given point in time its immunity is higher than the environmental electromagnetic noise. None the less - as shown by curve 2 in Figure 1-1 - in modern systems, for example operating at higher frequencies and also having (due to lower power operation) lower switching thresholds, the noise immunity level is decreasing.

![Figure 1-1](image-url)

Long time environmental noise development

It is obvious that crossing point P in Figure 1-1 would cause the whole electronic market to break down. Therefore, it is essential for the electronic market to apply measures to improve the electromagnetic compatibility (EMC) of electronic systems and thereby continually pushing the point P towards infinity on time line.
## 1.2 List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Explanation</th>
</tr>
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<tbody>
<tr>
<td>A</td>
<td>Amplitude</td>
</tr>
<tr>
<td>A_{pp}</td>
<td>Amplitude, peak-to-peak</td>
</tr>
<tr>
<td>A_{RMS}</td>
<td>Amplitude, root-mean-square</td>
</tr>
<tr>
<td>C</td>
<td>capacity</td>
</tr>
<tr>
<td>c</td>
<td>Speed of light (299792*10^3 m/s)</td>
</tr>
<tr>
<td>E</td>
<td>Amplitude of E-field</td>
</tr>
<tr>
<td>f</td>
<td>Frequency</td>
</tr>
<tr>
<td>f_c</td>
<td>Corner Frequency</td>
</tr>
<tr>
<td>f_{noise}</td>
<td>Noise Frequency, resulting from rising and falling edges</td>
</tr>
<tr>
<td>I</td>
<td>Current</td>
</tr>
<tr>
<td>I_{surge}</td>
<td>Pulse current</td>
</tr>
<tr>
<td>I_{average}</td>
<td>Average current</td>
</tr>
<tr>
<td>I</td>
<td>Length, e.g. of a wire</td>
</tr>
<tr>
<td>Q</td>
<td>Electric charge</td>
</tr>
<tr>
<td>r</td>
<td>Distance, e.g. from a noise source</td>
</tr>
<tr>
<td>S</td>
<td>Space</td>
</tr>
<tr>
<td>t_f</td>
<td>Fall time</td>
</tr>
<tr>
<td>t_r</td>
<td>Rise time</td>
</tr>
<tr>
<td>U</td>
<td>Voltage</td>
</tr>
<tr>
<td>V_{SS}</td>
<td>Ground potential</td>
</tr>
<tr>
<td>V_{DD}</td>
<td>Power supply</td>
</tr>
<tr>
<td>Z_0</td>
<td>Wave impedance in far-field, constant of 377Ohm</td>
</tr>
<tr>
<td>\lambda</td>
<td>Wavelength</td>
</tr>
<tr>
<td>\varepsilon_r</td>
<td>Permittivity</td>
</tr>
<tr>
<td>\mu_r</td>
<td>Permeability</td>
</tr>
<tr>
<td>\omega</td>
<td>Equals 2*\pi*f</td>
</tr>
</tbody>
</table>
2 BACKGROUND

Electromagnetic Compatibility (EMC) is the generic term for two similar issues just viewed from opposite direction. Electromagnetic Emission (EME) describes the effects when the device under Test (DUT) is the source of the noise while Electromagnetic Susceptibility (EMS) describes the effects when the DUT is the victim of the noise. As per the experience in Renesas Electronics Europe GmbH (hereinafter called REE) the main requirement on EMC related customer support is on EME issues. Therefore, the descriptions in this application note mainly utilize the EME-view. Nevertheless, by just viewing from opposite direction, most measures described here are applicable for EMS as well.

2.1 DIRECT SEMICONDUCTOR FAR FIELD EMISSION

Emission may occur either radiated or conductive, the latter as noise-voltage or noise current. It is common understanding that semiconductor devices such as microcontroller are sources of EME. It is also well known that the nearer to the noise source the cheaper EME countermeasures are. As most normative radiated EME measurements are defined for the far field \((r > \lambda)\) this application note shall start with a view onto the direct emission of a semiconductor device into far field.

Any current in a wire causes a far field emission. In order to get an idea about the maximum expectable semiconductor emission level the worst case emission of a straight wire (Hertz dipole) and a current loop with extreme parameters shall be calculated:

2.1.1 Straight wire (Hertz dipole)

In free space (no conductive material around) according to [1] the maximum E-field ‘E’ measured at a distance ‘r’ caused by a current ‘i’ with wavelength ‘\(\lambda\)’ flowing in a wire of length ‘l’ can be calculated as follows:

\[
E = \frac{(Z_0 \cdot i \cdot l)}{(2 \cdot r \cdot \lambda)} \quad \text{with} \quad \lambda = \frac{c}{f},
\]

\(c\) Speed of light

\(f\) Frequency

In PCBs the wavelength must be adapted by the material constants \(\varepsilon_r\) and \(\mu_r\).

\[
E = \frac{(Z_0 \cdot i \cdot l)}{(2 \cdot r \cdot \lambda)} \quad \text{with} \quad \lambda = \frac{c}{\sqrt{(\mu_r \cdot \varepsilon_r) \cdot f}},
\]

\(\mu_r\) Permeability (about 1 for FR4)

\(\varepsilon_r\) Permittivity (about 4.8 for FR4)
Chapter 2 Background

Example:

Measurements according to IEC61967-4 show a typical device VSS-current at for example 100 MHz

\( \lambda = 1.37 \text{m} \) of about 20 dB\( \mu \text{A} \) (10 \( \mu \text{A} \)). Assumed this current was caused by a single wire signal of 10 mm length. The return current shall flow far away (no compensation in far-field) the E-field at a distance of 10 m. This adds up to:

\[
E = \frac{377 \Omega \times 10 \mu A \times 0.01 \text{m}}{(2 \times 10 \text{m} \times 1.37 \text{m})} \approx 1.38 \frac{\mu V}{m} \approx 2.8 \frac{dB\mu V}{m}
\]

As for this approximation extreme assumptions were used the actual direct device emission should be much lower than 2.8\( dB\mu V/m \). Compared to common emission limits obviously the direct device emission from on-chip wiring can be neglected.

2.1.2 Current loop

According to [1] maximum E-field emission of a current ‘\( i \)’ with material wavelength ‘\( \lambda \)’ flowing in a loop area space ‘\( S \)’ and measured in a distance ‘\( r \)’ can be calculated as follows:

\[
E = \frac{Z_0 \times \pi \times i \times S}{r \times \lambda^2}
\]

Example:

Assumed a current of 100 \( \mu \text{A} \) (40 dB\( \mu \text{A} \)) at 100 MHz (\( \lambda = 1.37 \text{m} \)) flows in a loop area of 1 \( \text{mm}^2 \). Measured at a distance of 10 m the resulting E-field is:

\[
E = \frac{377 \Omega \times 3.14 \times 100 \mu A \times 10^{-6} \text{m}^2}{(10 \text{m} \times (1.37 \text{m})^2)} \approx 6.3 \frac{nV}{m} \approx -44.01 \frac{dB\mu V}{m}
\]

Again obviously the direct device emission from on-chip loop currents such as power supplies etc. can be neglected, especially as again the calculation is based on extreme assumptions.
2.2 **NEAR FIELD EMISSION**

Generally, the transition from near field to far field is related to the wavelength of the signal. In [1] the \( r \leq 0.8\lambda \) area with is defined as near field, \( r \geq 1.2\lambda \) while the area with is defined as far field with a transition area in-between. Generally, structures leading RF-power shall be kept small enough so that their contribution to the far-field emission is low. Even though, near-field emission may stimulate appropriate antenna structures nearby and by means of that remarkably contribute to the far-field emission. These system effects are not described here as this application note targets on detailed aspects of PCB design in the vicinity of Renesas microcontroller.
2.3 SIGNAL CLASSIFICATION

2.3.1 Narrow band noise and wide band noise

According to Fourier’s theory any signal can be represented by a sum of sine- and cosine-oscillations.

(1) A periodical non-sinusoidal signal, such as a clock, strobe etc. consists only of its base frequency portion and its integer multiples (harmonics). The so-called narrow band noise spectrum shows only portions at discrete frequencies while in between showing the environmental noise.

(2) A non-periodical signal, such as a data-stream, consists of portions of all frequencies. This is called wide band noise.

(3) Typical spectra measurements of Renesas microcontroller include a combination of both noise types as shown in the example.

Figure 2-1: Narrow band noise and wide band noise

Remark: In the Figure 2-1, the wide band noise dominates the lower frequency range of the diagram; the narrow band noise dominates the upper frequency range of the diagram.
2.3.2 Power consumption of clocked CMOS circuits

Power consumption of CMOS circuits is mainly related to the switching frequency of the circuit. Even if a circuit additionally consumes DC-power this is not relevant for EMC. The measurement in Figure 2-2 shows the power consumption of a CMOS circuit once operated at 2 MHz (red) and once at 8 MHz (blue). Obviously, roughly four times the frequency causes four times (or +12 dB) power consumption.

Figure 2-2: CMOS power consumption versus frequency
2.3.3 Spectra of rectangular and trapezoidal signals

According to Fourier, the AC-spectrum of a rectangular signal with 50% duty cycle is composed of the base frequency and its harmonics as per the following formula [3]:

$$\text{Signal} = A \sum_{n=1}^{\infty} \frac{\sin(n \omega t)}{n}$$

with $n = 1, 3, 5, \ldots$

Obviously, the amplitude diminishes by $1/n$ or $-20$ dB per decade.

For comparison with measurements the peak-to-peak Amplitude has to be corrected to root-mean-square (RMS) as this is typically measured by a spectrum analyzer etc.:

$$A_{RMS} = A_{pp} \frac{1}{2\sqrt{2}}$$

Fortunately, rectangular signals are only a limited view assuming 0 ns rise- and fall-time. Based on the assumption of equal rise- and fall-time a spectrum falls by $-20$ dB per decade up to a specific corner frequency. Above this frequency the spectrum falls with $-40$ dB per decade with a transition area in-between. The corner frequency [4] is given by:

$$f_c = \frac{1}{\pi t_R} = \frac{1}{\pi t_f}$$

**Figure 2-3:** Spectrum of a digital signal
**Example:** Emission strength at 100MHz for different clock signals

The signal strength of any 5 V clock signal at its base frequency is:

\[
20 \times \log\left(\frac{5V}{2 \times \sqrt{2} \times 1\mu V}\right) = 125 \text{dB} \mu V
\]

If the signal is rectangular its strength decreases by 20 dB per frequency decade.

(1) Assumed its base frequency is 1MHz, the observation frequency of 100MHz is 2 decades higher, and therefore the harmonic strength is about 40dB lower. So the emission at 100MHz is 85dB\(\mu V\) (curve 1).

(2) Reducing the base frequency to 100 kHz reduces the emission at 100MHz by 20 dB as 100MHz is 3 decades higher than 100 kHz, the emission at 100MHz is accordingly only 65dB\(\mu V\) (curve 2).

If the signal is trapezoidal with about 2 ns rise- and fall-time its corner frequency is 160 MHz. Up to 160 MHz the signal strength decreases by 20 dB per frequency decade. From 160 MHz onwards the signal strength decreases by 40 dB per frequency decade.

(3) Assumed again the signal base frequency is 1 MHz, at 10 MHz the emission is already 20 dB lower and at the observation frequency of 100MHz it is another 40 dB lower (curve 1 until 160 MHz and curve 3).

(4) Reducing the base frequency again to 100 kHz reduces the emission at 100MHz by another 20 dB and the emission at 100 MHz is only 45dB\(\mu V\) (curve 2 until 160 MHz and curve 4).

(5) Lengthening the rise fall-/fall time to 20ns (factor 10) moves the 40dB bend to 16MHz (curve 2 until 16MHz then curve 5).

![Emission strength of rectangular and trapezoidal signals](image-url)
2.4 THUMB RULES

2.4.1 There are only three counter measures to achieve EMC

Handling of currents and voltages is of course much easier than working on 3-dimensional electromagnetic fields. Basically the number of countermeasures can be reduced to three.

(1) Avoidance of unnecessary RF-noise

In CMOS devices the switching circuits generate the noise. Reduction of for instance the switching frequency or the number of switching circuits reduces the power consumption and therefore, the emission. Any reduction of power consumption is a reduction of emission. This could be for example low voltage operation or the usage of power reduction modes of the devices.

(2) Keeping RF-energy away from antenna structures

As calculated in the last chapter, RF-energy is not a problem if the structures dealing with it are too small for acting as effective antennas. A decoupling capacity for example copes with the RF-energy, locally keeping most of the RF-current in a small loop between device and capacitor.

(3) Transforming RF-energy into heat

Any resistive material such as resistors, ferrites etc. can be used for this measure.
2.4.2 Any piece of wire has impedance

When discussing higher frequencies a wire is not longer just a zero Ohm connection. Any wire has impedance caused by its self-inductance. As per [1] the self-inductance is in the range of 0.5nH/mm to 2.0nH/mm. For EMC the absolute value is not important, but the acknowledgement and detailed contemplation of this impedance is of highest importance. According to

\[ Z' = 2 \pi f \cdot L' \]

with \( L' = 1 \text{nH/mm} \) as a medium value the inductor impedance at for example 100MHz is

\[ Z' \approx 0.6 \frac{\Omega}{\text{mm}} \]

Example:

The blue plot in Figure 2-5 shows the calculated impedance of a decoupling capacity of 10nF in 0603 package (ESL = 0.6nH) and X7R dielectric (ESR = 0.2\( \Omega \)). The red plot shows the same capacity but connected via two little stubs of “only” 5 mm each (L= 2 * 5nH).

Obviously, from a specific frequency onwards the distance between both curves is nearly constant. In this example from about 60 MHz onwards the “red impedance” is at least 17 times higher than the “blue impedance”. Further, the low impedant area of the series resonance has become much smaller and has moved to lower frequencies due to the trace inductance. Overall, the capacitors filter efficiency has suffered dramatically from the two “little” stubs.

---

**Figure 2-5:** Stub wire impedance influence
2.4.3 Linear versus logarithmic scale

In EMC huge dynamic ranges (µV to KV) have to be described. The logarithmic scale is preferably used when small values within a huge dynamic range shall be described. The logarithmic scale is a comparative scale and therefore always requires a reference value. It uses the artificial unit dB and is calculated as per following formula:

\[
\frac{Value}{dB} = 20 \times \log\left(\frac{Value}{Reference}\right)
\]

For specific reference values (µV, µV/m etc.) the reference is marked by using dB with suffix (dBµV, dBµV/m). If not marked the reference must be mentioned explicitly. Due to the nature of the logarithms the multiplication in linear scale is replaced by a summation in logarithmic scale. Therefore, for estimation the terms as given in the table below are useful. For example the stub wires above increase the impedance by factor 17, which is approximately 16 or 2 × 2 × 2 × 2. In other words the impedance is increased by 6 dB + 6 dB + 6 dB + 6 dB or 24 dB compared to the minimum impedance.

<table>
<thead>
<tr>
<th>Linear</th>
<th>Logarithmic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Factor 0.1</td>
<td>- 20 dB</td>
</tr>
<tr>
<td>Factor 0.5</td>
<td>- 6 dB</td>
</tr>
<tr>
<td>Factor 2</td>
<td>+ 6 dB</td>
</tr>
<tr>
<td>Factor 10</td>
<td>+ 20 dB</td>
</tr>
<tr>
<td>Factor 100</td>
<td>+ 40 dB</td>
</tr>
<tr>
<td>Factor 1000</td>
<td>+ 60 dB</td>
</tr>
</tbody>
</table>

Table 2-1 linear vs. logarithmic scale
2.4.4 Definition of frequency ranges

In this application note the definition of low, mid and high frequencies shall be handled in relation to the frequency response of major elements on PCB, such as decoupling capacities. Therefore, the frequency ranges mentioned below are only for rough orientation.

(1) ‘Low’ are all frequencies at which the parasitic elements such as ESL or trace impedance can be neglected. This is typically the case for frequencies below up to about 30 MHz.

(2) ‘High’ are all frequencies at which the parasitic elements such as ESL or trace impedance must be considered. This is typically the case for frequencies from about 80 MHz onwards.

(3) ‘Medium’ are the frequencies in between.
3 RENESAS MICROCONTROLLER

The microcontroller portfolio of Renesas includes general-purpose microcontroller families as well as microcontroller families especially designed for specific markets. For many years now Renesas CMOS microcontroller incorporate a variety of EMC techniques. Some of these techniques are effective without any measure on customer side. Others require appropriate action on PCB-design side. Therefore, it is necessary to understand major sources of noise inside a Renesas CMOS microcontroller and its propagation to the environment.

3.1 A TYPICAL MICROCONTROLLER LAYOUT

In the following chapters details of semiconductors will be discussed. The technical terms shall be briefly explained by means of the following picture.

Figure 3-1: A typical microcontroller layout
Chapter 3 Renesas Microcontroller

All internal logic except AD-converter, oscillator and I/O-ring is identified as the core. Typically the core has no connection to pins except for its power pins. In the above picture for example the core contains the CPU, PLL, program memory, RAM and peripherals including CAN memory. The I/O-ring consists of the power and ground rail system with the port buffers and their protection circuits. The I/O-ring power supply of most NEC microcontroller is separated from the core power supply.

3.2 MAJOR NOISE SOURCES

As per experience in REE especially at higher frequencies the narrow band noise is higher than wide band noise. Therefore, the following chapters will concentrate on narrow band noise.

3.2.1 Oscillator

When considering clocks and narrow band noise, naturally the oscillator comes into someone’s mind. Figure 3-2 shows a typical measurement of the quartz oscillator signals X1 and X2 of a Renesas microcontroller. Although the signal shape is not exactly sinusoidal it is obviously close to. In fact, power spectrum measurements show only few harmonics. Further, compared to the total power consumption of a microcontroller, the power consumption of the oscillator is rather low. Therefore, the contribution of the quartz oscillator of a Renesas microcontroller to the applications noise emission is rather low. Nevertheless, the signal shape and thus the spectrum may be much different for other types of oscillator, for example RC-oscillator.

**Note:** Although the quartz oscillator is not a big issue for emission it may be susceptible to noise. Therefore, special care must be taken when routing the oscillator section of a microcontroller application.

![Quartz oscillator signals X1 and X2](image-url)
3.2.2 Core, PLL and clock-tree

Inside a digital device like a microcontroller a sinusoidal clock cannot be used. Therefore, in Renesas’ CMOS microcontroller the oscillator clock is rectangular reshaped and distributed inside the device via the clock-tree. For functional reasons the propagation delay into the various branches of the clock-tree must be tuned to provide the clock-edges all over the device at almost the same time. All switching core elements therefore, draw current at almost the same time. The resulting pulsed core supply current is the major core related noise source. Renesas microcontrollers usually use both edges of the clock. The resulting narrow band spectrum of the core current shows peaks at the core operation frequency and its harmonics, showing typically a maximum at twice the core operation frequency. As Renesas microcontroller commonly include one or more clock divider, harmonics of lower frequencies have to be expected as well. Finally, the internal data operation etc. contributes with some wide band noise at low level. As outlined before the oscillator is designed to be a minor source of noise and the core current is related to the core operation frequency.

Assuming that the core frequency is constant, the generation with a slow oscillator and a PLL (e.g. 4 MHz * 4 = 16 MHz) or using a faster oscillator (f.e.16 MHz) should cause a similar level of emission.

3.2.3 External memory interface

The external memory interface consists of address bus, data bus and some control signals. The address bus is output by the microcontroller and usually, due to non-linear access sequence, provides non-periodical signals. Thus, the address bus EME contribution is rather wide band noise. As the lower address bits are usually more frequently switching than the upper bits these are the more critical signals.

In case the external memory is ROM or flash type the data bus is driven by the memory. Even if the memory is a RAM, the read-cycles usually dominate. Therefore, the EME contribution of the data bus is mainly determined by the memory device(s).

For EME the control signals are the most interesting portion of the memory interface. The most critical signal is the system- and/or memory-clock driver (SDRAM) as it generates significant narrow band noise. Even if the pin is open (but active) its noise contribution may be significant (see also explanations on cross-talk to I/O-ports). Therefore, wherever possible, this clock driver should be switched off. Finally, the strobe signals (RAS, CAS, ASTB, etc.) are potential noise sources as they are often and somehow repetitive (narrow band) switching.

3.2.4 General purpose ports in the I/O-ring

The EME contribution of these pins can not be estimated generally as the user configures these pins. Static or occasionally switching pins should not cause significant emission, while frequently switching pins have to be considered as potential noise sources. Again, repetitive switching pins comprise higher noise potential than non-repetitive pins due to their narrow band character. Examples are system clock driver (FOUT) or CSI-clock, but also CSI-data output or CAN-data output.
3.3 **Noise Propagation to Non-Switching Pins**

Switching pins are very obvious noise sources. Unfortunately, there are also other effects that lead to emission of ostensibly unconcerned pins. Some of these shall be described now.

### 3.3.1 Microcontroller supply system

A supply system consists of one or more power pins and their related ground pins. Commonly, Renesas microcontrollers provide several separated power supply systems, which are separated from each other on power and ground side. At least one decoupling capacity for each power supply system is mandatory to provide the required power at low impedance over a wide frequency range.

Any active element inside a microcontroller has a direct or indirect connection to at least one power supply system. Thus, any switching inside the microcontroller causes a current to flow. The emission of this current is proportional to the area of the loop(s) in which the current flows. Hence, these loops have to be designed as small as possible. The most important example here is the current loop between microcontroller and decoupling capacity.

Any power supply's source impedance is higher than 0 Ohm, especially at higher frequencies when the inductive wire impedance becomes significant. Therefore, pulsed currents overlay a ripple voltage to the DC power supply that contributes to the emission. Providing the power to the microcontroller at low impedance may reduce this emission.

### 3.3.2 Cross-talk of core noise to I/O-ports

**Common Impedance Coupling**

Any two circuits sharing some common impedance in their power supply will suffer from cross-talk between each other. The left part of below figure illustrates the core-noise propagation in case of a common power supply for core and I/O-ring. The noise is caused by the core-current related voltage drop across the bond wire and pin inductance. In Figure 3-3 these are represented by the shown resistors. Even if the power supply system on PCB were to be free from any voltage ripple the chip-internal power supply would be noisy. As the port buffers and the core refer to the same internal power supply, the noise propagates to each output pin via the active transistor. However, not only output pins, but also input pins are affected due to parasitic capacities (for example protection circuits) inside the chip. With this configuration EME sensitive applications may require filtering of each pin. At least for microcontrollers with many pins this is for cost and PCB space reasons seldom reasonable.
(2) Capacitive and inductive coupling

As per the experience in REE, the common impedance coupling is the prevailing effect for cross-talk from core to I/O-ports. Nevertheless, capacitive and inductive coupling inside the chip and/or the package occurs as well. Due to rather high source impedance the capacitive coupling should not be a big issue. Inductive coupling occurs whenever a high frequency current flows beside another wire. On-chip this effect is minimized by means of optimized routing, even though the bonding can hardly be optimized as it is a highly aligned structure. Therefore, comparably higher core related noise has to be expected on pins adjacent to core power or ground pins.
3.3.3 Cross-talk between I/O-ports

The cross-talk effect due to common impedance coupling as described above generally also occurs between I/O-ports. For obvious reasons not each and every I/O-port can be provided with a separate power supply system. Therefore, the cross-talk effects can be minimized by chip design measures but not avoided at all. Possible countermeasures on application side are for example reduction of frequency or filtering of the most affected pins. As cross-talk to inputs usually is lower than to outputs also temporarily re-configuring of outputs to inputs (where possible) may help. Unnecessary switching should be avoided at all. For example if the system clock driver is not used (open pin) but active, the cross-talk to other I/O-ports may be too high to comply with fastidious EME requirements.

Figure 3-4: Cross-talk between I/O-ports
4 EXAMPLES FOR ON-CHIP EMC MEASURES IN RENESAS MICROCONTROLLER

For many years now Renesas CMOS microcontrollers incorporate a variety of EMC measures. On-chip capacities and spread spectrum clock generator, although effective without any measure on PCB design side, are described first. Further, as the application note focuses on PCB design techniques only few on-chip measures out of the Renesas EMC portfolio are shown here. These are powerful measures for EMC, which should be considered during the selection phase for a microcontroller.

4.1 ON-CHIP CAPACITIES

EME-optimized decoupling is intended to provide a maximum of the required RF-current by one or more decoupling capacitor(s). The more RF-current is kept in the loop between the switching circuit on the chip and the capacitor the lower is the contamination of the remaining power supply circuit. For optimization of the connecting line impedance usually the capacitor is located as near as possible to the supply pins of the microcontroller. For reduction of the current loop emission, the loop area should be minimized. By using only PCB-design techniques further significant improvements are difficult to achieve. Thus the consistent countermeasure is to move parts of the decoupling capacitor onto the chip thereby reducing the connecting impedance and the currents loop area considerably. These on-chip capacities are too small to provide the whole decoupling, so capacities on PCB are still necessary. Nevertheless, for the higher frequency range they may reduce the emission impressively.

The measurement results in Figure 4-1 compare the “same” microcontroller with and without on-chip capacities. The red plot shows the emission of the original version and the blue plot of the redesigned version with on-chip capacities. Over a wide frequency range improvements of up to about 15 dB have been achieved without increasing the chip size, means without adding extra cost.

Figure 4-1: EME with on-chip capacities
4.2 Spread Spectrum Clock Generator (SSCG)

As per the experience in REE, especially at higher frequencies the narrow band emission is dominant against the wide band emission. The nature of narrow band spectra is to show only portions at discrete frequencies, while in between showing the environmental noise. Unfortunately, if only one peak is above the limit the application fails the test although wide frequency areas may show big distance to the limit. By modulating the CPU operation frequency the HF-energy is spread over a wider frequency range thereby reducing the peak energy. The blue measurement results in Figure 4-2 show the emission peaks of static frequencies. The red plot shows the modulated spectrum measured with a peak detector while the black plot was measured with a quasi-peak detector. With a modulation of only about ± 1% the peak emission was reduced up to about 10 dB by distributing the HF-energy over 2 MHz bandwidth. Further improvements can be achieved by increasing the modulation width.

![Figure 4-2: Down Jitter EME with SSCG](image-url)
4.3 **Multiple Separated Power Supplies**

In Renesas microcontroller the power supply separation is widely used to effectively reduce cross-talk between core and I/O-ports. Further analogue circuits, clock generation and sometimes the external bus interface may be supplied separately. For gaining the maximum improvement the separation is usually made on power- and ground-side although this causes considerably higher efforts for internal ESD protection. Beside protection efforts the utilization of this measure is further limited by the availability of pins, especially in small packages with low pin-count. On the other hand, devices with high pin-count may have multiple supply pins for the same supply system in order to reduce the connecting impedance between PCB and on-chip supply system.

**Required action on PCB design side:**

Although being separated in the power supply of course there are some internal control signals between core and I/O-driver or any other separated circuit. In order to keep both supply systems on a similar potential both grounds must be connected with each other on the PCB via low impedance.

**Figure 4-3**: Ground impedance consideration
4.4 **Adjacent Power and Ground Pins**

The majority of Renesas microcontrollers are equipped with adjacent power supply pins. This pinout allows the PCB designer to easily minimize the current loop size between microcontroller and decoupling capacity. Minimization of the loop size of course requires one capacity each per adjacent supply pair. Concurrently, reduction of the loop size also reduces the connecting impedance of the decoupling capacity.

**Required action on PCB design side:**

Move the decoupling capacities as near as possible to the supply pins. Treat each piece of wire like impedance. Especially, the connection of the decoupling circuit with the board power supply system should be carefully considered.

**Remark:** Listed above are only few of today's possible on-chip EMC measures. As per common understanding, measures to achieve EMC are the more effective the nearer to the source of the noise these are applied and the earlier in the design process these are taken into account. Problems on EMC identified at late stage during application tests not only cause high cost for their correction, but sometimes also delay market introduction of the whole application. Further, at that stage several substantial decisions such as device selection have been made. Thus, consideration of LSI-level EMC measurements prior to selecting a new microcontroller for future projects is recommended.

**Note:** IEC 61967-x is a suitable family of test standards for chip-level EMC measurements. Renesas provides measurement reports of almost all microcontroller device families according to IEC 61967-4. Please contact your local Renesas sales representative to get a copy of a specific measurement report.
5 EXAMPLES FOR IMPROVED EMC OF RENESAS MICROCONTROLLER

5.1 POWER SUPPLY OPTIMIZATION

The power supply system of a PCB usually consists of a ground system and one or more power supplies. Power and ground nets are usually the most distributed nets in the circuit, thereby unfortunately providing a suitable antenna for the microcontroller supply noise. Therefore, it is inevitable to carefully design the power supply circuit. The first step to achieve an optimized power supply design is to analyze the distortion potential of any device power and ground pin as considered above. PCB-design should always start with the routing of the power supply system.

5.1.1 Ground system

(1) System ground: The system ground has two major functions: On the one hand it is part of the power supply system and on the other hand it provides the reference level for all signals. According to Ohm’s law any supply current in the ground system will cause a voltage drop proportional to the ground impedance. Due to the common used ground impedance (compare to section 3.3.2 (1) common impedance coupling) this voltage overlays all signals referring to this ground. For optimization the ground should have the lowest possible impedance and the noise current in the system ground should be minimized.

(2) Ground plane: In a multilayer PCB the first requirement can be fulfilled by utilizing a complete layer as a ground plane. The ground layer must be free from any signal traces or other gaps longer than 10mm. Any gap in the ground increases its impedance and introduces so-called slot-antennas. Examples of unwanted slots are shown below.

![Figure 5-1: Principal Slot Antennas](image1)

![Figure 5-2 Slot Antenna Layout](image2)
(3) Local device ground: The second requirement can be served by providing an extra local device ground below the device. This local device ground shall be connected low impedantly to the system ground in its centre as shown. By means of this structure local RF-currents are kept away from the system ground thereby avoiding related voltage drops in the system ground. The four connections to system ground as shown in Figure 5-3 are a compromise between low impedance (¼ the impedance of a single via connection) and minimum parallel connection between both grounds.

Figure 5-3: Local device ground QFP

Figure 5-4: Grounding BGA
(4) Ground fill: Usually not every area on every layer is used for wiring. These unused areas should be filled with copper and shall then be connected to ground. It is not sufficient to connect these ground fills just “somewhere” to the ground plane. These ground fills shall be connected to ground in a grid at least every 10 mm (see also Figure 5-67). This measure further reduces the ground impedance and concomitantly reduces the cross-talk between layers.

(5) Guard ring on PCB-edges: The mayor advantage of a multilayer PCB with ground-plane is the ground return path below each and every signal or power trace. As shown in Figure 5-5 the field lines of the signal return to PCB-ground as long as an “infinite” ground is available. Traces near the PCB-edges do not have this “infinite” ground and therefore, may radiate more than others. Thus, signals (e. g. clocks) or power traces (e.g. core power) identified to be critical should not be routed in the vicinity of PCB-edges, or – if not avoidable – should be accompanied by a guard ring on the PCB edge.

The intention of the guard ring is that RF-energy, that otherwise would have been emitted from the PCB-edge, is reflected back into the board where it partially will be absorbed. For this purpose ground traces on the borders of all layers (including power layer) should be applied as shown in Figure 5-5. As these traces should have the same (RF-) potential as the ground plane they must be connected to the ground plane at least every 10 mm.

---

Figure 5-5: Field lines of a signal above ground

---

Figure 5-6: Side view Guard ring in a 4-layer PCB

---

Figure 5-7 GND Guard Ring (PCB Top View)
5.1.2 Power routing and decoupling

After a reliable and low impedant ground was established the next step in PCB-design is the power routing.

(1) Power plane versus routed power traces: In multilayer PCB’s often one entire layer is used as a power plane. Other design methods comprise routed power traces or a combination of both techniques. The following shall oppose some advantages and disadvantages of both techniques.

<table>
<thead>
<tr>
<th>Advantages of power planes</th>
<th>Disadvantages of power planes</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Easy and fast to implement</td>
<td>• Requires one plane per supply system</td>
</tr>
<tr>
<td>• Low inductive power supply</td>
<td>• Increases cross-talk between different supply systems if these aren’t separated by a ground plane</td>
</tr>
<tr>
<td>• Creates a capacity together with ground plane</td>
<td>• Due to low impedance distributes noise from one source into the whole supply system</td>
</tr>
<tr>
<td></td>
<td>• Tempts the PCB-designer to less careful power design</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Advantages of routed power supplies</th>
<th>Disadvantages of routed power supplies</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Allows the usage of one layer for more than one supply system, thereby reducing the cross-talk between these supplies</td>
<td>• Requires more careful power routing</td>
</tr>
<tr>
<td>• May reduce cross-talk within each supply system</td>
<td>• Higher supply impedance may require extra capacity for supply stabilization</td>
</tr>
<tr>
<td></td>
<td>• Considerable DC-resistance in case of high current</td>
</tr>
</tbody>
</table>
The optimum obviously is to apply the advantages of both methods. Therefore, several local power planes should be implemented and connected to the supply via traces. Planes of different supply systems should be located in the same layer or separated by a ground plane to minimize cross-talk between these systems. Although the local power planes are easy to implement special care must be taken when connecting the power pins and the decoupling capacities to the planes.

(a) Connection of decoupling capacities

The decoupling of the most critical power supply pins of the microcontroller (for identification of these refer to 1) very often is the most fastidious part in a PCB design. Even in a multilayer design every millimeter of trace has to be carefully considered.

(b) Sketch equivalent circuits

A piece of paper and a pencil are still useful tools. When considering the best placement, direction and connection of the capacity a small sketch may be very useful. Each piece of wire shall be drawn as impedance even though the actual value is not important. Figure 5-8 clearly indicates that the two red impedances should be minimized while the other two may be object to concessions.
Figure 5-9 shows the implementation in the PCB-layout. The connection to the local ground plane has been kept as short as feasible. The power trace is routed from the device via the capacity pad to a VIA (through hole connection), which connects it to the inner power plane. Placing the VIA for example in the centre of the red trace would have added several nH to the capacitors impedance and thereby would have reduced the filter efficiency tremendously. Further, no power for other pins and/or devices must be fetched from the red trace, as it is very noisy.

Figure 5-9: Decoupling PCB-layout

(2) A VIA has a considerable impedance: As any trace also a VIA has a considerable impedance. Therefore, VIAs of critical circuits such as decoupling circuits must be exclusive for this circuit. The two left parts of Figure 5-10 indicate how a shared VIA causes cross-talk between the involved circuits. The right most part shows the correct wiring.

Figure 5-10: Cross-talk due to a shared VIA
(3) **Filter:** When the above described design techniques are followed most applications should comply with their EMC requirements. Nevertheless, in case of critical EMC requirements or complex designs further filter elements may be necessary. In REE good experience was made with a multiple stage power supply filter.

(a) **Multiple stage power supply filter**

The most critical power supplies should be filtered in multiple stages to achieve the maximum possible noise suppression. An example filter circuit is given below. As outlined before, the impedance of each piece of wire has to be considered. Especially, the connections of the vertical elements (e.g. all capacities) are critical. The T-filter for example provides a perfect connection of the power-line to the capacity without adding extra impedance. Only if the PCB design provides a comparably low impedance connection to ground the full suppression can be achieved.

Figure 5-11: Multiple stage power supply filter

![Filter Circuit Diagram](image)

**RF-C:** For inductance minimization the smallest feasible package (0603 or smaller) should be used. Ceramic material NPO or at least X7R shall be used. The capacity value has to be evaluated during EMC tests. Start value should be the maximum available capacity in the chosen package. The connection to the device shall be implemented as described in Chapter 0 “Power routing and decoupling”.

**Decoupling-C:** This capacity provides medium frequency current to the device as it forms the pulsed device current into average “DC”-current. Its main task is to keep the power supply within 1.5V ± 5% DC-specification (e.g.). One or more decoupling capacity (47 nF to 100 nF, X7R, 0603) shall be connected to the local VDD-plane. The required capacity shall be calculated according to below formula, several capacities in parallel may be required in order to reduce the ripple caused by ESR and ESL.

\[ Q = C \cdot U = \int idt \quad C \approx \frac{i \cdot \Delta t}{\Delta U} \]

with Q = Electric charge
with U = Voltage
with C = Capacity
Example for a core voltage decoupling:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage (U)</td>
<td>1.2V</td>
<td>Core voltage</td>
</tr>
<tr>
<td>Max ripple voltage (U\text{ripple})</td>
<td>12mV</td>
<td>1% U</td>
</tr>
<tr>
<td>Min rise time (t\text{rise})</td>
<td>1ns</td>
<td>Typical value</td>
</tr>
<tr>
<td>Average current (I\text{average})</td>
<td>100mA</td>
<td></td>
</tr>
<tr>
<td>Frequency (f)</td>
<td>80MHz</td>
<td>Typical CPU frequency</td>
</tr>
</tbody>
</table>

Table 5-1 example core voltage decoupling

\[
C \approx \frac{0.1A \times 12.5 \times 10^{-9} \text{s}}{12 \times 10^{-3} \text{V}} = 104.2 \text{nF}
\]

The resulting decoupling capacity has to be at least 100nF then. Nevertheless, the ESL of the capacity has to be taken into account then, as well.

An assumed ESL of a 0603 cap is 1nH. From the impedance point of view (at 80MHz) this results in.

\[
Z \approx 2\pi f L = 2\pi \times 80 \times 10^6 \text{Hz} \times 1 \times 10^{-9} \text{H} = 0.5 \Omega
\]

This leads to a voltage drop of:

\[
U \approx Z I_{\text{surge}} = 0.5 \Omega \times 0.1 \text{A} = 0.05 \text{V}
\]

which is about 5 times the acceptable ripple voltage.

Therefore, a parallel set of capacitors is absolutely mandatory to reduce the ESL impedance.

This is even more to be taken into account, having a BGA with several supply pins. Here it is not only mandatory, but necessary, since the trace impedance between capacitor and pin to decouple is even higher then.

The connections to the ground plane and to the local VDD-plane shall be made by at least two VIAs each. If the production constraints allow, the VIAs shall be placed within the soldering pads, otherwise the shortest possible trace-length (max. 1 mm) shall be used for connection.
**T-Filter:** The ferrite T-Filter (e.g. Murata NFM60R30T222) separates the local $V_{DD}$ plane from global $V_{DD}$. It keeps the antenna for the device supply current noise small and transforms HF-energy into heat.

The ground connection is most critical and shall be made by at least two VIAs. If the production constraints allow, the VIAs shall be placed within the soldering pad of the filter, otherwise the shortest possible trace-length (max. 1 mm) shall be used for the ground connection.

**Figure 5-12:** Local VDD separated by T-Filter

**Filter-C:** This filter capacity (47 nF to 100 nF, X7R, 0603) forms another LRC-Filter with the 1st half of the ferrite filter.
(b) 3-terminal capacitors (Feed-through capacitor)

ESL (Equivalent series inductance) and ESR (Equivalent series resistance) is very small, the self-resonance frequency is high. So improvement of EMI can be expected by using a 3-terminal capacitor.

The example of insertion 3-terminal capacitor indicate Figure 5-11,12. 3-terminal capacitor with "through" connection works as a filter. 3-terminal capacitor with "non-through" connection works as a bypass capacitor.

Figure 5-13: Example: 3-terminal capacitor with "through" connection

Figure 5-14: Example: 3-terminal capacitor with "non-through" connection
(c) Spare bridging elements

In case the distortion potential of a power supply is not clear the best possible filtering should be implemented with the option to omit parts that according to later evaluation may not be needed. Parallel parts are easy to omit but serial parts require an optional bridging element, for example as shown in Figure 5-15. If later tests prove the necessity of the serial element no other parts have to be moved to find a place for the new element. On the other hand, this must not be done extensively, as these may cause space restriction for other parts of the circuit.

Figure 5-15: Spare bridging element
5.2 SIGNAL ROUTING

Before starting the PCB-design the circuit should be analyzed for critical signals according to the back-ground as described for example in this application note. For most critical signals such as clocks, strobes and other often switching signals one or more of the following measures should be applied.

5.2.1 Line termination

According to [5] circuit designers can choose from many different termination techniques. Line termination may be necessary on long traces to avoid reflections or on short traces to avoid ringing. Most common are end- or source-terminations. End-terminations for example minimize the rise time of the signal and therefore, may be suitable for speed optimization. Source- or series-terminations minimize the current on the signal trace and are preferable for emission reduction, therefore.

The resistor for series termination has to be located as near as possible to the driver (source) of the signal. It may be optimized to match the transmission line impedance or to create a low pass filter with the load capacitance. If the transmission line impedance shall be matched the sum of driver impedance and resistor value has to be equal to the transmission line impedance. For EME-optimization the current on the signal trace and the harmonics of the signal frequency should be minimized. Thus, a resistor value as high as the timing and functional constraints allow is desirable here.

5.2.2 Transmission lines on PCBs

Transmission lines have the lowest emission within the variety of traces, as the return current can flow directly under the line. Thus, the spanned return current loop is as short as it can be.

The most common transmission lines used on PCBs are either strip line or microstrip line geometries. More or less complex and accurate formulas for the calculation of impedance, delays etc. are available in [5]. In Figure 5-16 drawings 1 and 2 are examples for microstrip lines; drawing 3 is an example for strip line geometry. It is important to note that the calculation of strip line or microstrip line parameters presumes infinite ground. As this is not realizable the ground plane on either side of the signal trace should be at least five times wider than the maximum of signal-trace-width and signal-trace-distance to ground. This requirement is another reason for implementing the guard ring as it allows to route traces near the board edges.

When implementing strip lines or microstrip lines in a PCB-design make sure that above presumption is met by the design. Any crossing of other traces locally modifies the characteristic of the strip line or microstrip line and may cause inadvertently higher emissions. Also the power plane is not suitable as reference plane for a strip line or microstrip line.
5.2.3 Layer stacking

The layer stacking, i.e. the distances between all layers of the PCB, should be carefully considered and defined. The distance to ground and the thickness of the surrounding material influences the characteristic of all traces. Further the emission of a signal above ground is somehow proportional to its distance from ground. Therefore, the maximum height of any critical signal above ground should not be more than 0.2 mm. Clocks of frequencies higher than 30 MHz should not be farther from ground than 0.1 mm. Frequencies higher than 50 MHz should be routed as a strip line.

If only very few strip lines are required the second ground plane can be avoided by covering these signals with ground. For that purpose the clock signal is routed on a layer adjacent to the ground layer. On the next layer a wider ground trace is routed on top of the clock signal. This ground trace is connected to the ground plane on both sides of the clock signal every 5-10 mm. Figure 5-17 gives an example for a covered signal line on a 4-layer PCB.
5.3 **OSCILLATOR**

User manuals of Renesas microcontroller usually contain a chapter on the oscillator and its allowable and not-allowable wiring. Make sure to read this chapter prior to designing the clock circuit of your PCB.

5.3.1 **Optimized pinout**

Quartz oscillators in Renesas microcontroller usually are optimized for the intended frequency range and therefore, should not be critical for emission. Nevertheless, Renesas microcontrollers commonly provide an oscillator pinout that allows short connections between quartz and microcontroller as shown in Figure 5-14. Further, the adjacent ground pin allows an easy implementing of a special guard ring around the oscillator circuit.
5.3.2 Oscillator ground connection

Although the impedance of a ground plane is low, it is of course not zero. Therefore, any noise current in the ground plane causes a voltage drop in the ground. If the two capacities of the oscillator are connected directly to the ground plane the voltage drop in the red portion of the ground in Figure 5-19 will be overlaid to the oscillator signals. If the noise related voltage drop is big enough the oscillator may be disturbed.

The overlay of ground noise may be avoided by providing an extra ground trace for the oscillator ground as indicated in green in Figure 5-20. This is even in a multilayer PCB a powerful measure to improve the susceptibility of the oscillator.
5.4 REGC CONNECTION

If a Renesas microcontroller is equipped with an on-chip regulator, a lowered core voltage is provided. From functional and EMC point of view, a special external circuitry is necessary.

While VDD is the supply of the regulator here, REGC is the core voltage output and VSS is the respective decoupling potential and μC GND.

5.4.1 Circuitry

Usually, a bigger capacitor is used to stabilize the core voltage. This one should be sized as described in the accompanying microcontroller documentation. A smaller one (in the range of 100nF) is used to decouple VDD at VSS. Both capacitors shall be placed in close vicinity to the microcontroller, as the resulting decoupling loop and its spanned area (red for REGC and green for VDD) are to be kept as small as possible, to reduce emission here. This is shown in Figure 5-21 REGC connection.
5.5 **RESET CONNECTION**

A reset pin may be sensitive against external noise. Therefore, in noisy environment, a ceramic filter capacitor is recommended for the RESET-pin. It should be placed near to the microcontroller and referred to the respective VSS pin of the µC.

![Reset connection](image)

The decoupling capacitor of VDD has the higher priority here and is Therefore, placed nearer to the CPU than the Reset decoupling capacitor.
6 ITEMS TO REMEMBER

(1) Direct semiconductor contribution to the far field emission can be neglected, as on-chip structures are too small for being an effective antenna. The microcontroller generates currents and voltages, which stimulate the PCB layout and the connected cables. EMC of microcontroller devices is Therefore, mainly an issue of current, voltage and impedance. The PCB and the connected wiring harness act as antenna structures in both directions (EME and EMS).

(2) Any piece of wire has an inductance that gets remarkable impedance with increasing frequency. Especially in filter circuits any wire impedance must be considered. Capacitors may be switched in parallel to increase the capacity and reduce the inductive influence.

(3) Decoupling loops should be as small as possible, as the emission is proportional also to the spanned loop area.

(4) Especially, at higher frequencies the narrow band noise usually is dominant against the wide band noise. Emission related to the device operation frequency is mainly emitted by the supply- and ground-current of the core while the noise contribution of the oscillator is rather low. The most critical signal of the external memory interface is the system- and/or memory-clock driver, followed by strobe signals like CAS, RAS or CS.

(5) Frequently switching IO-signals, especially repetitive signals have to be considered to significantly contribute to the applications emission. The system clock driver should not be enabled for EME - sensitive applications. Inline resistors will smoothen the rise- and fall times of signals and reduce the emission contribution of these signals.

(6) The maximum height of any critical signal above ground should not be more than 0.2 mm. Clocks of frequencies higher than 30 MHz should not be farther from ground than 0.1 mm. Clocks of frequencies higher than 50 MHz should be routed as a strip line or as covered signal line.
7 LITERATURE

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Table 7-1 References