INTRODUCTION

The QuickSwitch family of FET switches was pioneered in 1990 to offer designers products for high-speed bus connection and logic replacement with sub-nano-second propagation delay, zero added noise and timing skew, and no additional static power dissipation. Since their introduction, QuickSwitch products have gained acceptance as ideal devices for hot-docking, voltage translation, capacitance isolation, logic replacement, clock gating, and several other applications.

WHAT IS A QUICKSWITCH?

In its basic form, a QuickSwitch is an N-channel FET switch controlled by either combinatorial or sequential control logic using CMOS technology. The low ON resistance (typically 5Ω), low capacitance, high current capacity, and very high OFF resistance, make the FET switch an ideal element for bus connection. Figure 1 shows the basic QuickSwitch configuration.

![Figure 1. Basic QuickSwitch](image)

When the switch is enabled, the gate of the N-channel switch transistor driven by a CMOS logic gate is at Vcc and the switch exhibits a typical ON resistance of 5Ω. When disabled, the gate of the switch is at Ground potential and the switch offers very high resistance between the A and B terminals. In the OFF state, the leakage current at the switch terminals is typically 10nA, and the capacitance between the terminals is low. Typical capacitance at the switch terminals is 5pF in the OFF state. These properties make the QuickSwitch an ideal device for unbuffered bus connection.

QUICKSWITCH ON RESISTANCE

The ON resistance of the QuickSwitch is determined by the size of the switch FET and the voltage applied to the switch terminals. The ON resistance decreases as the voltage between the switch gate and the switch terminals increases. Therefore, the switch exhibits a somewhat nonlinear ON resistance characteristics with respect to the voltage at its input terminal. Note that the FET switch is essentially bidirectional. Therefore, either of the two switch terminals can be regarded as the input, the other being the output.

A plot of the ON resistance of a QuickSwitch is shown in Figure 2.

![Figure 2. QuickSwitch ON Resistance vs. V IN](image)

A typical QuickSwitch device has an ON resistance of less than 5Ω for input voltages near Ground. The resistance rises as the switch input voltage rises. At the TTL High voltage of 2.4V at the switch inputs, the ON resistance is typically 10Ω. As the switch input voltage rises towards Vcc, the switch exhibits higher ON resistance. At input voltages approaching approximately Vcc – 1, the switch enters cut-off region.

The input range also extends to 0.5V below ground. Below this voltage, the clamp diode connected to the switch terminal begins to draw current.

QUICKSWITCH WITH SERIES RESISTOR OPTION

IDT offers most QuickSwitch functions with a series resistor option. These switches have an integrated resistor of typically 23Ω value in series with the switch. To obtain the ON resistance vs. Vin characteristics for a switch with the resistor option, the reader should add 23Ω to the graph in Figure 2. The series resistor serves as a source-termination resistor or a damping resistor to reduce noise caused by signals with fast transitions.

VOUT vs. VIN CHARACTERISTICS

The QuickSwitch provides a low resistance connection between the input and output over a wide input voltage range. Starting from Vin of approximately –0.5V, the output voltage equals the input voltage. This relationship is maintained until the input voltage reaches approximately Vcc – 1V. For input voltages between Vcc – 1 and Vcc, the output voltage gets clipped to approximately Vcc – 1 due to the ‘source-follower’ configuration of the N-channel switch. The Vin vs. Vout characteristics for three different output loads is shown in Figure 3.
QuickSwitch General Information

The switch develops a voltage drop across its terminals as a function of the load resistance. Because of the non-linear nature of switch resistance, the voltage drop is also non-linear as shown in Figure 4.

QuickSwitch V_out vs. Vcc

When the input voltage to the switch is at or near Vcc, the output voltage is approximately 1V below Vcc due to the "source-follower" configuration of the N-channel switch as described earlier. This voltage drop is process dependent and may vary from 1V to 1.3V. Increasing or decreasing the Vcc will increase or decrease the output voltage by the same amount as shown in Figure 5.

QuickSwitch Operation with TTL Signals

One common application of the QuickSwitch is its use as a bus switch. Some popular devices such as QS3245 are used for replacing FCT245 or ABT245 logic functions which interface between two TTL buses. In this application the QuickSwitch performs bus connection and bus isolation with sub-nanosecond propagation delay and zero added skew and ground bounce.

Figure 6 below shows the QuickSwitch as a bus switch driven by a TTL driver at its input. The switch output is connected to CMOS inputs which offer a capacitive load to the driver through the switch.
When the switch is closed, connecting the driver to its load, the gate of the N-channel FET is at Vcc and the switch transistor is fully ON. During the low-to-high TTL transitions at the switch input, the load capacitance will charge via the low ON resistance of the switch. Typically, a 50pF load will charge with a time-constant of 250ps through the 5Ω switch. During the high-to-low transitions, the load capacitance will discharge with the same time-constant. Since the time-constant is much less than the rise or fall time of the driver, the signal transition at the load is determined by the driver, and not by the switch. To a first approximation, the switch adds zero propagation delay. If the signal transitions at the switch input are TTL compatible, i.e. from 0 to 3.5V, these transitions are faithfully reproduced at the output with no additional noise.

When the switch is open, disconnecting the driver from the load, the gate of the N-channel FET is at 0V, and the switch transistor is OFF. The impedance between the switch terminals is extremely high. The parasitic capacitance at the switch terminals offers low AC impedance, thus minimizing signal feed-through between the switch terminals in the OFF state.

When the QuickSwitch is either powered down or is in the disabled state, there is no DC path from either switch terminal to either ground or Vcc for voltages above –0.5V. This feature makes the QuickSwitch ideal as an interface device for isolating system components during hot docking (live insertion).

The bus switch can replace drivers and transceivers in systems if bus repowering is not required. It provides no drive of its own, but relies on the driver connected to its input. For moderately capacitive loading, the QuickSwitch provides a net gain in speed because of the sub-nanosecond propagation delay through the switch, which is much smaller than the propagation delay through a buffer or a transceiver and the additional derating for the load capacitance.
QUICKSWITCH GENERAL INFORMATION

QUICKSWITCH RATINGS AND SPECIFICATIONS

INTRODUCTION
In this section, the ratings, AC and DC specifications, and test method for various parameters are discussed in order to provide information and clarification to the user.

ABSOLUTE MAXIMUM RATINGS
The absolute maximum continuous ratings are those values beyond which permanent and irreversible damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum conditions is not implied.

The Supply Voltage rating defines the absolute maximum Vcc that can be safely applied to the device. This rating is consistent with that of other TTL logic devices. The Supply Voltage rating is determined by the breakdown limits of internal components. If the Vcc is taken beyond the rated limit, excessive current may be drawn from the power supply due to device breakdown and permanent damage may occur due to excessive heat generated. As device dimensions are reduced to improve circuit performance, the breakdown voltage also decreases. As a rule of thumb, the absolute maximum Supply Voltage rating is normally 40% above the nominal operating supply voltage. For 5V circuits, the absolute maximum supply voltage is 7V. It is 4.6V for circuits operating at a nominal 3.3V supply. It is a prudent practice to limit even the transient supply voltage rise to the absolute maximum rating.

The DC Input Voltage rating is the maximum voltage that can be applied to the TTL control inputs of a QuickSwitch device. Since IDT’s QuickSwitch devices are designed without a clamp diode to Vcc to enable hot insertion, the DC input voltage may exceed Vcc provided it is less than the rated voltage. This rating is also determined by the breakdown characteristics of internal components.

The DC Switch Voltage is maximum voltage that can be applied to the switch terminals. For all devices which use an N-channel FET switch, the rated switch voltage is the same as the rated input voltage. For devices that use N-FET and P-FET combination, the absolute maximum switch voltage is limited to 0.5V above Vcc to prevent damage to the circuit due to excessive current flow through the parasitic diode associated with the P-channel FET.

The AC Input Voltage applies to the transient voltage (for example, voltage undershoot) at the TTL control input or switch input. It states that pulses of up to –3V can be tolerated for a duration less than 20ns without damaging the device. However, large undershoots can cause significant clamp current and local heating. If the transient pulses have a high duty cycle, the average power dissipation must be taken into account to ensure that the average DC current and power dissipation do not exceed the rated values.

The DC Switch Current per pin defines the maximum current that can be drawn through the switch in ON state to pull down an external load to ground.

The Power Dissipation defines the maximum total power dissipation capability of the device. It represents the package power dissipation limit based on the thermal time constant for the package/die combination and the maximum permissible chip junction temperature. The total power dissipation is the sum of static and dynamic dissipation components.

The Storage Temperature rating defines the extremes of temperature range that a package may be subjected to for long term storage, even the power being applied to the device.

INPUT AND SWITCH CAPACITANCE
Each control input pin and switch pin has a capacitance associated with it. The capacitance at a control input is due to the package and the input circuitry connected to the pin. It is package dependent and typically ranges from 3pF to 5pF.

The switch pins have two capacitance values—one for the OFF state and one for the ON state, as shown in Figure 7. In the OFF state, each switch pin is isolated and has a capacitance to ground. The capacitance in this state is the sum of pin capacitance and the total capacitance associated with the switches connected to the pin. For example, an individual switch in the QS3384 device will have a lower capacitance than the Mux pin of QS3253 Dual 4:1 Mux/Demux.

DC ELECTRICAL CHARACTERISTICS
The DC electrical characteristics define the input operating conditions for proper operation, responses to applied DC signals, and Switch characteristics over specified voltage and temperature range. Limits of all DC electrical characteristics are guaranteed over the recommended operating temperature and power supply range as stated in the data-sheets for individual products.
QUICKSWITCH GENERAL INFORMATION

V_{IH} and V_{IL} define the limits of guaranteed logic HIGH and logic LOW recognition levels at the control inputs. For example, V_{IH} limit of 2.0V implies that any voltage greater than 2.0V shall be recognized by the input circuit as a logic HIGH. Similarly, V_{IL} limit of 0.8V implies that any voltage less than 0.8V shall be recognized as logic LOW. Typical applied input voltages are between 3.5V and Vcc for logic HIGH and between 0V and 0.5V for logic LOW, thus assuring adequate noise margin. Note that the AC characteristics are guaranteed for input signal swing of 0V to 3.0V.

I_{IN} defines the input leakage current at the control inputs of a QuickSwitch. The typical input leakage current is of the order of 1 to 5nA at room temperature.

I_{OZ} defines the maximum leakage current at the switch pin in OFF state. The typical switch leakage current is also of the order of 1 to 5nA at room temperature, indicating the excellent Off-isolation characteristics of the QuickSwitch devices.

R_{ON} defines the resistance offered by a switch in the ON state. Since the resistance is a function of the input voltage applied to the switch, it is normally specified at two different values of input voltage. R_{ON} is measured by forcing the specified amount of current through the switch as shown in Figure 8. It is calculated by taking the ratio of voltage drop across the switch and the current forced through the switch.

\[ R_{ON} = \frac{V_{DROP}}{I_{FORCED}} \]

Figure 8. QuickSwitch R_{ON} Measurement

R_{ON} increases with the applied input voltage. The relationship between R_{ON} and V_{IN} is nonlinear and the ON resistance begins to increase significantly as V_{IN} approaches V_{CC}.

The Pass Voltage, V_{P}, relates to the output voltage "clipping" feature of the N-channel QuickSwitch when the switch input voltage is equal to or greater than the supply voltage. This feature is used in the 5V/3.3V translation applications. V_{P} is measured at the switch output at I_{OUT} = -5\mu A when the switch input is held at V_{CC}. Typical voltage drop across the switch under these conditions is 1V, thus giving a typical V_{P} of 4V.

POWER SUPPLY CHARACTERISTICS

The Power Supply characteristics define the components of power supply current under normal operating conditions.

I_{CCQ} is the Quiescent (static) power supply current when all control inputs are at logic LOW or HIGH levels and the switches are OFF. This current represents the leakage current between the Vcc and Ground pins of a QuickSwitch device. It will also include DC current through the device due to a resistive path from Vcc to Ground, if applicable.

\[ \Delta I_{CC} \]

is the power supply current component per each TTL control input when the input is in logic HIGH state. It represents the current through the input stage.

\[ Q_{CCD} \]

is the dynamic power supply current component expressed in terms of mA or mA per MHz. This current is measured with switch pins open and switching the control inputs with 50% duty cycle, so that it measures only the current required to switch the internal nodes of the circuit. Note that measured value of dynamic supply current at a given frequency includes the I_{CCQ} component which needs to be subtracted to obtain the Q_{CCD} value.

SWITCHING CHARACTERISTICS

The switching characteristics discussed below relate specifically to the switches. Other parameters such as set-up and hold times, release times, clock pulse width etc. have the same meaning and interpretation as those in logic circuits, and are excluded from the following discussion.

Data Propagation Delay parameters, t_{PLH} and t_{PHL}, refer to the delay through the switch in ON state. Since the switch behaves like a low value resistor, the propagation delay is related to the RC time-constant R_{ON} \times C_{L}, where C_{L} is the load capacitance. The time-constant is of the order of 1ns for R_{ON} = 5\Omega and C_{L} = 5pF. Note that the time-constant is of the order of 1.4ns for QuickSwitch devices with resistor options with typical R_{ON} = 28\Omega.

Switch Turn-on Delay specifications, t_{PZH} and t_{PZH}, define the time taken to cross nominal TTL threshold of 1.5V at the switch output when the switch turns on in response to the control signal.

Switch Turn-off Delay specifications, t_{PHZ} and t_{PHZ}, define the time taken to place the switch in high-impedance OFF state in response to the control signal. Since the output is undriven in the OFF state, external load must be used to move the output away from the previous logic state in order to create a measurable voltage change at the output. The turn-off delay is the time taken for the output voltage to change by 300mV from the original quiescent level, with reference to logic level transition at the control input.

AC Test Conditions

The AC test conditions used for the verification and guarantee of switching characteristics follow industry-accepted practices for high-performance standard logic products.

Control signals for changing the state of the switches transition between ground and 3.0V with a rise or fall time of 2.5ns measured between 10% and 90% points.

The AC test circuit for 5-volt products is shown in Figure 9. The inputs under test are driven by a pulse generator with a source impedance of 50\Omega. The output load consists of a 50pF capacitance (including jig and probe capacitance) and a resistor network. The 500\Omega resistance to ground normally consists of a 450\Omega discrete resistor in series with the 50\Omega impedance of the co-ax probe which offers very low capacitance for accurate measurements.
For all tests except $t_{PLZ}$ and $t_{PZL}$, the switch connected to the 7-volt supply is open. The AC load is the parallel combination of 50pF and 500Ω.

To perform the $t_{PHZ}$ and $t_{PZH}$ tests, the switch shown in Figure 9 is connected to the 7V supply. This creates an “artificial” logic HIGH level when the QuickSwitch is in the OFF state, so that output voltage transitions can occur during logic LOW to high-impedance state when the switch is undriven.

**Figure 9. AC Test Circuit for 5V Products**

For all tests except $t_{PLZ}$ and $t_{PZL}$, the switch connected to the 7-volt supply is open. The AC load is the parallel combination of 50pF and 500Ω.

To perform the $t_{PHZ}$ and $t_{PZH}$ tests, the switch shown in Figure 9 is connected to the 7V supply. This creates an “artificial” logic HIGH level when the QuickSwitch is in the OFF state, so that output voltage transitions can occur during logic LOW to high-impedance state when the switch is undriven.
QUICKSWITCH GENERAL INFORMATION

TEST CIRCUIT AND WAVEFORMS

INPUT CONDITIONS: Input Voltage = 0V to 3V, $t_{r} = 2.5\text{ns}$ (10% to 90%), $R_L = 500\Omega$, $C_L = 50pF$

LOAD SWITCH POSITION

<table>
<thead>
<tr>
<th>Parameter</th>
<th>S1 Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH, tPHL</td>
<td>Open</td>
</tr>
<tr>
<td>tPZH, tPHZ</td>
<td>Open</td>
</tr>
<tr>
<td>tPLZ, tPZL</td>
<td>Closed</td>
</tr>
</tbody>
</table>

NOTES:
1. $t_{PLH}$ and $t_{PHL}$: Data propagation delays through the switch when the Switch is ON.
2. $t_{PZH}$: The output goes from Hi-Z (Switch OFF) to a High State (Switch ON).
3. $t_{PZL}$: The output goes from Hi-Z (Switch OFF) to a Low State (Switch ON).
4. $t_{PLZ}$: The output goes from Low State (Switch ON) to a Hi-Z (Switch OFF).
5. $t_{PHP}$: The output goes from High State (Switch ON) to a Hi-Z (Switch OFF).
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades. "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   - **Standard**: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   - **High Quality**: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2019 Renesas Electronics Corporation. All rights reserved.