VERSACLOCK®LP APPLICATION NOTE FOR SMARTBOOKS, NETBOOKS, & E-BOOK READERS

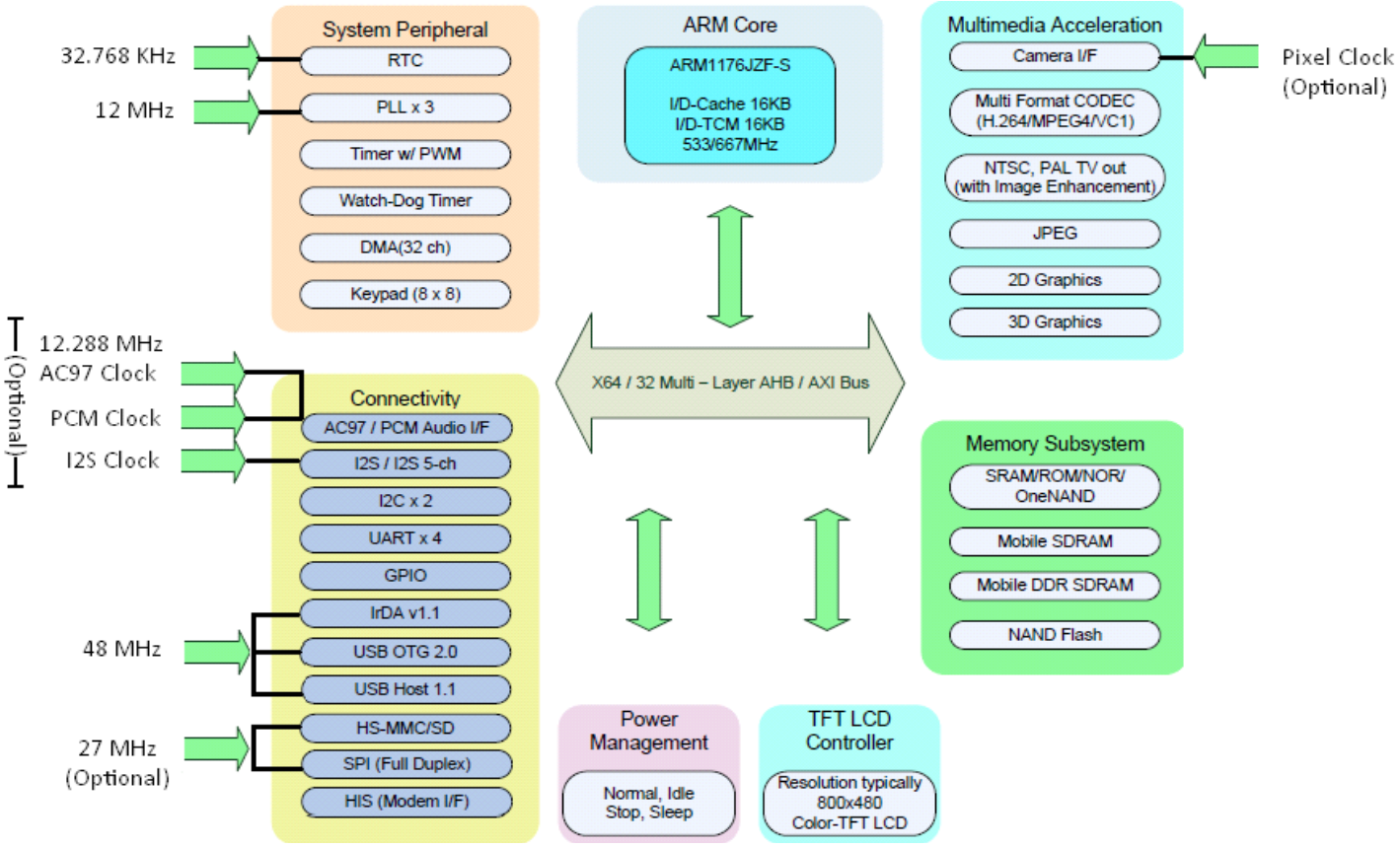
Introduction

Some of the growing application areas of the VersaClock®LP device are in Smartbooks, Netbooks and E-Book Readers. There are several discrete crystals and oscillators used in these systems that can potentially be replaced with a single clock synthesizer and buffer IC. This can lead to savings in power, board space and cost. This application note provides schematic and layout guidelines that should be considered while designing in the VersaClock®LP device in the above mentioned applications. It also provides an insight into the external clocking requirements of popular processors used in these systems.

External Clocking Needs of Popular Processors

The external clocking needs of 4 popular Netbook, Smartbook and E-book Reader processors are illustrated below.

Samsung 6410



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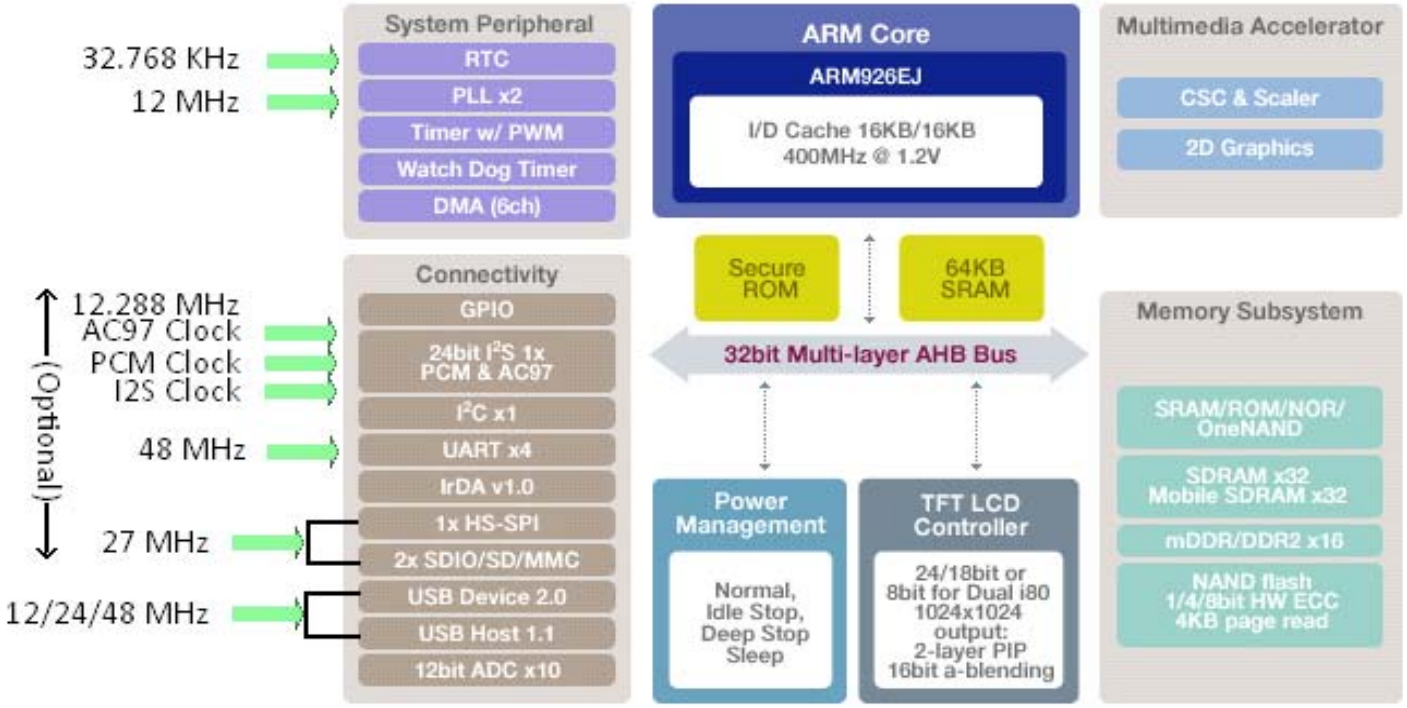
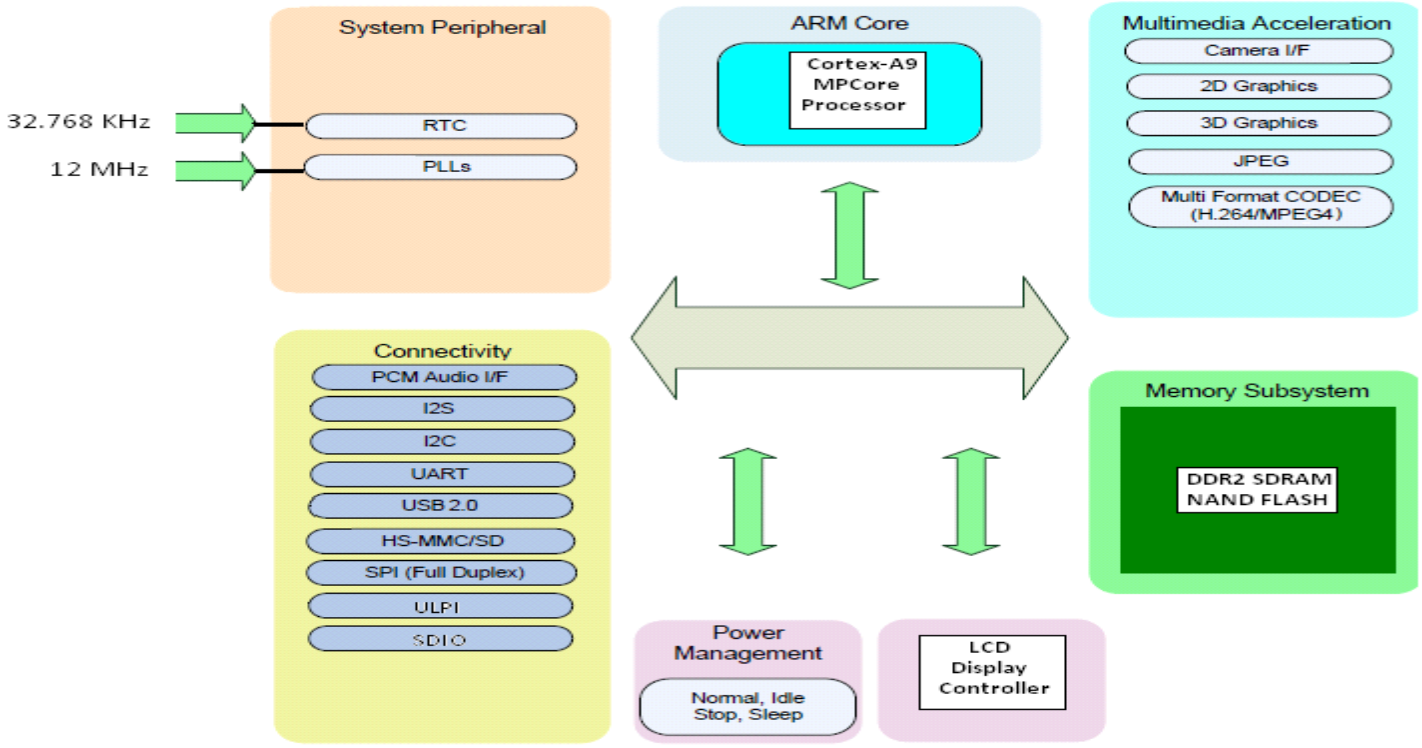
Samsung 2416



Nvidia T20



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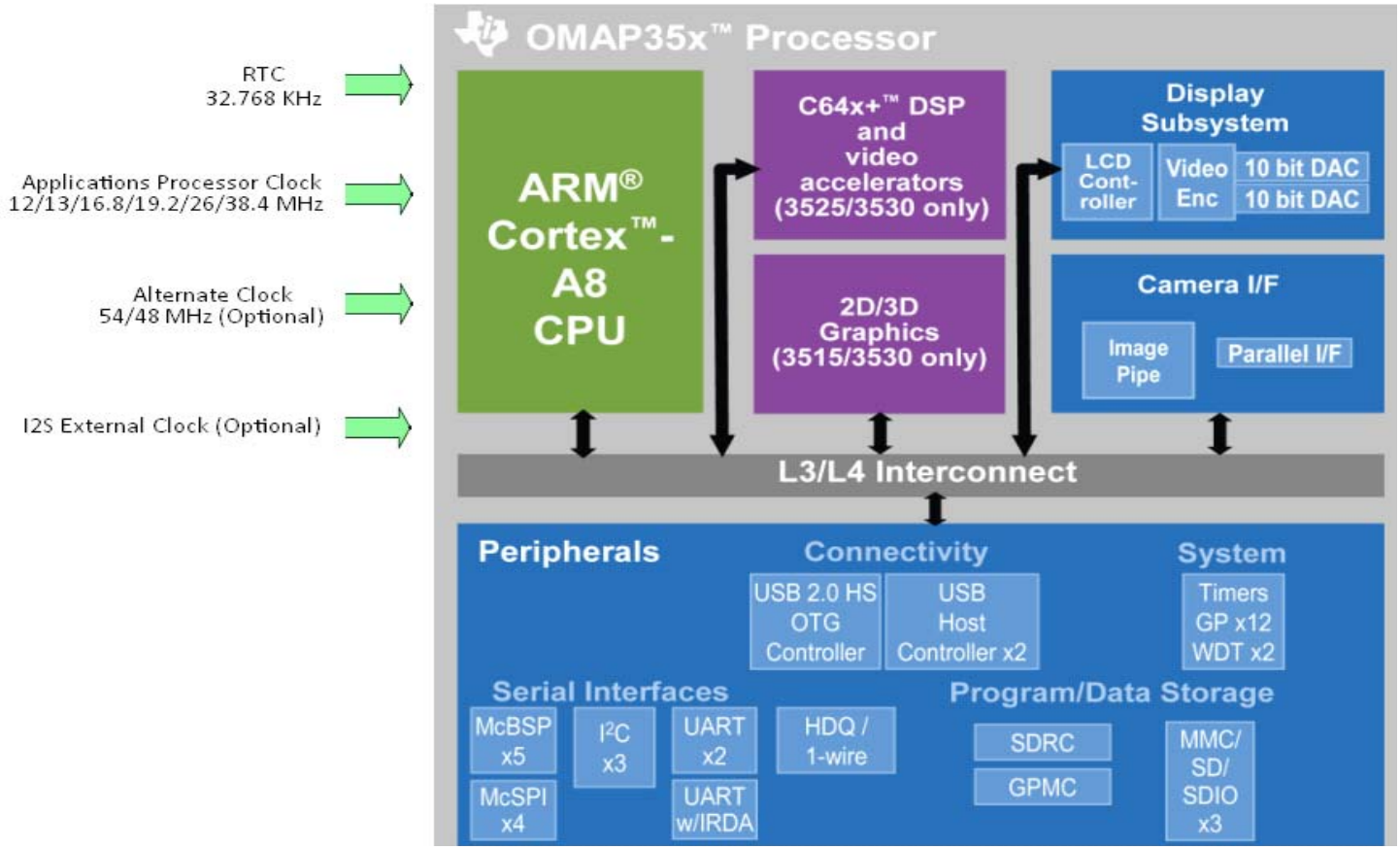
TI OMAP3530



Other than the frequency requirements of the processor, Smartbook, Netbook and E-book Readers may require additional frequencies for the applications listed below.

- LAN (25 MHz typical)
- Bluetooth/Wi-Fi (19.2 MHz / 26 MHz typical)
- GPS (16.368 MHz / 16.369 MHz/ 26 MHz typical)
- Low Power 32.768 kHz clock for PMIC, Bluetooth/Wi-Fi, Keyboard and Embedded Controller

The table in the following page lists the typical input and output frequency requirements in systems using the processors listed above. It also lists the optimal PLL divider and loop filter settings that would need to be set on the VersaClock LP device in order to synthesize the required output frequencies.

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Typical VersaClock LP Configurations

Processor	Input	Output Frequency	Output VDDO (Typical)	Application		PLL Parameters							
				Processor	Peripheral	Reference Divider	Feedback Divider	Output Divider	Ip(uA)	Rz(Kohms)	Cz(pF)	Cp(pF)	Damping Factor	Bandwidth (KHz)
Samsung 6410	24	12	1.8V-3.3V	Core		1	18	36	22.747	5	277	27	0.88	320
Samsung 2416		48	3.3V for 6410, 1.8V-3.3V for 2416	USB		1	18	9	22.747	5	277	27	0.88	320
		12.288	1.8V-3.3V	AC97		5	64	25	22.747	10	277	27	0.93	180
		25	1.8V/3.3V		LAN	2	25	12	22.747	5	277	27	0.75	230
	32.768	32.768	1.8V-3.3V	RTC		Buffered Output								
		32.768	3.3V		Bluetooth/Wi-Fi Chipset									
Nvidia T20	26	12	1.8V	Core		Buffered Output								
		26	1.8V		Wi-Fi Chipset									
		26	1.8V		Bluetooth Chipset	1	12	26	22.747	5	277	27	1	480
		25	1.8V/3.3V		LAN	2	25	13	22.747	5	277	27	0.75	230
	32.768	32.768	1.8V/3.3V		Embedded Controller	Buffered Output								
		32.768	1.8V	RTC	PMIC									
TI OMAP3530	26	26	1.8V	Core		Buffered Output								
		26	1.8V		Bluetooth/Wi-Fi Chipset									
		25	1.8V/3.3V		LAN	2	25	13	22.747	5	277	27	0.75	230
	32.768	32.768	1.8V/3.3V		Embedded Controller	Buffered Output								
		32.768	1.8V	RTC	PMIC									

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Input Crystal/Clock Selection

The following items need to be considered while selecting the reference crystal/clock source for the VersaClock LP device.

Frequency Accuracy

Different standards impose different requirements for the overall frequency accuracy of the reference clock. Some popular standards with their reference clock frequency accuracy requirements are summarized in the table below.

Standard	Frequency Accuracy Across Operating Temperature
Bluetooth	+/- 20 ppm
802.11a	+/- 20 ppm
802.11b/g	+/- 25 ppm
GPS	+/- 0.5 ppm
10/100 Ethernet	+/- 100 ppm
USB	+/- 500 ppm

In general, the frequency tolerance of the VersaClock LP device input clock/crystal should be selected such that the output clocks meet the overall frequency accuracy requirement for all target devices in the system.

Output Clock Phase Noise

The phase noise of the synthesized output clock from the VersaClock LP device depends on the operating bandwidth of the internal PLLs. It is often crucial for the bandwidth of these PLLs to be set optimally in order to keep the phase noise of the synthesized outputs low. The bandwidth of a PLL is often limited by the phase detector rate. Bluetooth, Wi-Fi and GPS ICs are particularly sensitive to the phase noise of the reference clock to their chipset. An ideal scenario would be to generate buffered copies of the VersaClock LP device reference clock and route them directly to these ICs, assuming they require similar reference clock frequencies. More often that not, these ICs are designed to work with multiple reference clock frequencies and finding a common operating frequency is often possible.

Select versions of the VersaClock LP device have a unity gain buffer that preserves the waveshape of the input reference clock and contributes negligible additive phase noise. Other frequencies could then be synthesized from this reference clock. USB and Ethernet Phy standards specify a maximum tolerable RMS filtered phase jitter specification for their reference clocks. Audio Codecs are sensitive to reference clock carrier to noise ratio in addition to phase noise. LCD controllers are sensitive to long term jitter on the reference clock while application processors are sensitive to short term cycle-cycle jitter. In general, for PLL synthesized output clocks, the higher the PLL phase detector rate, the higher is the permissible closed loop bandwidth of the PLL and lower is the overall phase noise and accumulated jitter. If possible, for phase noise critical applications, select an input frequency that will yield the highest phase detector frequency for the PLL.

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Crystal Specifications

The following are typical specifications when selecting a crystal to be used as input source to the VersaClock LP device:

MHz Crystal

Frequency	8 MHz – 30 MHz
Tolerance over Temperature	±5 PPM – ±50 PPM
Operating Mode	Fundamental (AT Cut)
Load Capacitance	20pF
ESR	50 ohms (max)
Operating Temperature	0 to 70°C
Power dissipation	1 mWatt (max)
Package	SMD Low Profile

Recommended Crystal Manufacturers	
Manufacturer	**Web URL**
Abracon	http://www.abracon.com/
PDI	http://www.pdixtal.com/
Hosonic	http://www.hosonic.com/
Pletronics	http://www.pletronics.com/
Fox	http://www.foxonline.com/

kHz Crystal

Frequency	32.758 kHz
Tolerance over Temperature	20 PPM (+/- .002%)
Operating Mode	Fundamental
Load Capacitance	6.0-8.0pF
ESR	65K ohms (max)
Operating Temperature	0 to 70°C
Power dissipation	0.1 µWatt (max)
Package	SMT (7 x 1.5 x 1.4 mm)

Recommended Crystal Manufacturers	
Manufacturer	**Web URL**
Epson Toyocom	http://www.epsontoyocom.co.jp/english/
Citizen	http://www.citizencrystal.com/khz.htm
Ecliptek	http://www.ecliptek.com/
ECS	http://www.ecsxtal.com/
Fox	http://www.foxonline.com/

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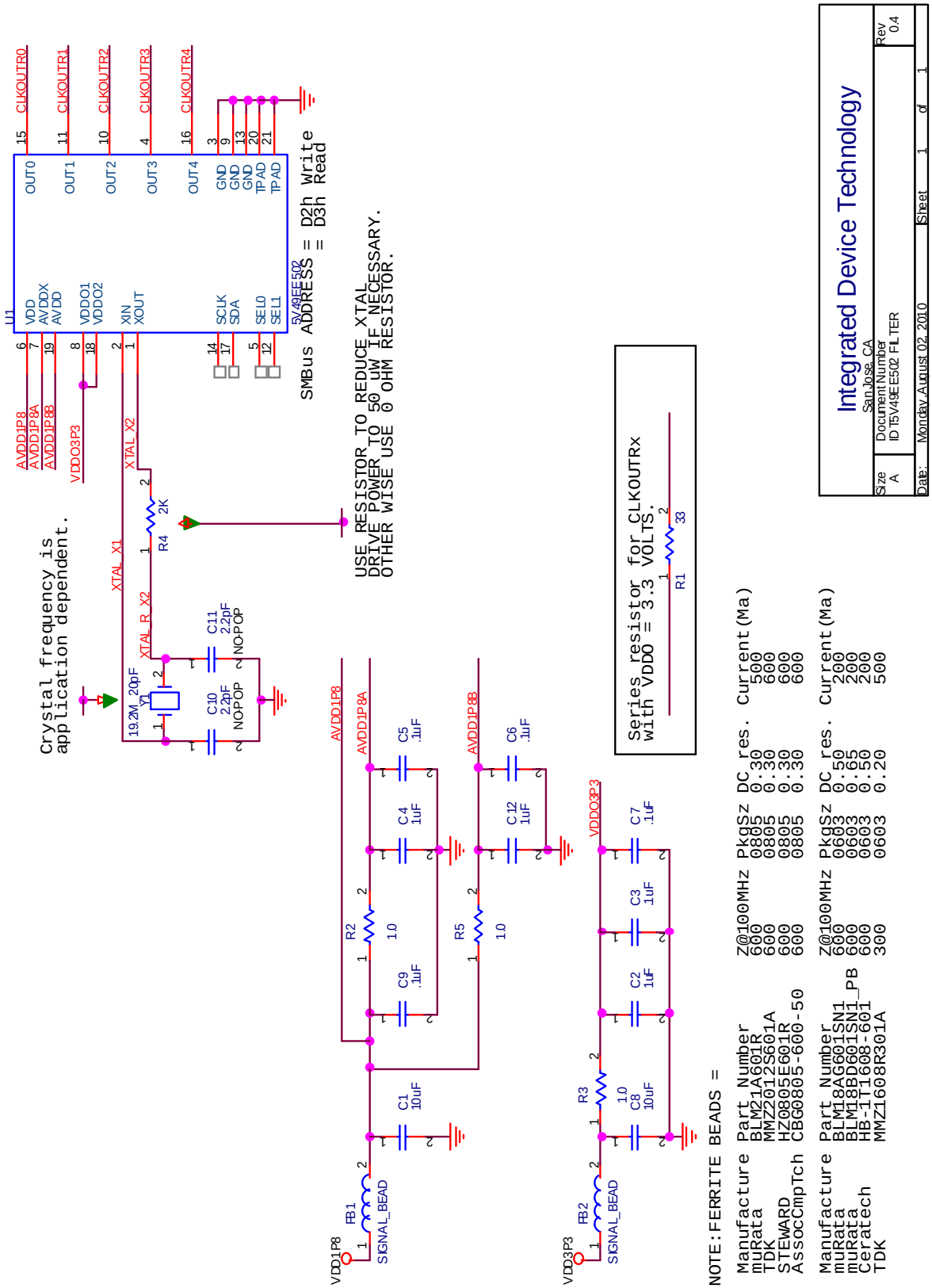
Recommended Schematic for IDT5P49EE502



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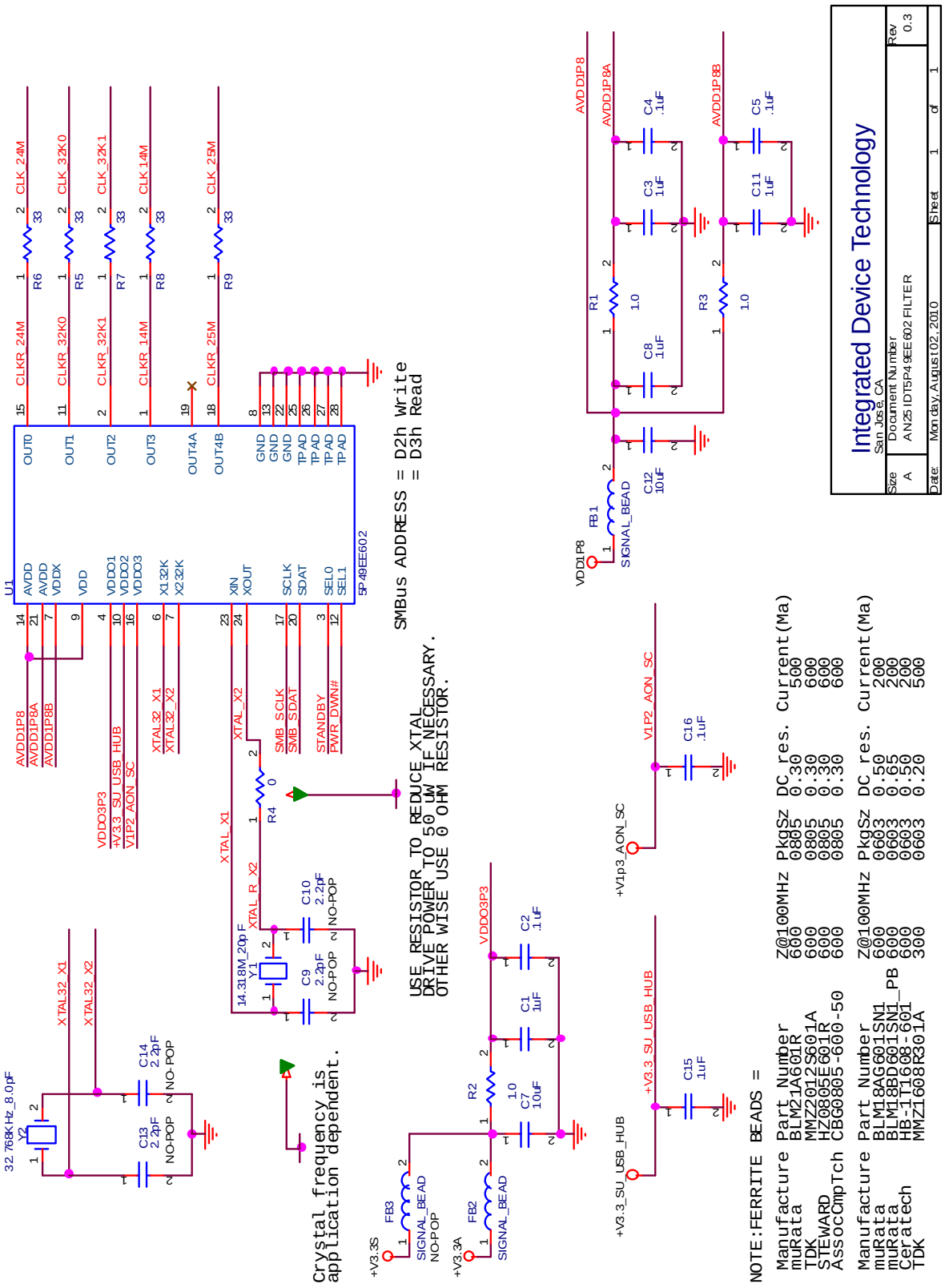
Recommended Schematic for IDT5P49EE602



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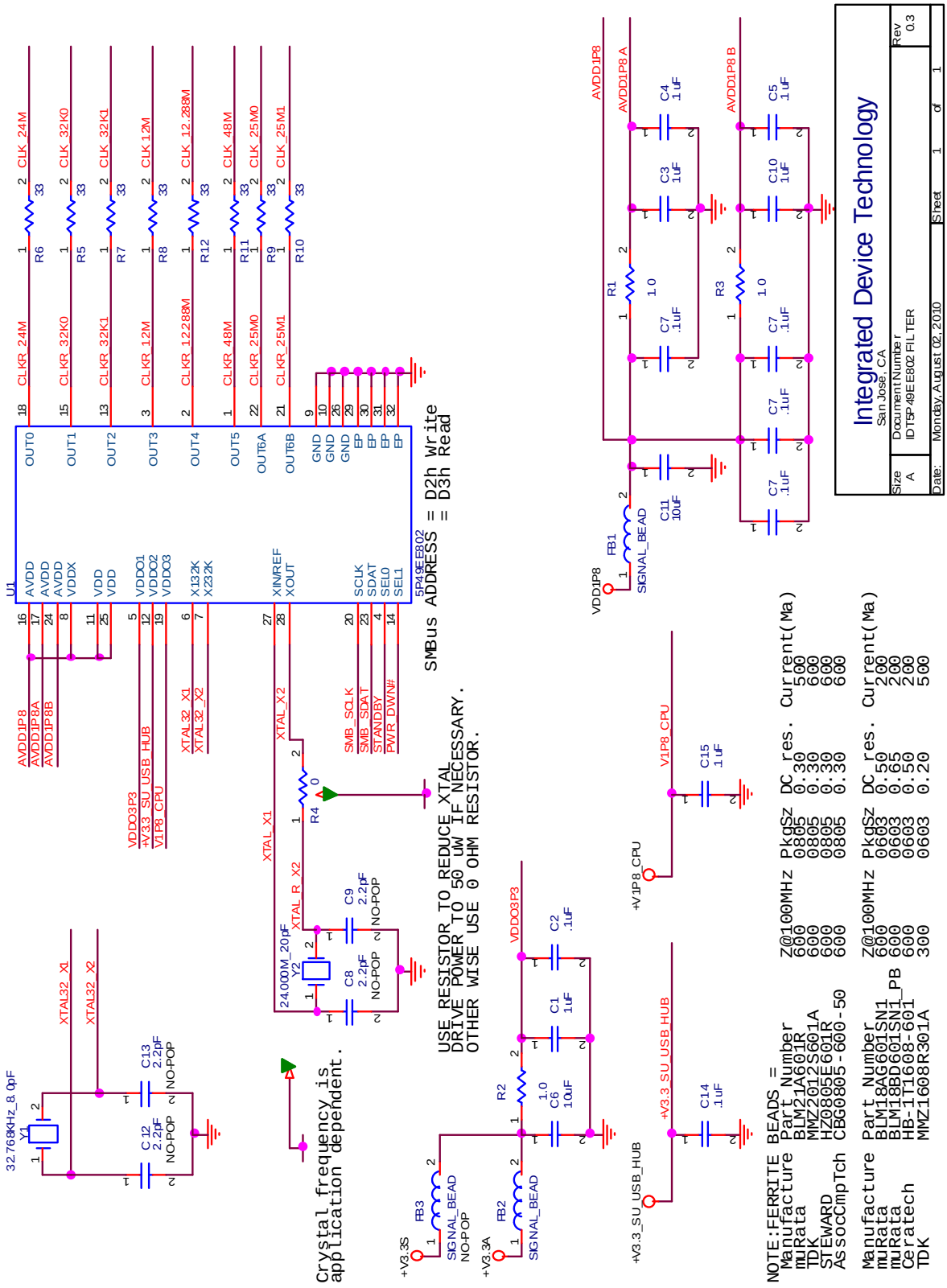
Recommended Schematic for IDT5P49EE802



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PCB Layout Guidelines

Clocking ICs with regular output transitions can be demanding on voltage and current distribution components such as power supplies, power buses and power planes. The power bus inductance often prevents the rapid energy transfer needed to keep up with the quick output transitions and fast rise/fall times. 0.1µF bypass capacitors placed right next to the VDD pins of the device (as recommended on the schematic) can greatly improve this situation by delivering the required energy in time. Care should be taken while selecting these capacitors.

Bypass Capacitor Selection and Placement

1) Choose a surface mount bypass capacitor (preferably ceramic X5R type) that has a low ESR, low ESL and low impedance at the frequency of interest.
2) Package sizes have an impact on the ESL of the capacitor as well. Choose a small package size '0402' for the bypass capacitor in order to keep the parasitic inductance as low as possible.
3) The length of the trace (if any) from the device power pin to the bypass capacitors should be kept as short as possible to keep the impedance of the bypass path low. The other end of the bypass capacitor is connected to a via going directly to the ground plane. The length of the trace (if any) from the capacitor to the via should be kept as short as possible.

The clock chip may also inject noise into the system power supply and vice versa. A low pass filter formed by a combination of a ferrite bead and capacitor (as recommended on the schematic) is often used to block power supply noise.

Low Pass Filter Component Selection and Placement

1) The Ferrite bead selected should have a maximum DC resistance between 0.4-0.8 ohms with a current rating of at least 200mA.
2) The Ferrite bead should have an impedance of 300 ohms or more at 100 MHz. Try to use a ferrite bead in '0603' package to reduce parasitics.
3) The Ferrite bead should not have a long inductive tail extending to low frequencies. Use the ferrite beads suggested on the schematic for reference.
4) The capacitor to ground should be placed right next to the ferrite bead in order to be effective. This capacitor delivers the power required for low frequency load surges.
5) Choose a 10µF MLCC capacitor for this purpose with low ESR and ESL.

Additionally, the Analog and Digital VDDs need to be isolated for optimal performance. Use an inexpensive resistor and capacitor as recommended on the schematic for this isolation. It is recommended to connect the VersaClock LP device VDDOs (Output Voltages) to the I/O power supply of the chipset that is receiving the clock synthesized from the output that the VDDO voltage controls. In order to minimize signal reflections, connect a 33 ohm series resistor on the outputs.

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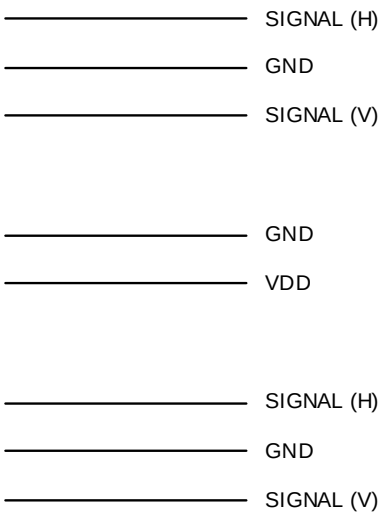
PCB Stack-up

PCB stack-up can impact the EMC performance of a product greatly. An ideal stack-up can be very effective in reducing the radiation from the loops on the PCB (differential mode emissions) as well as cables connected to the board (common-mode emissions). The five most critical objectives when selecting an ideal PCB stack-up are

1) Signal layers should always run adjacent to a power plane.
2) Signal layers should be tightly coupled to their reference planes.
3) Power and Ground planes should be closely coupled.
4) Critical signals should be routed on buried layers located between planes. The planes will then act as a shield and constrain the radiation.
5) Having multiple ground planes will lower the ground impedance of the board and reduce common mode radiation.

An 8-layer board can be used to satisfy all the above objectives. The preferred stack-up for an 8-layer board is shown below:



The above stack-up has a tightly coupled center power-ground plane for controlling common mode emissions. Critical signals can be routed on signal layers 3 or 6 and be effectively shielded by the planes. 'H' indicates horizontal routing for signals on Layers 1 and 6 while 'V' indicates vertical routing for signals on Layers 3 and 8. Orthogonal routing will help to minimize capacitive coupling between the signals on different layers. This configuration has the added advantage that orthogonal signals always reference the same plane. Typical layer spacing for a 0.060" thick board is 0.006"/0.006"/0.015"/0.006"/0.015"/0.006"/0.006.

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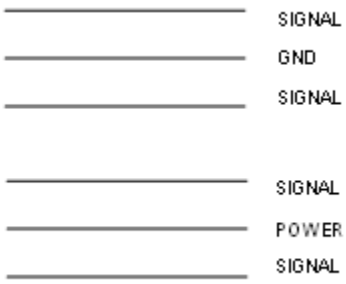
For 6-layer boards, the most common stack-up is shown below:



This stack-up is also fairly good in controlling emissions. The interplane capacitance between power and ground is not significant and external decoupling schemes explained earlier must be followed.

For 4-layer boards, stripling routing of critical signals is often not possible.

Signal Routing Guidelines

1) Maintain minimum separation of 3 times the clock trace width when routing signal traces adjacent to the clock trace.
2) Maintain minimum separation of 3 times the clock trace width from PCB edges and split planes when routing clock traces.
3) Do not route clock traces across plane splits.
4) If VersaClock LP device is mounted on the top side of the board, the best practice for routing clock traces stripline (for the 8-layer and 6-layer stack-up shown earlier) would be to connect the output series termination resistor (if used) directly to the VersaClock LP device output pins with a very short trace and no vias between the resistor and the device. On the other end of the resistor place a via to the signal layer on Layer 3. For unity gain buffer outputs an AC coupling capacitor can be connected directly to the output of the device at one end and a via to the signal layer on Layer 3 at the other end. When switching signal layers, always route to another signal layer that shares the same reference plane. For the 8-layer and 6-layer board stack-up shown earlier with the VersaClock LP device mounted on the top side, this would imply switching from signal layer on Layer 1 to signal layer on Layer 3 as both these layers have the reference plane (Gnd plane on Layer 2). Avoid routing to signal layers that are adjacent to a different plane.

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Errata

The following is the errata list for the VersaClock LP device (at the time this document was created):

- The rms crystal drive current for the MHz oscillator on the VersaClock LP device is around 3.7mA. This results in a power dissipation of around 343µW for a crystal with a typical series resistance of 25ohms. We recommend using a SMD low profile crystal with a power dissipation specification of 500µW or higher with this device.
- The internal load capacitance on XIN and XOUT is fixed to 32pF. This leads to an effective internal load capacitance of 16pF. Factoring in the input pad capacitance, the effective internal capacitance increases to around 18pF. We recommend using a MHz crystal with load capacitance rating of 20pF (accounting for PCB stray capacitance) with this device.
- We recommend using a 32.768 kHz crystal (if required) with 8pF load capacitance rating. The internal load capacitors on X132K and X232K need to be unbalanced to achieve 50% Duty Cycle on the output.
- The output impedance for outputs powered by VDDO = 1.8V is around 80 ohms. Running traces > 1 inch on a system board for outputs power by VDDO = 1.8V is not recommended from a signal integrity standpoint.
- The 32.768 kHz oscillator has a typical operating current of 35µA and the power down current of the VersaClock LP device is around 10µA.
- GPS and wireless module performance cannot be guaranteed with the synthesized clocks from VersaClock LP device.
- Please consult IDT if your jitter requirements are not met on any one of the VersaClock LP device output clocks when programmed with the software generated configuration file.

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(Rev.4.0-1 November 2017)

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