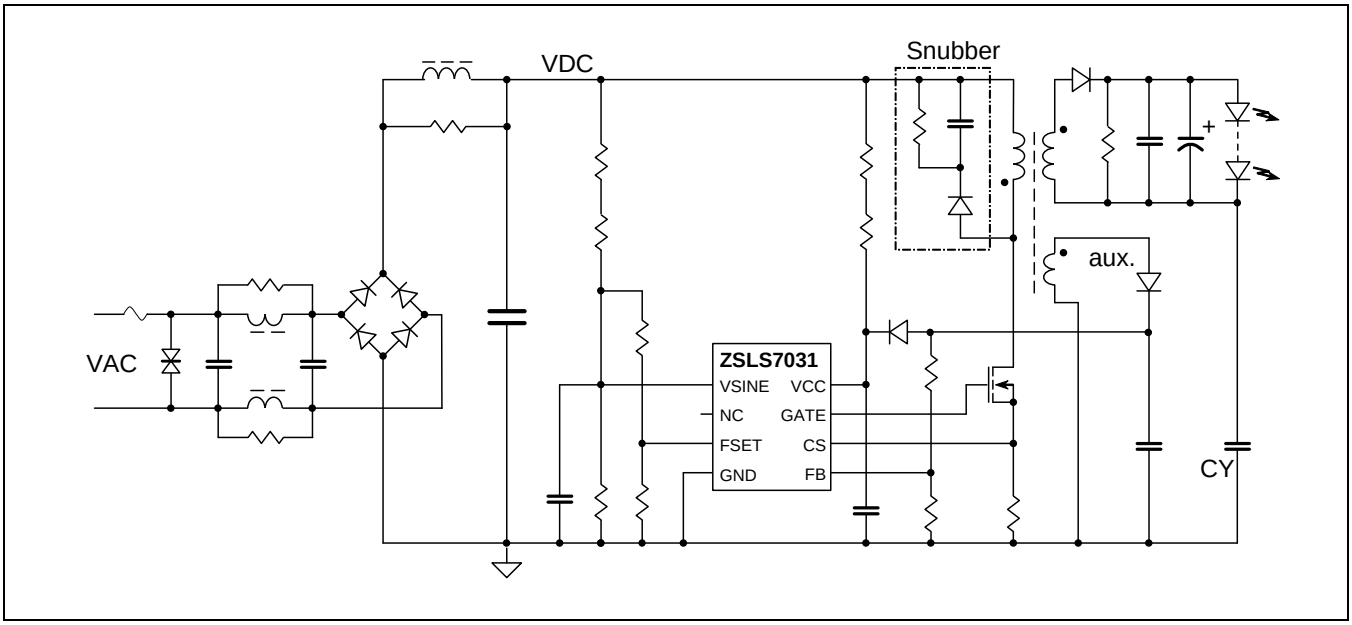
Contents

1 Introduction

This application note demonstrates the design process for a flyback converter using IDT's ZSLS7031 LED Driver IC. A typical application circuit is shown in Figure 1.1.

The flyback converter should always operate in discontinuous mode (DCM) to achieve optimal supply voltage compensation and the best power factor with minimized total harmonic distortions (THD). This leads to some constraints regarding transformer dimensioning. In order to simplify the calculations, the transformer is initially considered as "ideal"; i.e., it does not cause any losses (winding and core losses) and has no leakage inductance.

Figure 1.1 Typical LED Driver Application Circuit Using Flyback Topology



2 Dimensioning the Flyback Transformer

2.1 Winding Ratio and Flyback Voltage

The primary-over-secondary voltage ratio of the ideal transformer equals the winding ratio at any time as calculated in equation (1).

$$\frac{V_{prim}}{V_{sec}} = \frac{n_{prim}}{n_{sec}} \tag{1}$$

The path of the current flow of a flyback converter alternates between the primary and secondary, but on the transition from primary to secondary current flow and vice versa, the current ratio is inversely proportional to the winding ratio.

$$\frac{I_{sec}}{I_{prim}} = \frac{n_{prim}}{n_{sec}} \tag{2}$$

A low primary switching current is beneficial for achieving high efficiency; therefore a high winding ratio should be targeted. However, a high winding ratio causes high flyback voltage and thus high drain voltage for the switching transistor. It is good practice to dimension the maximum drain voltage to not exceed 75% of the transistor's drain voltage rating, including the "snubber voltage" overshoot, which will be discussed later.

A typical value for the flyback voltage V_{fb} (referenced to the momentary rectified line voltage VDC) in an off-line design is in the order of 100V, which gives a reasonable margin for the voltage rating of a 500 to 600 V or 700 to 800 V MOSFET in a 120VAC or 230VAC application, respectively. Once the V_{fb} has been defined, the winding ratio can be calculated from the LED forward voltage V_{LED} and the secondary rectifier diode forward voltage V_D using equation (3).

$$\frac{n_{prim}}{n_{sec}} = \frac{V_{fb}}{V_{LED}+V_D} \tag{3}$$

After the transformer dimensioning is complete and an appropriate core has been selected, the number of turns n can be calculated from the inductance L and the AL value given for the core using equation (4).

$$L = AL \times n^2 \quad \Rightarrow \quad n = \sqrt{\frac{L}{AL}} \tag{4}$$

2.2 Peak Switching Current and Primary Inductance

The best utilization of the transformer's magnetic core is achieved when the converter operates just "on the edge" of DCM under the worst-case conditions. Because the ZSLS7031 operates at a constant frequency and keeps the maximum switching current in every half line-cycle constant, the worst-case condition occurs when both the supply voltage and the load voltage (V_{LED}) are at their minimum. The rising and falling edges of the current are longest then and must fit into a single switching period $t_{SW} = 1/f_{SW}$.

In a power factor correction (PFC) design, i.e. when both line voltage and current have a sinusoidal shape, the momentary power is a sin² function. Normalized to amplitudes of 1, the result is equation (5):

$$sin^2(\omega t) = \frac{1}{2} - \frac{1}{2}\cos(2\omega t) \tag{5}$$

This is also a sinusoidal wave shape with twice the line frequency and a 50% offset. Its amplitude is 2 x the average value. This leads to the conditions needed for the calculation of the transformer's primary inductance.

Maximum power in the center of each half cycle is twice the average power, while voltage amplitude is $\sqrt{2}$ x VAC_{eff} where VAC_{eff} is the effective AC supply voltage. Consequently the worst-case line current amplitude can be determined with equation (6), where P_{AC} is the average input power of the converter.

$$I_{max} = \sqrt{2} \times \frac{P_{AC}}{VAC_{min}} \tag{6}$$

This current must be equal to the average primary current of the transformer in a single switching cycle. P_{AC} is higher than the LED power P_{LED} since overall efficiency is always $\eta < 100\%$.

$$P_{AC} = \frac{P_{LED}}{\eta} \tag{7}$$

A reasonable value to start calculations with is $\eta = 0.85$.

The next step is to define the switching frequency f_{SW}. Higher frequencies lead to a smaller transformer but also to higher switching losses ($P_{dyn} \sim f_{SW}$) and thus lower efficiency. A fundamental upper limit of f_{SW} is given by the minimum on-time of the power transistor, defined by the blanking time t_{blank}, which is typically 500ns. Typical applications operate at f_{SW} in the range of 50kHz to 100kHz.

Energy is stored in the magnetic core during the power transistor's on-time and transferred into the output during the off-time. Since the converter operates in DCM, there is no magnetic energy left at the end of each switching cycle. This leads to the maximum pulse energy in the center of one half-cycle:

$$E_{p,max} = \frac{2\,P_{AC}}{f_{sw}} \tag{8}$$

The energy stored in an inductor L equals

$$E_L = \frac{1}{2}\,L\,I^2 \tag{9}$$

Equations (8)and (9) must deliver the same result, therefore

$$\frac{2\,P_{AC}}{f_{sw}} = \frac{1}{2}\,L\,I^2 \;\Rightarrow\; L\,I^2 = \frac{4\,P_{AC}}{f_{sw}} \tag{10}$$

During the on-time of the power transistor, the VAC amplitude voltage drops across the primary inductance, while during off-time, the current decay is driven by the flyback voltage, which can be derived with equation (11).

$$\frac{di}{dt} = \frac{V}{L} \tag{11}$$

This results in

$$t_{on} = \frac{L_{prim} \times i_{sw,peak}}{\sqrt{2} \times VAC} \quad and \quad t_{off} = \frac{L_{prim} \times i_{sw,peak}}{V_{fb}} \tag{12}$$

The ratio of t_{on}/t_{off} is given by the inverse voltage ratio during t_{on} and t_{off}.

$$\frac{t_{on}}{t_{off}} = \frac{V_{fb}}{\sqrt{2} \times VAC} \quad where\ t_{on} + t_{off} \leq t_{sw} = \frac{1}{f_{sw}} \tag{13}$$

In a typical application, t_{on} is shorter than t_{off} at the line voltage amplitude.

Under worst-case conditions, $t_{on} + t_{off} = t_{SW}$ is assumed. Simplifying $\sqrt{2}$ x VAC to the amplitude voltage V_a gives equation (14).

$$t_{off} = t_{on} \times \frac{V_a}{V_{fb}} \Rightarrow t_{sw} = t_{on} \times \left(1 + \frac{V_a}{V_{fb}}\right) \Rightarrow t_{on} = t_{sw} \times \frac{V_{fb}}{V_a + V_{fb}} \tag{14}$$

During t_{on} the current can be assumed to increase linearly. The average current is thus half the peak current $i_{sw,peak}$. The average current i_{av} over a full switching cycle t_{SW} is then given by equation (15),

$$i_{av} = \frac{1}{2}\, i_{sw,peak} \times d \tag{15}$$

where the duty cycle *d* is given under worst-case conditions as

$$d = \frac{t_{on}}{t_{sw}} = \frac{V_{fb,min}}{V_{a,min} + V_{fb,min}} \tag{16}$$

Substituting equation (16) into (15) and taking into considering that i_{av} must be equal to the line current amplitude I_{max} yields equation (17).

$$i_{sw,peak} = 2 \times \frac{I_{max}}{d} = 2\, I_{max} \times \frac{V_{a,min} + V_{fb,min}}{V_{fb,min}} \tag{17}$$

With I_{max} x $V_{a,min}$ = 2 P_{AC}, equation (18) is derived.

$$i_{sw,peak} = 4\, P_{AC} \times \frac{V_{a,min} + V_{fb,min}}{V_{a,min} \times V_{fb,min}} \tag{18}$$

During t_{on} the pulse energy given in equation (8) must be stored in the magnetic core. This leads to the transformer's primary inductance L_{prim} being

$$L_{prim} = t_{on} \times \frac{V_{a,min}}{i_{sw,peak}} = t_{sw} \times \frac{V_{fb,min}}{V_{a,min} + V_{fb,min}} \times \frac{V_{a,min}}{i_{sw,peak}} \Rightarrow \tag{19}$$

$$L_{prim} = \frac{t_{sw}}{i_{sw,peak}} \times \frac{V_{a,min} \times V_{fb,min}}{V_{a,min} + V_{fb,min}}$$

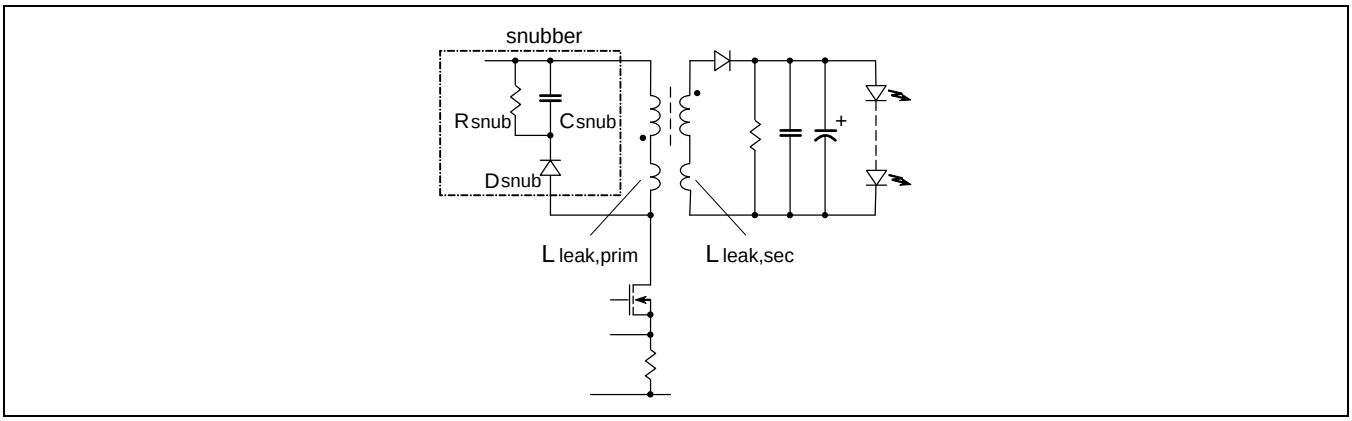
Substituting (18) into (19) yields

$$L_{prim} = \frac{t_{sw}}{4\,P_{AC}} \times \left(\frac{V_{a,min} \times V_{fb,min}}{V_{a,min} + V_{fb,min}} \right)^2 \quad (20)$$

2.3 Leakage Inductance and Snubber Network

A real transformer shows primary and secondary leakage inductance, which is not “linked” to the respective other side, i.e. current driven into the primary leakage inductance cannot continue flowing in the secondary and vice versa. In the electrical-equivalent diagram of a transformer, the leakage inductances $L_{leak,prim}$ and $L_{leak,sec}$ are connected in series with the main winding inductance on each side as shown in Figure 2.1.

Figure 2.1 Electrical-Equivalent Transformer with Primary and Secondary Leakage Inductances



Consequently, when the peak switching current is reached and the transistor is turned off, $L_{leak,prim}$ causes the primary current to continue flowing, while $L_{leak,sec}$ prevents the secondary current from abruptly starting to flow. The primary current charges the parasitic node capacitance on the transistor’s drain up to its breakdown voltage. To avoid this repetitive stress condition, a snubber network consisting of a capacitor, a resistor, and a diode is added, limiting the voltage to a level below the drain breakdown (see Figure 1.1 and Figure 2.1). The capacitor is typically several nF and large enough to absorb the single pulse energy without significant voltage increase. The resistor discharges the capacitor continuously and must dissipate the average power that is fed into the snubber capacitor. The snubber voltage must be higher than the flyback voltage V_{fb}, because V_{fb} is still present after the energy from the leakage inductance has been transferred.

The higher the snubber voltage V_{snub} is, the faster the current in the leakage inductor decays, thus reducing the average current into the snubber capacitor. Since V_{fb} is always superimposed, a higher V_{snub} reduces the power dissipation of the snubber resistor. However, it also increases the P_{diss} of the power transistor because drain current continues flowing up to the higher V_{snub}. In this situation, transient transistor losses are inversely proportional to the switching speed.

Numerical calculation of the snubber resistor and its losses is complex. A simplified approach will be used here to establish a good starting point for the optimization. It disregards the fact that on the rising edge of the power transistor's drain voltage (i.e., switching the transistor off), there is already energy transferred from the leakage inductance into the parasitic node capacitance and the transistor, conducting in linear mode.

The peak switching current flow is the same in the primary inductance and primary leakage inductance. Current commutation from primary to secondary is limited by the decay of current in the primary and by the increase in the secondary leakage inductance. At the end of the transistor's drain voltage rising edge, the difference between V_{snub} and V_{fb} drops across the primary and transformed secondary leakage inductances, virtually connected in series. Advantageously, this sum is exactly what is being measured when shorting the secondary and measuring the remaining inductance on the primary side. The resulting L_{leak} can be calculated with equation (21):

$$L_{leak} = L_{leak,prim} + \left(\frac{n_{prim}}{n_{sec}}\right)^2 \times L_{leak,sec} \tag{21}$$

The primary current decay is thus given by equation (22).

$$\frac{di_{leak}}{dt} = \frac{V_{snub} - V_{fb}}{L_{leak}} \tag{22}$$

Assuming current decay to be linear over the decay time t_{decay}, this leads to the average current driven into the snubber network:

$$I_{sn,av} = \frac{1}{2}\, I_{peak} \times \frac{t_{decay}}{t_{sw}} = \frac{1}{2}\, I_{peak} \times \frac{I_{peak}}{\frac{di_{leak}}{dt}} \times f_{sw}$$

$$I_{sn,av} = \frac{1}{2}\, I^2{}_{peak} \times \frac{L_{leak}}{V_{snub} - V_{fb}} \times f_{sw} \tag{23}$$

Power dissipation of the snubber resistor can therefore be calculated as

$$P_{diss,sn} = I_{sn,av} \times V_{snub} = \left[\frac{1}{2}\, I^2{}_{peak} \times L_{leak} \times f_{sw}\right] \times \frac{V_{snub}}{V_{snub} - V_{fb}} \tag{24}$$

where the term in brackets is the average power stored in the leakage inductance. It is obvious that the snubber network must dissipate this power as a minimum.

The snubber resistor can be calculated from equation (24) by considering the conditions at the AC voltage peak where V_{snub} is highest and the momentary power is twice the average (2 x P_{AC}). The power stored in the leakage inductance becomes

$$P_{leak,max} = 2\, P_{AC} \times \frac{L_{leak}}{L_{prim}} \tag{25}$$

and therefore

$$P_{diss,max} = 2\,P_{AC} \times \frac{L_{leak}}{L_{prim}} \times \frac{V_{snub}}{V_{snub} - V_{fb}} \tag{26}$$

giving the value of the resistor R_{snub} in the snubber network:

$$R_{snub} = \frac{V^2_{snub}}{P_{snub}} = \frac{V^2_{snub}}{2\,P_{AC} \times \frac{L_{leak}}{L_{prim}} \times \frac{V_{snub}}{V_{snub} - V_{fb}}} = \frac{V_{snub} \times (V_{snub} - V_{fb})}{2\,P_{AC} \times \frac{L_{leak}}{L_{prim}}} \tag{27}$$

V_{snub} should be as high as possible for low snubber losses, but a high V_{snub} also requires a high voltage rating and causes higher losses in the power transistor. A reasonable compromise is to assume that V_{snub} is (2 to 2.5) x V_{fb} in the center of the sine wave (e.g., V_{snub} = 200 to 250 V above VDC when V_{fb} = 100 V). This leads to the peak power dissipation of the snubber resistor being 2 to 1.65 times the power stored in L_{leak}.

The average power dissipation of the snubber resistor can be estimated by assuming the power wave shape to be a sinusoidal curve with its maximum as defined above and the minimum given by the flyback voltage dropping across R_{snub} when the line voltage crosses zero. This leads to equation (28).

$$P_{diss,av}(R_{snub}) = P_{min} + \frac{1}{2}\,(P_{max} - P_{min}) = \frac{1}{2}\,(P_{max} + P_{min})$$

$$P_{diss,av}(R_{snub}) = \frac{1}{2} P_{diss,max} \left[1 + \left(\frac{V_{fb}}{V_{snub}}\right)^2\right] \tag{28}$$

As mentioned previously, this derivation neglects the energy reduction in the leakage inductance during the rising edge of the power transistor's drain voltage. This amount is not negligible, and in a typical application can be considered to be in the order of 30%. The snubber resistor should therefore be chosen to be 40% higher than calculated, while its power dissipation can be considered 30% lower. Final optimization must be done on the actual application circuit.

Low leakage inductance of the transformer is essential for good efficiency of the flyback converter. In order to keep L_{leak} and the related power dissipation low, it is advantageous to interleave primary and secondary windings. This might not be simple if a high isolation voltage (e.g., 4kV) is required. A common approach is to split the primary into two layers with half the total number of turns each and place the secondary between the two layers, with a sufficient isolation layer on its top and bottom. A slightly better result can be achieved when splitting the secondary and placing the primary between the two layers. In many cases, the secondary voltage is lower than the primary, while the current is higher. If so, it makes sense to split the secondary into two layers with the full number of turns each and connect them in parallel externally.

Splitting the secondary has an additional advantage: an auxiliary winding on the transformer is often used to supply the controller IC during operation and also provide information about the output voltage; e.g., for overvoltage shutdown. The auxiliary winding gives a much better image of the output voltage when it is not placed in close proximity with the primary, but rather with the secondary as a type of shield between the auxiliary and primary windings. Typically the load current of the auxiliary winding is low (a few mA), and the "shield" avoids peak rectifying the snubber ringing coupled from the primary.

2.4 Transformer Core Dimensioning

Primarily for cost reasons, the transformer is often realized using an E-E type ferrite core with a center air gap. The pulse energy is primarily stored in the air gap since for a given flux density, the specific energy (energy per volume) of a magnetic field is inversely proportional to the magnetic permeability μ.

$$\rho_m = \frac{B^2}{2\,\mu} \tag{29}$$

Typical ferrite materials saturate at flux densities between 300mT and 350mT, so a reasonable maximum operational flux should not exceed 250mT (2500G). The air gap's permeability is nearly the same as the vacuum permeability μ_0 ($\mu_r \approx 1$).

$$\mu_0 = 4\,\pi \times 10^{-7}\ \left[\frac{V\,s}{A\,m}\right] \tag{30}$$

With the pulse energy E_p, the required air gap volume V_{ag} is given by equation (31).

$$V_{ag} = \frac{2\,E_p\,\mu_0}{B^2}\ [m^3] \tag{31}$$

For simplification, equation (32) can be used, providing a result in mm³ rather than m³:

$$V_{ag} = \frac{2513\,E_p}{B^2}\ [mm^3] \tag{32}$$

The further assumption of B_{max} = 250mT (= 0.25T) results in equation (33)

$$V_{ag} = 40208\,E_p\ [mm^3] \tag{33}$$

Alternatively, equation (34) can be used as a rule of thumb.

$$V_{ag} \approx 40\ \frac{mm^3}{mWs} \tag{34}$$

2.5 Auxilliary Winding

The transformer contains an auxiliary winding that is used to supply the ZSLS7031 during operation and also provide a voltage feedback for output open-load (overvoltage) protection. The number of turns for this voltage should be chosen to achieve an output voltage V_{CC} = 12 to 14 V at nominal LED voltage using equation (35).

$$\frac{n_{aux}}{n_{sec}} = \frac{V_{CC}}{V_{LED}} \tag{35}$$

3 Dimensioning the Buck-Boost Inductor

The buck-boost converter can be considered as a special case of the flyback converter where the transformer's primary/secondary ratio equals 1 and the secondary is simply left out, which of course sacrifices isolation. This topology is advantageous in terms of efficiency when the LED voltage is reasonably high; i.e., in the region where the flyback voltage would be with a transformer present. Since a single inductor does not have leakage inductance, a snubber dissipating the related energy is not needed.

Considering this, all equations for calculating the transformer's primary inductance in a flyback converter are valid for a buck-boost inductor also by simply assuming the following.

$$n_{prim} = n_{sec},\ I_{prim} = I_{sec},\ V_{fb} = V_{LED} + V_D \tag{36}$$

The operating supply current for the ZSLS7031 in a buck-boost converter can be provided from an auxiliary winding on the inductor, making it a transformer again (but without the need for a snubber), or by an alternative supply concept described in the *ZSLS7031 Application Note—230VAC Buck-Boost Converter for 45 LEDs*.

4 Related Documents

Document
ZSLS7031 Data Sheet
ZSLS7031 Application Note—230VAC Buck-Boost Converter for 45 LEDs.

Visit the ZSLS7031 product page at www.IDT.com/ZSLS7031 or contact your nearest sales office for the latest version of these documents.

5 Glossary

Term	Description
DCM	Discontinuous Mode
FB	Feedback
PFC	Power Factor Correction
THD	Total Harmonic Distortion

6 Document Revision History

Revision	Date	Description
1.00	April 28, 2014	First release.
	April 20, 2016	Changed to IDT branding.

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