Contents

List of Figures

List of Tables

1. Introduction

The ZSSC4151 Sensor Signal Conditioner IC is available in a RoHS-compliant QFN24 package (4mm x 4mm; wettable flanks). See the *ZSSC4151 Feature Sheet* for additional options. This document provides details for package dimensions, pin assignments and layout, footprint, board connections, package marking, and thermal resistance.

2. QFN24 (4x4mm) Package Marking

Table 2.1 QFN24 Package Marking

Top Side		Comments
1st Line	4151	4151E = Product name
2nd Line	YYWW	YY = Year (e.g., 14 for 2014, 15 for 2015, ...); WW = Workweek (e.g., 15)
3rd Line	XXXXX	Last five digits of IDT lot number

3. ZSSC4151 Pin Assignments and Layout

Figure 3.1 shows the ZSSC4151 pin assignments and layout. This pin layout enables implementation of the recommended printed circuit board (PCB) design in which the external signals (VDDE, VSSE, and AOUT) are not routed close to or crossing sensitive input signals from the sensor(s). Table 3.1 shows the pin assignments of the QFN24 (4x4mm) package.

Figure 3.1 Pin Layout for the ZSSC4151

Package QFN24 (4x4mm)

The underside of the package
(the “exposed pad”)
is electrically connected
to the potential VSSA.

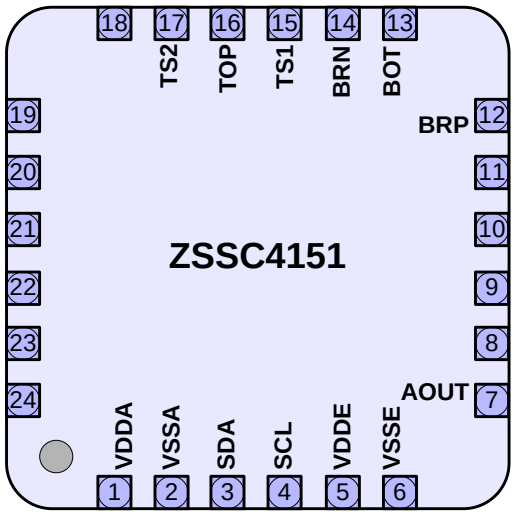


Table 3.1 Pin Assignments – QFN24 (4x4mm)

Pin No QFN24	Pin Name	Description	Notes
1	VDDA	Positive analog supply voltage	Internal analog power supply
2	VSSA	Negative analog supply voltage	Internal analog ground
3	SDA	I²C™* data I/O	Analog I/O, internal pull-up
4	SCL	I²C™ clock	Analog input, internal pull-up
5	VDDE	Positive external supply voltage	Power supply, protected up to ±40V
6	VSSE	External ground	Ground, protected up to ±40V
7	AOUT	Ratiometric analog output and OWI	Analog I/O, protected up to ±40V
8	n.c.	No connection – unused	
9	n.c.	No connection – unused	
10	n.c.	No connection – unused	
11	n.c.	No connection – unused	
12	BRP	Positive sensor input	Analog input
13	BOT	Negative bridge supply voltage	Analog I/O
14	BRN	Negative sensor input	Analog input
15	TS1	External temperature sensor 1	Analog input
16	TOP	Positive bridge supply voltage	Analog I/O
17	TS2	External temperature sensor 2	Analog input
18	n.c.	No connection – unused	
19	n.c.	No connection – unused	
20	n.c.	No connection – unused	
21	n.c.	No connection – unused	
22	n.c.	No connection – unused	
23	n.c.	No connection – unused	
24	n.c.	No connection – unused	
25	EPad	Exposed pad – internally connected to VSSA	Ground – should be shorted externally to VSSA (pin 2)

* I²C™ is a trademark of NXP.

4. QFN24 (4x4mm) Thermal Resistance Value

The QFN24 (4x4mm) package has a junction-to-ambient θ_{JA} of 31.8 °C/W.

θ_{JA} has been simulated in accordance to following JEDEC-standards:

- Test Board Design as per JESD51-7.
- Natural Convection Test Conditions as per JESD51-2.

Parameter	Symbol	Value	Unit
Thermal Resistance – junction to ambient	θ_{JA}	31.8	°C/W

5. QFN24 (4x4mm) Package Dimensions

Figure 5.1 and Table 5.1 show the package drawing and parameters for the ZSSC4151 QFN24 (4x4mm) package based on JEDEC MO-220. Dimensions are in millimeters.

Figure 5.1 Dimensions QFN24 (4x4mm)

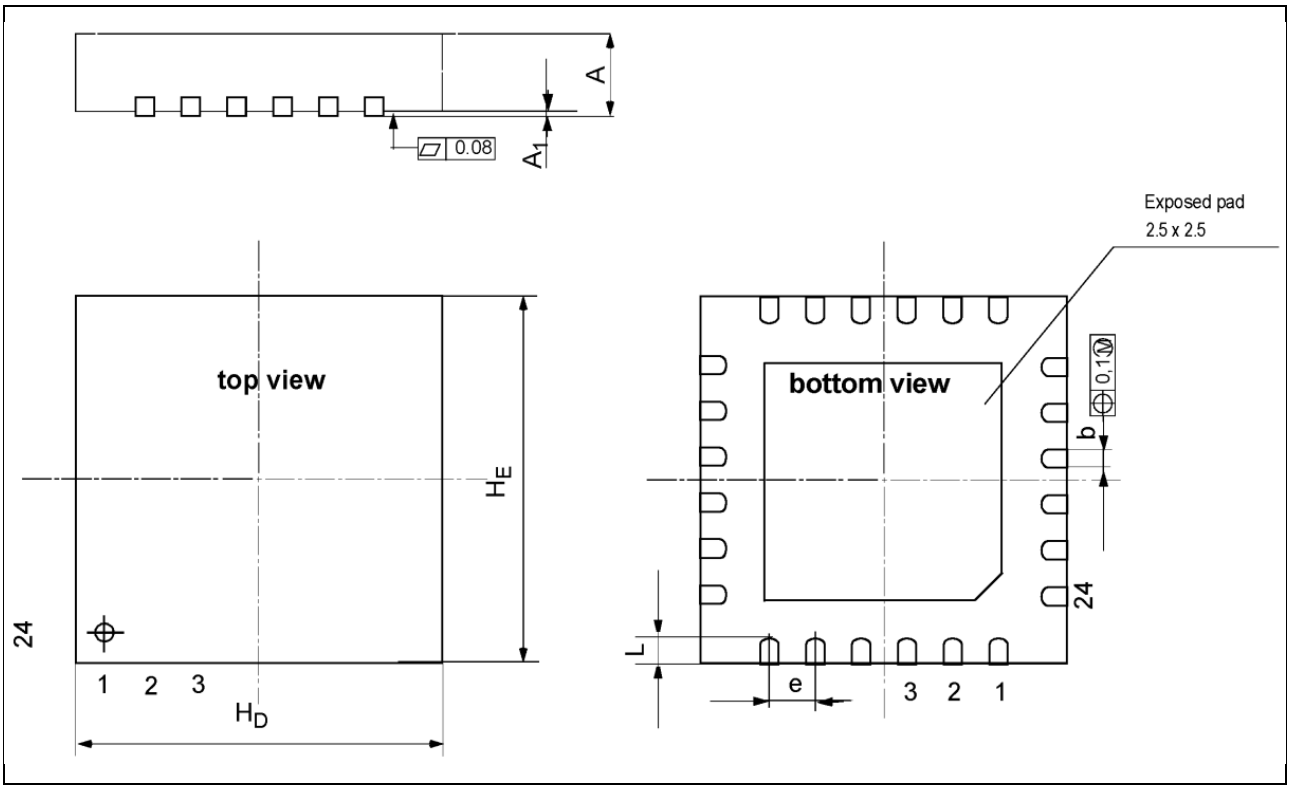


Table 5.1 QFN24 Dimensions (4x4mm)

Dimension Limit	MIN	NOM	MAX
A	0.80		0.90
A1	0.00		0.05
b	0.20		0.30
e		0.50	
H_D	3.90		4.10
H_E	3.90		4.10
L	0.30		0.50

6. QFN24 (4x4mm) Footprint and Wettable Flank Description

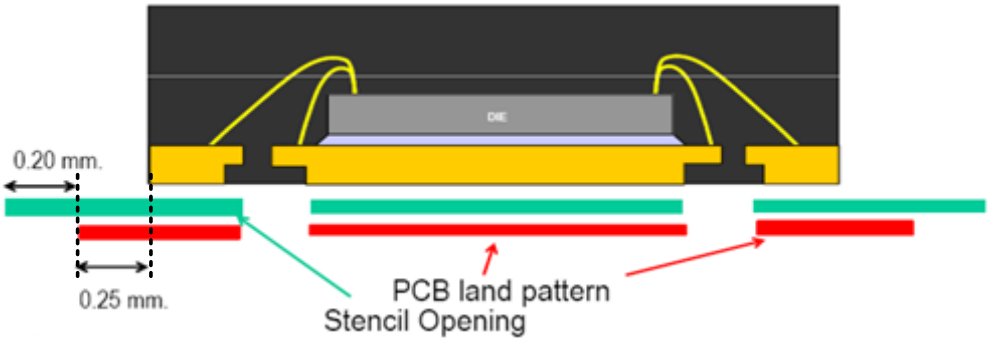
Figure 6.1 illustrates the general concept of the wettable flank (side plating) allows automatic optical inspection.

Figure 6.1 Wettable Flank General Concept

Figure 6.2 illustrates a suggested footprint for PCB designs using the ZSSC4151 QFN24 (4x4mm) package.

- The exposed area of the landing pattern is 0.25mm from the unit edge.
- The stencil opening excess is approximately 0.2mm from the landing pattern.

Figure 6.2 Footprint Dimensions for QFN24 with Wettable Flanks



7. Related Documents

Document
ZSSC4151 Data Sheet
ZSSC4151 Feature Sheet
ZSSC4151 Functional Description
ZSSC4151 Application Note—Power Management

Visit the ZSSC415x product page http://www.idt.com/ZSSC4151 or contact your nearest sales office for the latest version of these documents.

8. Glossary

Term	Description
PCB	Printed Circuit Board
QFN	Quad Flat No Leads Package
SSC	Sensor Signal Conditioner

9. Document Revision History

Revision	Date	Description
1.00	September 9, 2015	First release.
	April 1, 2016	Changed to IDT branding.

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