

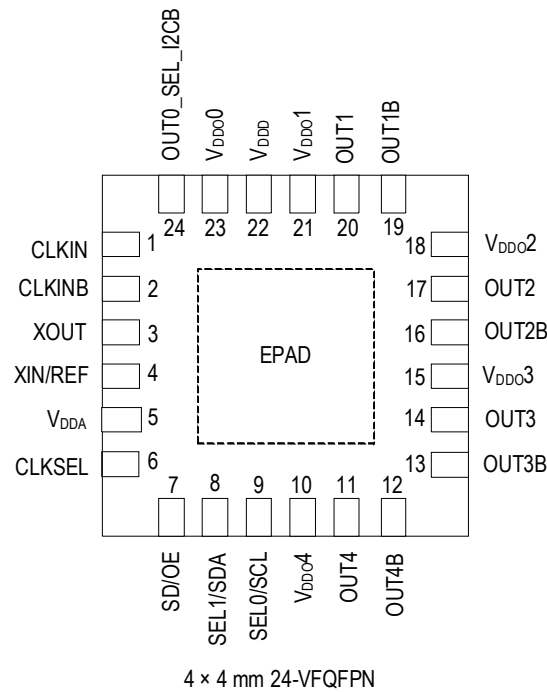


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## Pin Assignments

Figure 1. Pin Assignments for 4 x 4 mm 24-VFQFPN Package – Top View



## Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type		Description
1	CLKIN	Input	Internal Pull-down	Differential clock input. Weak 100kΩ internal pull-down.
2	CLKINB	Input	Internal Pull-down	Complementary differential clock input. Weak 100kΩ internal pull-down.
3	XOUT	Output		Crystal oscillator interface output.
4	XIN/REF	Input		Crystal oscillator interface input, or single-ended LVCMOS clock input. Input voltage needs to be below 1.2V. Refer to the section <a href="#">Driving XIN/REF with a CMOS Driver</a> .
5	V <sub>DDA</sub>	Power		Analog functions power supply pin. Connect to 1.8V to 3.3V. V <sub>DDA</sub> and V <sub>DD0</sub> should have the same voltage applied.
6	CLKSEL	Input	Internal Pull-down	Input clock select. Selects the active input reference source in manual switchover mode. 0 = XIN/REF, XOUT (default). 1 = CLKIN, CLKINB. See <a href="#">Table 20. Input Clock Select</a> for more details.
7	SD/OE	Input	Internal Pull-down	Enables/disables the outputs (OE) or powers down the chip (SD).
8	SEL1/SDA	Input	Internal Pull-down	Configuration select pin, or I <sup>2</sup> C SDA input as selected by OUT0_SEL_I2CB. Weak internal pull-down resistor.
9	SEL0/SCL	Input	Internal Pull-down	Configuration select pin, or I <sup>2</sup> C SCL input as selected by OUT0_SEL_I2CB. Weak internal pull-down resistor.

**Table 1. Pin Descriptions (Cont.)**

Number	Name	Type		Description
10	V <sub>DDO4</sub>	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT4/OUT4B.
11	OUT4	Output		Output clock 4. Refer to the <a href="#">Output Drivers</a> section for more details.
12	OUT4B	Output		Complementary output clock 4. Refer to the <a href="#">Output Drivers</a> section for more details.
13	OUT3B	Output		Complementary output clock 3. Refer to the <a href="#">Output Drivers</a> section for more details.
14	OUT3	Output		Output clock 3. Refer to the <a href="#">Output Drivers</a> section for more details.
15	V <sub>DDO3</sub>	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT3/OUT3B.
16	OUT2B	Output		Complementary output clock 2. Refer to the <a href="#">Output Drivers</a> section for more details.
17	OUT2	Output		Output clock 2. Refer to the <a href="#">Output Drivers</a> section for more details.
18	V <sub>DDO2</sub>	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT2/OUT2B.
19	OUT1B	Output		Complementary output clock 1. Refer to the <a href="#">Output Drivers</a> section for more details.
20	OUT1	Output		Output clock 1. Refer to the <a href="#">Output Drivers</a> section for more details.
21	V <sub>DDO1</sub>	Power		Output power supply. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT1/OUT1B.
22	V <sub>DDD</sub>	Power		Digital functions power supply pin. Connect to 1.8 to 3.3V. V <sub>DDA</sub> and V <sub>DDD</sub> should have the same voltage applied.
23	V <sub>DDO0</sub>	Power		Power supply pin for OUT0_SEL_I2CB. Connect to 1.8 to 3.3V. Sets output voltage levels for OUT0.
24	OUT0_SEL_I2CB	Input/ Output	Internal Pull-down	Latched input/LVCMOS output. At power-up, the voltage at the pin OUT0_SEL_I2CB is latched by the part and used to select the state of pins 8 and 9. If a weak pull-up (10kΩ) is placed on OUT0_SEL_I2CB, pins 8 and 9 will be configured as hardware select pins, SEL1 and SEL0. If a weak pull-down (10kΩ) is placed on OUT0_SEL_I2CB or it is left floating, pins 8 and 9 will act as the SDA and SCL pins of an I <sup>2</sup> C interface. After power-up, the pin acts as an LVCMOS reference output.
25	GND	GND		Connect to ground pad.

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 2. Absolute Maximum Ratings**

Item	Rating
Supply Voltage, $V_{DDA}$ , $V_{DDD}$ , $V_{DDO}$	3.6V.
XIN/REF Input	1.2V.
CLKIN, CLKINB Input	$V_{DDO0}$ , 1.2V voltage swing.
I <sup>2</sup> C Loading Current	10mA.
Storage Temperature, $T_{STG}$	-65°C to 150°C.
Junction Temperature	125°C
ESD Human Body Model	2000V.

## Thermal Characteristics

**Table 3. Thermal Characteristics**

Symbol	Parameter	Value	Units
$\theta_{JA}$	Theta $J_A$ . Junction to air thermal impedance (0mps).	42	°C/W
$\theta_{JB}$	Theta $J_B$ . Junction to board thermal impedance (0mps).	2.35	°C/W
$\theta_{JC}$	Theta $J_C$ . Junction to case thermal impedance (0mps).	41.8	°C/W

## Recommended Operating Conditions

**Table 4. Recommended Operating Conditions**

Symbol	Parameter	Minimum	Typical	Maximum	Units
$V_{DDOX}$	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
$V_{DDD}$	Power supply voltage for core logic functions.	1.71		3.465	V
$V_{DDA}$	Analog power supply voltage. Use filtered analog power supply.	1.71		3.465	V
$T_{PU}$	Power ramp time for all $V_{DDs}$ to reach 90% of $V_{DD}$ .	0.05		50	ms
$T_A$	Operating temperature, ambient.	-40		85	°C
$C_L$	Maximum load capacitance (3.3V LVCMOS only).			15	pF

## Electrical Characteristics

**Table 5. Current Consumption**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ .

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$I_{DDCORE}^1$	Core Supply Current	100MHz on all outputs, 25MHz REFCLK.		33	42	mA
$I_{DDOx}$	Output Buffer Supply Current	LVPECL, 350MHz, 3.3V $V_{DDOx}^2$ .		45	58	mA
		LVPECL, 350MHz, 2.5V $V_{DDOx}^2$ .		36	47	mA
		LVDS, 350MHz, 3.3V $V_{DDOx}^2$ .		26	32	mA
		LVDS, 350MHz, 2.5V $V_{DDOx}^2$ .		25	30	mA
		LVDS, 350MHz, 1.8V $V_{DDOx}^2$ .		22	27	mA
		HCSL, 250MHz, 3.3V $V_{DDOx}^2$ .		39	48	mA
		HCSL, 250MHz, 2.5V $V_{DDOx}^2$ .		37	46	mA
		LVC MOS, 50MHz, 3.3V, $V_{DDOx}^{2,3}$ .		22	27	mA
		LVC MOS, 50MHz, 2.5V, $V_{DDOx}^{2,3}$ .		20	24	mA
		LVC MOS, 50MHz, 1.8V, $V_{DDOx}^{2,3}$ .		17	21	mA
		LVC MOS, 200MHz, 3.3V $V_{DDOx}^{2,3}$ .		43	56	mA
		LVC MOS, 200MHz, 2.5V $V_{DDOx}^{2,3}$ .		33	43	mA
		LVC MOS, 200MHz, 1.8V $V_{DDOx}^{2,3}$ .		24	31	mA
$I_{DDPD}$	Power Down Current	SD asserted, I <sup>2</sup> C programming.		10	12	mA

<sup>1</sup>  $I_{DDCORE} = I_{DDA} + I_{DDD}$ .

<sup>2</sup> Measured into a 5" 50Ω trace. See Test Loads section for more details.

<sup>3</sup> Single CMOS driver active.

**Table 6. AC Timing Characteristics**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$F_{IN}^1$	Input Frequency	Input frequency limit (crystal).	8		40	MHz
		Input frequency limit (CLKIN,CLKINB).	1		350	MHz
		Input frequency limit (single-ended over XIN).	1		200	MHz
$F_{OUT}^2$	Output Frequency	Single-ended clock output limit (LVCMOS), individual FOD mode.	1		200	MHz
		Differential clock output limit (LVPECL/LVDS/HCSL), individual FOD mode.	1		350	
		Single-ended clock output limit (LVCMOS), cascaded FOD mode, output 2–4.	0.001		200	
		Differential clock output limit (LVPECL/LVDS/HCSL), cascaded FOD mode, output 2–4.	0.001		350	
$f_{VCO}$	VCO Operating Frequency Range		2500		2900	MHz
$T_{DC}^3$	Output Duty Cycle	Measured at $V_{DD}/2$ , all outputs except reference output, $V_{DDOX} = 2.5V$ or $3.3V$ .	45	50	55	%
		Measured at $V_{DD}/2$ , all outputs except reference output, $V_{DDOX} = 1.8V$	40	50	60	%
		Measured at $V_{DD}/2$ , reference output OUT0 (5MHz–150.1MHz) with 50% duty cycle input.	40	50	60	%
		Measured at $V_{DD}/2$ , reference output OUT0 (150.1MHz–200MHz) with 50% duty cycle input.	30	50	70	%
$T_{SKEW}$	Output Skew	Skew between the same frequencies, with outputs using the same driver format and phase delay set to 0ns.		75		ps
$T_{STARTUP}^{4,5}$	Startup Time	Measured after all $V_{DD}$ s have risen above 90% of their target value <sup>6</sup> .			30	ms
		PLL lock time from shutdown mode.		3	4	ms

<sup>1</sup> Practical lower frequency is determined by loop filter settings.

<sup>2</sup> A slew rate of 2.75V/ns or greater should be selected for output frequencies of 100MHz or higher.

<sup>3</sup> Duty cycle is only guaranteed at maximum slew rate settings.

<sup>4</sup> Actual PLL lock time depends on the loop configuration.

<sup>5</sup> Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM programming/write time.

<sup>6</sup> Power-up with temperature calibration enabled; contact Renesas if shorter lock-time is required in system.

**Table 7. General Input Characteristics**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$C_{IN}$	Input Capacitance	CLKIN,CLKINB,CLKSEL,SD/OE,SEL1/SD A, SEL0/SCL.		3	7	pF
$R_{PD}$	Pull-down Resistor	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL, CLKIN, CLKINB, OUT0_SEL_I2CB.	100		300	kΩ
$V_{IH}$	Input High Voltage	CLKSEL, SD/OE.	$0.7 \times V_{DDD}$		$V_{DDD} + 0.3$	V
$V_{IL}$	Input Low Voltage	CLKSEL, SD/OE.	GND - 0.3		$0.3 \times V_{DDD}$	V
$V_{IH}$	Input High Voltage	OUT0_SEL_I2CB.	1.7		$V_{DDO0} + 0.3$	V
$V_{IL}$	Input Low Voltage	OUT0_SEL_I2CB.	GND - 0.3		0.4	V
$V_{IH}$	Input High Voltage	XIN/REF.	0.8		1.2	V
$V_{IL}$	Input Low Voltage	XIN/REF.	GND - 0.3		0.4	V
$T_R/T_F$	Input Rise/Fall Time	CLKSEL, SD/OE, SEL1/SDA, SEL0/SCL.			300	ns

**Table 8. CLKIN Electrical Characteristics**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{SWING}$	Input Amplitude – CLKIN, CLKINB	Peak to peak value, single-ended.	200		1200	mV
dv/dt	Input Slew Rate – CLKIN, CLKINB	Measured differentially.	0.4		8	V/ns
$I_{IL}$	Input Leakage Low Current	$V_{IN} = GND$ .	-5		5	μA
$I_{IH}$	Input Leakage High Current	$V_{IN} = 1.7V$ .			20	μA
$DC_{IN}$	Input Duty Cycle	Measurement from differential waveform.	45		55	%



**Table 9. Electrical Characteristics – CMOS Outputs**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage	$I_{OH} = -15mA (3.3V), -12mA (2.5V).$	$0.7 \times V_{DDO}$		$V_{DDO}$	V
		$I_{OH} = -8mA (1.8V).$	$0.5 \times V_{DDO}$		$V_{DDO}$	V
$V_{OL}$	Output Low Voltage	$I_{OL} = 15mA (3.3V), 12mA (2.5V), 8mA (1.8V).$			0.45	V
$R_{OUT}$	Output Driver Impedance	CMOS output driver.		17		$\Omega$
$T_{SR}$	Slew Rate, SLEW[1:0] = 00	Single-ended 3.3V LVCMOS output clock rise and fall time, 20% to 80% of $V_{DDO}$ (output load = 5pF) $V_{DDOX} = 3.3V.$	1.0	2.2		V/ns
	Slew Rate, SLEW[1:0] = 01		1.2	2.3		
	Slew Rate, SLEW[1:0] = 10		1.3	2.4		
	Slew Rate, SLEW[1:0] = 11		1.7	2.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 2.5V LVCMOS output clock rise and fall time, 20% to 80% of $V_{DDO}$ (output load = 5pF) $V_{DDOX} = 2.5V.$	0.6	1.3		
	Slew Rate, SLEW[1:0] = 01		0.7	1.4		
	Slew Rate, SLEW[1:0] = 10		0.6	1.4		
	Slew Rate, SLEW[1:0] = 11		1.0	1.7		
	Slew Rate, SLEW[1:0] = 00	Single-ended 1.8V LVCMOS output clock rise and fall time, 20% to 80% of $V_{DDO}$ (output load = 5pF) $V_{DD} = 1.8V.$	0.3	0.7		
	Slew Rate, SLEW[1:0] = 01		0.4	0.8		
	Slew Rate, SLEW[1:0] = 10		0.4	0.9		
	Slew Rate, SLEW[1:0] = 11		0.7	1.2		
$I_{OZDD}$	Output Leakage Current (OUT1–4)	Tri-state outputs.			5	$\mu A$
	Output Leakage Current (OUT0)	Tri-state outputs.			30	$\mu A$

**Table 10. Electrical Characteristics – LVDS Outputs**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$  unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
$V_{OT (+)}$	Differential Output Voltage for the TRUE Binary State	247		454	mV
$V_{OT (-)}$	Differential Output Voltage for the FALSE Binary State	-454		-247	mV
$\Delta V_{OT}$	Change in $V_{OT}$ between Complimentary Output States			50	mV
$V_{OS}$	Output Common Mode Voltage (Offset Voltage) at 3.3 V $\pm 5\%$ , 2.5V $\pm 5\%$	1.125	1.25	1.375	V
	Output Common Mode Voltage (Offset Voltage) at 1.8V $\pm 5\%$	0.8	0.875	0.96	V
$\Delta V_{OS}$	Change in $V_{OS}$ between Complimentary Output States			50	mV
$I_{OS}$	Outputs Short Circuit Current, $V_{OUT+}$ or $V_{OUT-} = 0V$ or $V_{DDO}$		9	24	mA
$I_{OSD}$	Differential Outputs Short Circuit Current, $V_{OUT+} = V_{OUT-}$		6	12	mA
$T_R$	LVDS rise time 20%–80%		300		ps
$T_F$	LVDS fall time 80%–20%		300		ps

**Table 11. Electrical Characteristics – LVPECL Outputs**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, T_A = -40^\circ C$  to  $+85^\circ C$  unless stated otherwise.

Symbol	Parameter	Minimum	Typical	Maximum	Units
$V_{OH}$	Output Voltage High, Terminated through $50\Omega$ tied to $V_{DD} - 2V$	$V_{DDO} - 1.19$		$V_{DDO} - 0.69$	V
$V_{OL}$	Output Voltage Low, Terminated through $50\Omega$ tied to $V_{DD} - 2V$	$V_{DDO} - 1.94$		$V_{DDO} - 1.4$	V
$V_{SWING}$	Peak-to-Peak Differential Output Voltage Swing	1.1		2	V
$T_R$	LVPECL rise time 20%–80%		400		ps
$T_F$	LVPECL fall time 80%–20%		400		ps

**Table 12. Electrical Characteristics – HCSL Outputs <sup>1</sup>**

$V_{DDA}, V_{DDD}, V_{DDO0} = 3.3V \pm 5\%, 2.5V \pm 5\%, T_A = -40^\circ C$  to  $+85^\circ C$  unless stated otherwise.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
dV/dt	Slew Rate	Scope averaging on <sup>2,3</sup> .	1		4	V/ns
$\Delta V/dt$	Slew Rate Matching	Scope averaging on <sup>2,3</sup> .			20	%
$V_{MAX}$	Maximum Voltage	Measurement on single-ended signal using absolute value (scope averaging off).			1150	mV
$V_{MIN}$	Minimum Voltage		-300			mV
$V_{SWING}$	Voltage Swing	Scope averaging off <sup>2,6</sup> .	300			mV
$V_{CROSS}$	Crossing Voltage Value	Scope averaging off <sup>4,6</sup> .	250		550	mV
$\Delta V_{CROSS}$	Crossing Voltage Variation	Scope averaging off <sup>5</sup> .			140	mV

<sup>1</sup> Guaranteed by design and characterization. Not 100% tested in production.

<sup>2</sup> Measured from differential waveform.

<sup>3</sup> Slew rate is measured through the  $V_{SWING}$  voltage range centered around differential 0V. This results in a  $\pm 150mV$  window around differential 0V.

<sup>4</sup>  $V_{CROSS}$  is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>5</sup> The total variation of all  $V_{CROSS}$  measurements in any particular system. Note that this is a subset of  $V_{CROSS}$  min/max ( $V_{CROSS}$  absolute) allowed. The intent is to limit  $V_{CROSS}$  induced modulation by setting  $\Delta V_{CROSS}$  to be smaller than  $V_{CROSS}$  absolute.

<sup>6</sup> Measured from single-ended waveform.

**Table 13. Spread Spectrum Generation Specifications**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$f_{SSOUT}$	Spread Frequency	Output frequency range for spread spectrum.	5		300	MHz
$f_{MOD}$	Mod Frequency	Modulation frequency.	30 to 63			kHz
$f_{SPREAD}$	Spread Value	Amount of spread value (programmable)–center spread.	$\pm 0.1\%$ to $\pm 2.5\%$			% $f_{OUT}$
		Amount of spread value (programmable)–down spread.	-0.2% to -5%			

## I<sup>2</sup>C Bus Characteristics

**Table 14. I<sup>2</sup>C Bus (SCL/SDA) DC Characteristics**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V <sub>IH</sub>	Input High Level	For SEL1/SDA pin and SEL0/SCL pin.	0.7 × V <sub>DDD</sub>			V
V <sub>IL</sub>	Input Low Level	For SEL1/SDA pin and SEL0/SCL pin.			0.3 × V <sub>DDD</sub>	V
V <sub>HYS</sub>	Hysteresis of Inputs		0.05 × V <sub>DDD</sub>			V
I <sub>IN</sub>	Input Leakage Current		-1		36	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 3mA.			0.45	V

**Table 15. I<sup>2</sup>C Bus (SCL/SDA) AC Characteristics**

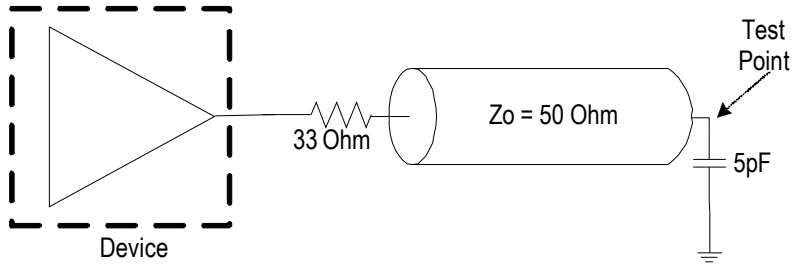
Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
F <sub>SCLK</sub>	Serial Clock Frequency (SCL)	—	10		400	kHz
t <sub>BUF</sub>	Bus Free Time between Stop and Start	—	1.3			μs
t <sub>SU:START</sub>	Setup Time, Start	—	0.6			μs
t <sub>HD:START</sub>	Hold Time, Start	—	0.6			μs
t <sub>SU:DATA</sub>	Setup Time, Data Input (SDA)	—	0.1			μs
t <sub>HD:DATA</sub>	Hold Time, Data Input (SDA) <sup>1</sup>	—	0			μs
t <sub>OVD</sub>	Output Data Valid from Clock	—			0.9	μs
C <sub>B</sub>	Capacitive Load for Each Bus Line	—			400	pF
t <sub>R</sub>	Rise Time, Data and Clock (SDA, SCL)	—	20 + 0.1 × C <sub>B</sub>		300	ns
t <sub>F</sub>	Fall Time, Data and Clock (SDA, SCL)	—	20 + 0.1 × C <sub>B</sub>		300	ns
t <sub>HIGH</sub>	High Time, Clock (SCL)	—	0.6			μs
t <sub>LOW</sub>	Low Time, Clock (SCL)	—	1.3			μs
t <sub>SU:STOP</sub>	Setup Time, Stop	—	0.6			μs

<sup>1</sup> A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V<sub>IH(MIN)</sub> of the SCL signal) to bridge the undefined region of the falling edge of SCL.

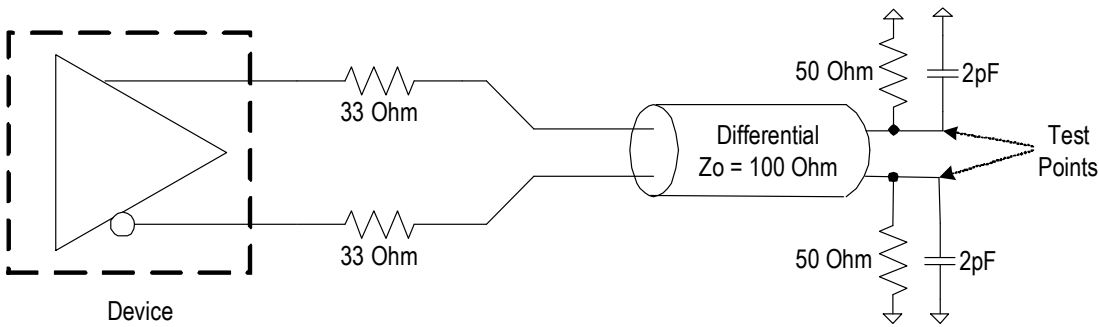
<sup>2</sup> I<sup>2</sup>C inputs are 3.3V tolerant.

## Test Loads

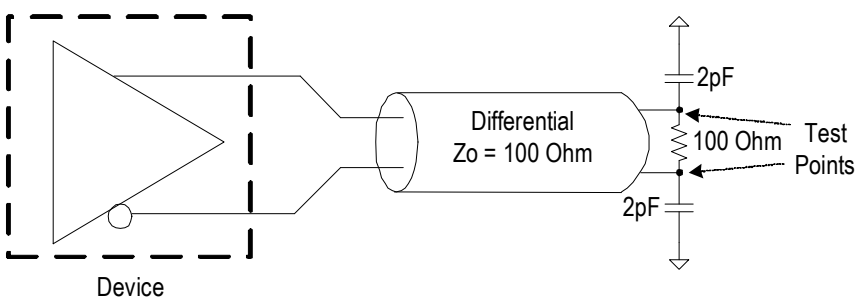
**Figure 2. LVCMOS Test Load**



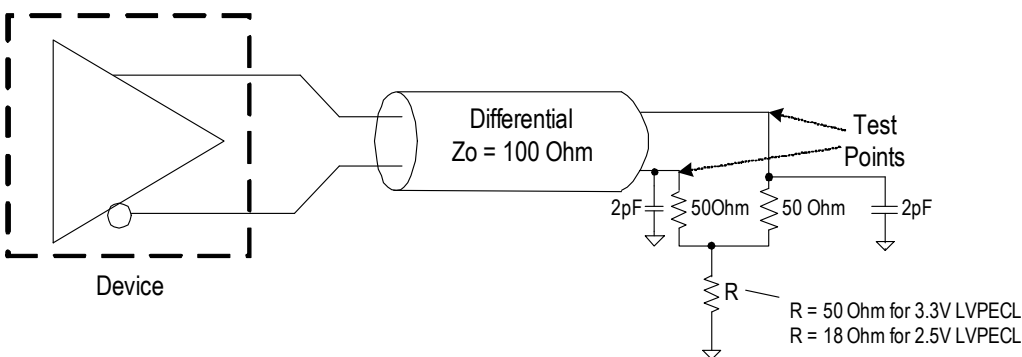
**Figure 3. HCSL Test Load**



**Figure 4. LVDS Test Load**

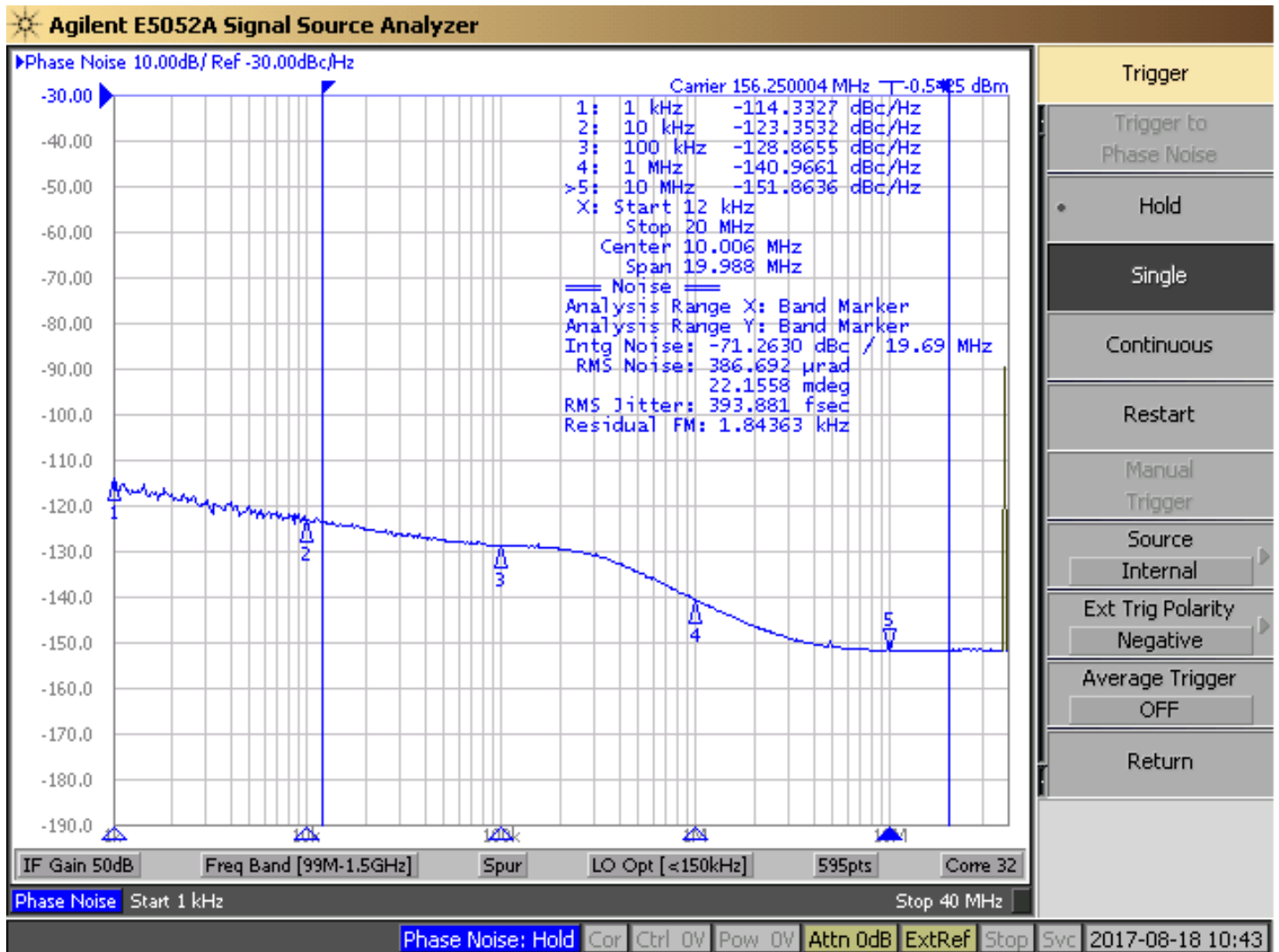


**Figure 5. LVPECL Test Load**



# Jitter Performance Characteristics

**Figure 6. Typical Phase Jitter Plot at 156.25MHz**



**Note:** Measured with OUT2 = 156.25MHz on, 39.625MHz input.

**Table 16. Jitter Performance <sup>1,2</sup>**

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
J <sub>CY-CY</sub>	Cycle to Cycle Jitter	LVC MOS 3.3V ±5%, -40°C–90°C.		5	30	ps
		All differential outputs 3.3V ±5%, -40°C–90°C.		25	35	ps
J <sub>PK-PK</sub>	Period Jitter	LVC MOS 3.3V ±5%, -40°C–90°C.		28	40	ps
		All differential outputs 3.3V ±5%, -40°C–90°C.		4	30	ps
J <sub>RMS</sub>	RMS Phase Jitter (12kHz–20MHz)	LVC MOS 3.3V ±5%, -40°C–90°C.		0.3		ps
		All differential outputs 3.3V ±5%, -40°C–90°C.		0.5		ps

<sup>1</sup> Measured with 25MHz crystal input.

<sup>2</sup> Configured with OUT0 = 25MHz–LVC MOS; OUT1 = 100MHz–HCSL; OUT2 = 125MHz–LVDS; OUT3 = 156.25MHz–LVPECL.

## PCI Express Jitter Performance and Specification

**Table 17. PCI Express Jitter Performance (Spread Spectrum = Off)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
PCIe Phase Jitter (Common Clocked Architectures)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s) SSC = OFF		4		86	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Lo Band (5.0 GT/s) SSC = OFF		0.05		3	ps (RMS)	1,2
		PCIe Gen2 Hi Band (5.0 GT/s) SSC = OFF		0.22		3.1	ps (RMS)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s) SSC = OFF		0.12		1	ps (RMS)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s) SSC = OFF		0.12		0.5	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s) SSC = OFF		0.05		0.15	ps (RMS)	1,2,3,5
PCIe Phase Jitter (SRNS Architectures)	$t_{jphPCIeG1-SRNS}$	PCIe Gen1 (2.5 GT/s) SSC = OFF		0.3		N/A	ps (p-p)	1,2,6
	$t_{jphPCIeG2-SRNS}$	PCIe Gen2 (5.0 GT/s) SSC = OFF		0.26			ps (RMS)	1,2,6
	$t_{jphPCIeG3-SRNS}$	PCIe Gen3 (8.0 GT/s) SSC = OFF		0.07			ps (RMS)	1,2,6
	$t_{jphPCIeG4-SRNS}$	PCIe Gen4 (16.0 GT/s) SSC = OFF		0.07			ps (RMS)	1,2,6
	$t_{jphPCIeG5-SRNS}$	PCIe Gen5 (32.0 GT/s) SSC = OFF		0.07			ps (RMS)	1,2,6

<sup>1</sup> The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table.

<sup>2</sup> Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

<sup>3</sup> SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

<sup>4</sup> Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

<sup>5</sup> Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

<sup>6</sup> While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by Ö2.

**Table 18. PCI Express Jitter Performance (Spread Spectrum = On)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Units	Notes
PCIe Phase Jitter (Common Clocked Architectures)	$t_{jphPCIeG1-CC}$	PCIe Gen 1 (2.5 GT/s) SSC $\leq$ -0.5%		16		86	ps (p-p)	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Lo Band (5.0 GT/s) SSC $\leq$ -0.5%		0.02		3	ps (RMS)	1,2
		PCIe Gen 2 Hi Band (5.0 GT/s) SSC $\leq$ -0.5%		0.92		3.1	ps (RMS)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (8.0 GT/s) SSC $\leq$ -0.5%		0.37		1	ps (RMS)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (16.0 GT/s) SSC $\leq$ -0.5%		0.37		0.5	ps (RMS)	1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen 5 (32.0 GT/s) SSC $\leq$ -0.5%		N/A		0.15	ps (RMS)	1,2,3,5
PCIe Phase Jitter (SRIS Architectures)	$t_{jphPCIeG1-SRIS}$	PCIe Gen 1 (2.5 GT/s) SSC $\leq$ -0.3%		14		N/A	ps (p-p)	1,2,6
	$t_{jphPCIeG2-SRIS}$	PCIe Gen 2 (5.0 GT/s) SSC $\leq$ -0.3%		1.4			ps (RMS)	1,2,6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen 3 (8.0 GT/s) SSC $\leq$ -0.3%		0.42			ps (RMS)	1,2,6
	$t_{jphPCIeG4-SRIS}$	PCIe Gen 4 (16.0 GT/s) SSC $\leq$ -0.3%		0.36			ps (RMS)	1,2,6
	$t_{jphPCIeG5-SRIS}$	PCIe Gen 5 (32.0 GT/s) SSC $\leq$ -0.3%		N/A			ps (RMS)	1,2,6

<sup>1</sup> The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table.

<sup>2</sup> Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

<sup>3</sup> SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

<sup>4</sup> Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.

<sup>5</sup> Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

<sup>6</sup> While the PCI Express Base Specification 5.0, Revision 1.0 provides the filters necessary to calculate SRIS jitter values, it does not provide specification limits, hence the n/a in the Limit column. SRIS values are informative only. In general, a clock operating in an SRIS system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by Ö2.

## Features and Functional Blocks

### Device Startup and Power-On-Reset

The device has an internal power-up reset (POR) circuit. All  $V_{DDs}$  must be connected to desired supply voltage to trigger POR.

User can define specific default configurations through internal One-Time-Programmable (OTP) memory. Either customer or factory can program the default configuration. Please refer to [VersaClock 6E Family Register Descriptions and Programming Guide](#) for details or contact Renesas if a specific factory-programmed default configuration is required.

Device will identify which of the 2 modes to operate in by the state of  $OUT0\_SEL\_I2CB$  pin at POR. Both of the 2 modes default configurations can be programmed as stated above.

- Software Mode (I<sup>2</sup>C):**  $OUT0\_SEL\_I2CB$  is low at POR. I<sup>2</sup>C interface will be open to users for in-system programming, overriding device default configurations at any time.
- Hardware Select Mode:**  $OUT0\_SEL\_I2CB$  is high at POR. Device has been programmed to load OTP at power-up ( $REG0[7]=1$ ). The device will load internal registers according to [Table 19. Power-up Behavior](#).

Internal OTP memory can support up to 4 configurations, selectable by  $SEL0/SEL1$  pins.

At POR, logic levels at  $SEL0$  and  $SEL1$  pins must be settled, resulting the selected configuration to be loaded at power up.

After the first 10ms of operation, the levels of the  $SELx$  pins can be changed, either to low or to the same level as  $V_{DD0}/V_{DDA}$ . The  $SELx$  pins must be driven with a digital signal of < 300ns rise/fall time and only a single pin can be changed at a time. After a pin level change, the device must not be interrupted for at least 1ms so that the new values have time to load and take effect.

**Table 19. Power-up Behavior**

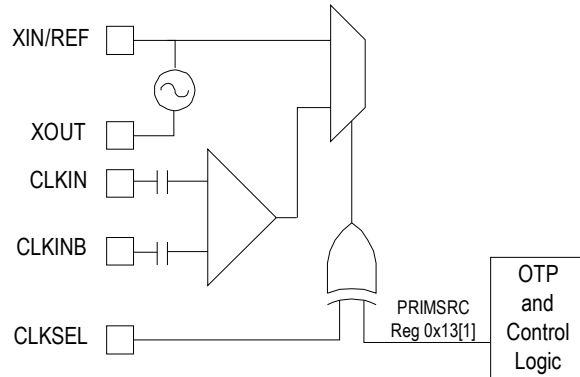
$OUT0\_SEL\_I2CB$ at POR	$SEL1$	$SEL0$	I <sup>2</sup> C Access	$REG0:7$	Config
1	0	0	No	0	0
1	0	1	No	0	1
1	1	0	No	0	2
1	1	1	No	0	3
0	X	X	Yes	1	I <sup>2</sup> C defaults
0	X	X	Yes	0	0

### Reference Clock and Selection

The device supports up to two clock inputs.

- Crystal input, can be driven by a single-ended clock.
- Clock input ( $CLKIN$ ,  $CLKINB$ ), a fully differential input that only accepts a reference clock. A single-ended clock can also drive it on  $CLKIN$ .

**Figure 7. Clock Input Diagram, Internal Logic**



### Manual Switchover

The  $CLKSEL$  pin selects the input clock between either  $XTAL/REF$  or ( $CLKIN$ ,  $CLKINB$ ).

$CLKSEL$  polarity can be changed by I<sup>2</sup>C programming (Byte  $0x13[1]$ ) as shown in the table below.

0 =  $XIN/REF$ ,  $XOUT$  (default); 1 =  $CLKIN$ ,  $CLKINB$ .

**Table 20. Input Clock Select**

PRIMSRC	$CLKSEL$	Source
0	0	$XIN/REF$
0	1	$CLKIN$ , $CLKINB$
1	0	$CLKIN$ , $CLKINB$
1	1	$XIN/REF$

When  $SM[1:0]$  is "0x", the redundant inputs are in manual switchover mode. In this mode,  $CLKSEL$  pin is used to switch between the primary and secondary clock sources. The  $PRIMSRC$  bit determines the primary and secondary clock source setting. During the switchover, no glitches will occur at the output of the device, although there may be frequency and phase drift, depending on the exact phase and frequency relationship between the primary and secondary clocks.

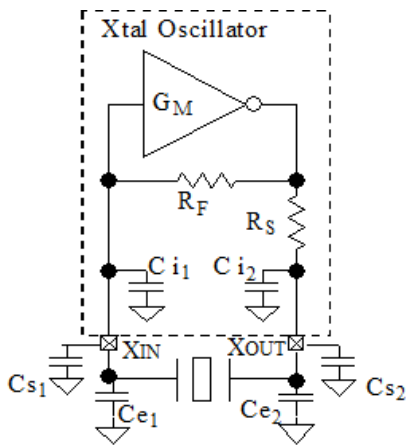


## Internal Crystal Oscillator (XIN/REF)

### Choosing Crystals

A crystal manufacturer will calibrate its crystals to the nominal frequency with a certain load capacitance value. When the oscillator load capacitance matches the crystal load capacitance, the oscillation frequency will be accurate. When the oscillator load capacitance is lower than the crystal load capacitance, the oscillation frequency will be higher than nominal and vice versa so for an accurate oscillation frequency you need to make sure to match the oscillator load capacitance with the crystal load capacitance.

### Tuning the Crystal Load Capacitor



Cs1 and Cs2 are stray capacitances at each crystal pin and typical values are between 1pF and 3pF.

Ce1 and Ce2 are additional external capacitors, increasing the load capacitance reduces the oscillator gain so please consult the factory when adding Ce1 and/or Ce2 to avoid crystal startup issues. Ci1 and Ci2 are integrated programmable load capacitors, one at XIN and one at XOUT. Ci1 and Ci2.

The value of each capacitor is composed of a fixed capacitance amount plus a variable capacitance amount set with the XTAL[5:0] register.

**Table 22. Recommended Crystal Characteristics**

Parameter	Minimum	Typical	Maximum	Units
Mode of Oscillation	Fundamental			
Frequency	8	25	40	MHz
Equivalent Series Resistance (ESR)		10	100	Ω
Shunt Capacitance			7	pF
Load Capacitance (CL) at <= 25MHz	6	8	12	pF
Load Capacitance (CL) > 25MHz to 40MHz	6		8	pF
Maximum Crystal Drive Level			100	μW

Ci1 and Ci2 are commonly programmed to be the same value. Adjustment of the crystal tuning capacitors allows maximum flexibility to accommodate crystals from various manufacturers. The range of tuning capacitor values available are in accordance with the following table.

Ci1/Ci2 starts at 9pF with setting 000000b and can be increased up to 25pF with setting 111111b. The step per bit is 0.5pF.

**Table 21. XTAL[5:0] Tuning Capacitor**

Parameter	Bits	Step (pF)	Minimum (pF)	Maximum (pF)
XTAL	6	0.5	9	25

You can write the following equation for this capacitance:

$$C_i = 9pF + 0.5pF \times XTAL[5:0]$$

$$C_{XIN} = C_{i1} + C_{s1} + C_{e1}$$

$$C_{XOUT} = C_{i2} + C_{s2} + C_{e2}$$

The final load capacitance of the crystal:

$$C_L = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$$

It is recommended to set the same value for capacitors the same at each crystal pin, meaning:

$$C_{XIN} = C_{XOUT}$$

**Example 1:** The crystal load capacitance is specified as 8pF and the stray capacitance at each crystal pin is Cs = 1.5pF. Assuming equal capacitance value at XIN and XOUT, the equation is as follows:

$$8pF = (9pF + 0.5pF \times XTAL[5:0] + 1.5pF) / 2$$

$$\text{So, } XTAL[5:0] = 11 \text{ (decimal).}$$

**Example 2:** The crystal load capacitance is specified as 12pF and the stray capacitance Cs is unknown. Footprints for external capacitors Ce are added and a worst case Cs of 5pF is used. For now we use Cs + Ce = 5pF and the right value for Ce can be determined later to make 5pF together with Cs.

$$12pF = (9pF + 0.5pF \times XTAL[5:0] + 5pF) / 2$$

$$\text{So, } XTAL[5:0] = 20 \text{ (decimal).}$$

## Programmable Loop Filter

The device PLL loop bandwidth range depends on the input reference frequency (Fref).

**Table 23. Loop Filter Settings**

Input Reference Frequency (MHz)	Loop Bandwidth Minimum (kHz)	Loop Bandwidth Maximum (kHz)
1	40	126
350	300	1000

## Fractional Output Dividers (FOD)

The device has 4 fractional output dividers (FOD). Each of the FODs are comprised of a 12-bit integer counter, and a 24-bit fractional counter. The output divider can operate in integer divide only mode for improved performance, or utilize the fractional counters to generate a clock frequency accurate to 50ppb.

FOD has the following features:

### Individual Spread Spectrum Modulation

The output clock frequencies can be modulated to spread energy across a broader range of frequencies, lowering system EMI.

Each divider has individual spread ability. Spread modulation independent of output frequency, a triangle wave modulation between 30 and 63kHz.

Spread spectrum can be applied to any output clock, any clock frequency, and any spread amount from  $\pm 0.25\%$  to  $\pm 2.5\%$  center-spread and  $-0.5\%$  to  $-5\%$  down-spread.

### Bypass Mode

Bypass mode (divide by 1) to allow the output to behave as a buffered copy from the input or another FOD.

### Cascaded Mode

As shown in the block diagram, FODs can be cascaded for lower output frequency.

For example, user currently has OUT1 running at 12.288MHz and needs another 48kHz output. The user can cascade FOD2 by taking input from OUT1, with a divide ratio of 256. In this way, OUT 2 is running at 48kHz while in alignment with 12.288MHz on OUT1.

### Dividers Alignment

Each output divider block has a synchronizing pulse to provide startup alignment between outputs dividers. This allows alignment of outputs for low skew performance.

When device is at hardware select mode outputs will be automatically aligned at POR. The same synchronization reset is also triggered when switching between configurations with the SEL0/1 pins. This ensures that the outputs remain aligned in every configuration.

When using software mode I<sup>2</sup>C to reprogram an output divider during operation, alignment can be lost. Alignment can be restored by manually triggering the reset through I<sup>2</sup>C.

The outputs are aligned on the falling edges of each output by default. Rising edge alignment can also be achieved by utilizing the programmable skew feature to delay the faster clock by 180 degrees. The programmable skew feature also allows for fine tuning of the alignment.

## Programmable Skew

The device has the ability to skew outputs by quadrature values. The skew on each output can be adjusted from 0 to 360 degrees. Skew is adjusted in units equal to 1/32 of the VCO period. So, for 100MHz output and a 2800MHz VCO, you can select how many 11.161ps units you want added to your skew (resulting in units of 0.402 degrees). For example, 0, 0.402, 0.804, 1.206, 1.408, and so on. The granularity of the skew adjustment is always dependent on the VCO period and the output period.

## Output Drivers

The device output drivers support the following features individually:

- 2.5V or 3.3V voltage level for HCSL/LVPECL operation
- 1.8V, 2.5V or 3.3V voltage levels for CMOS/LVDS operation
- CMOS supports 4 operating modes:
  - CMOSD: OUTx and OUTxB 180 degrees out of phase
  - CMOSX2: OUTx and OUTxB phase-aligned
  - CMOS1: only OUTx pin is on
  - CMOS2: only OUTxB pin is on

When a given output is configured to at CMOSD or CMOSX2, then all previously described configuration and control apply equally to both pins.

- Independent output enable/disabled by register bits. When disabled, an output can be either in a logic 1 state or Hi-Z.

The following options are used to disable outputs:

1. Output turned off by I<sup>2</sup>C.
2. Output turned off by SD/OE pin.
3. Output unused, which means is turned off regardless of OE pin status.

## SD/OE Pin Function

SD/OE pin can be programmed as following functions:

1. OE output enable (low active).
2. OE output enable (high active).
3. Global shutdown (low active).
4. Global shutdown (high active).

Output behavior when disabled is also programmable. User will have the option to choose output driver behavior when it's off:

1. OUTx pin high, OUTxB pin low. (Controlled by SD/OE pin).
2. OUTx/OUTxB Hi-Z (Controlled by SD/OE pin).
3. OUTx pin high, OUTxB pin low. (Configured through I<sup>2</sup>C).
4. OUTx/OUTxB Hi-Z (Configured by I<sup>2</sup>C).

The user has the option to disable the output with either I<sup>2</sup>C or SD/OE pin. Refer to [VersaClock 6E Family Register Descriptions and Programming Guide](#) for details.

## I<sup>2</sup>C Operation

The device acts as a slave device on the I<sup>2</sup>C bus using one of the two I<sup>2</sup>C addresses (0xD0 or 0xD4) to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations.

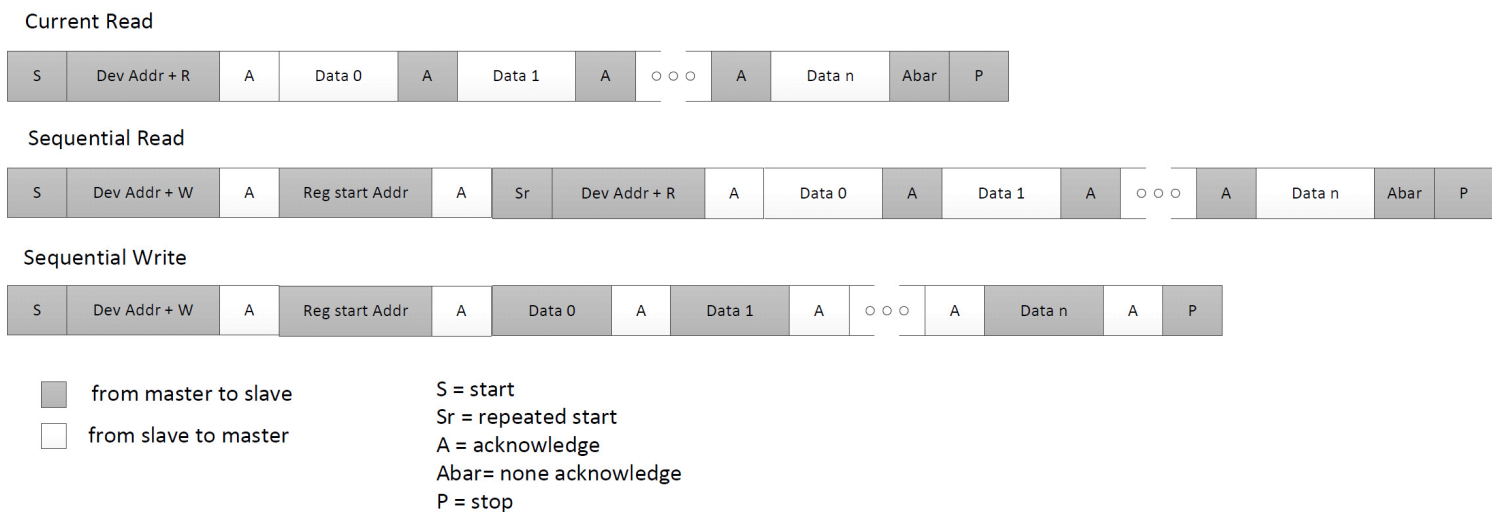
Address bytes(2 bytes) specify the register address of the byte position of the first register to write or read.

Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first).

Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP bit is received, at which point, all data received in the block write will be written simultaneously.

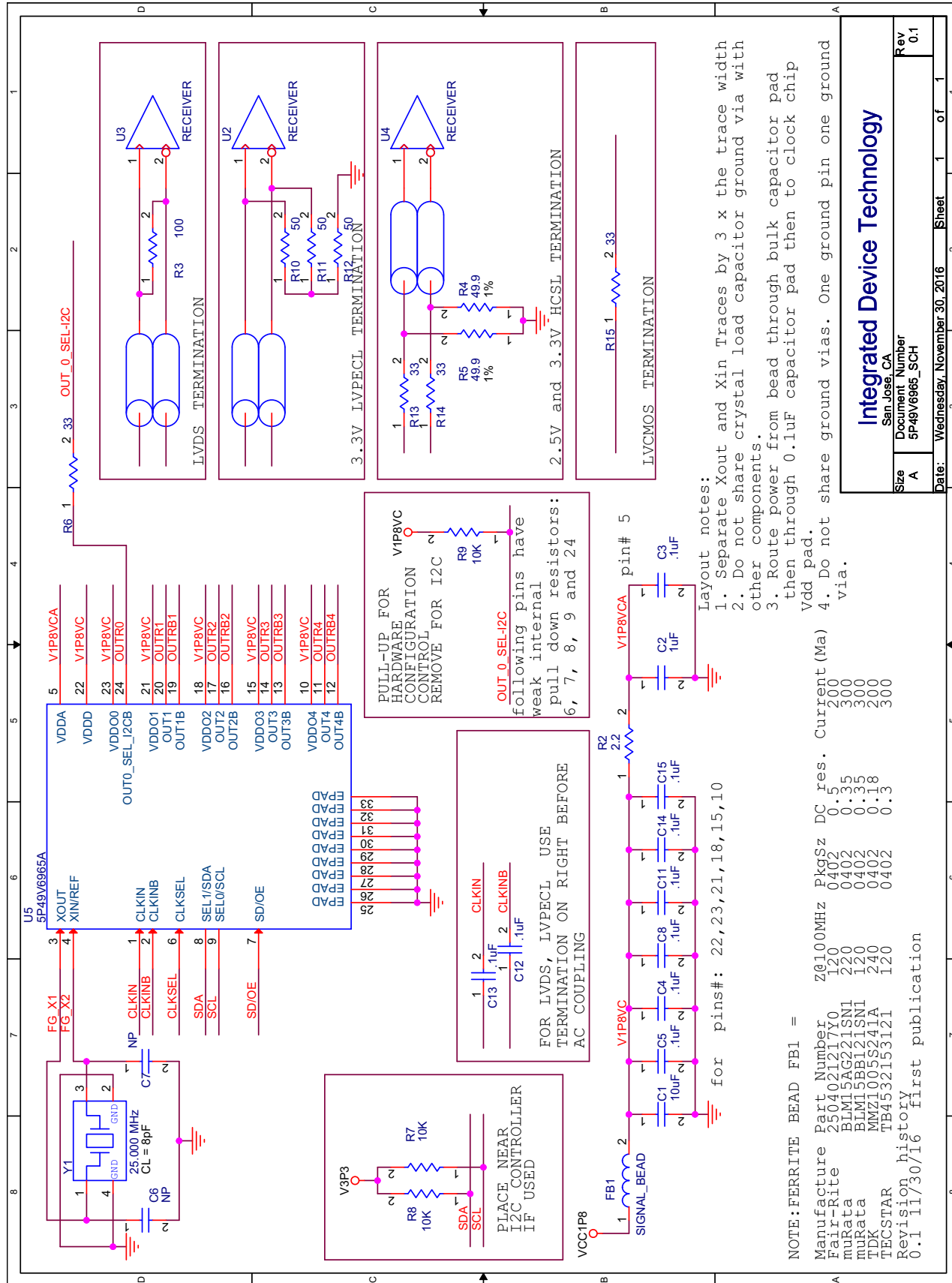
For full electrical I<sup>2</sup>C compliance, use external pull-up resistors for SDATA and SCLK.

**Figure 8. I<sup>2</sup>C R/W Sequence**



# Typical Application Circuits

Figure 9. Application Circuit Example



Size	A	Document Number	5P49V6965_SCH	Rev	0.1
Date:	Wednesday, November 30, 2016	Sheet	1	of	1

**Integrated Device Technology**  
 San Jose, CA

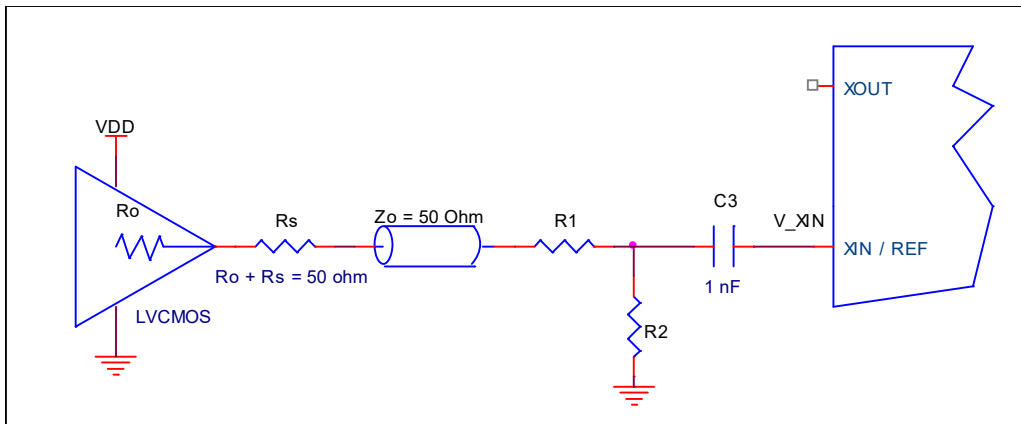
## Input – Driving the XIN/REF or CLKIN

### Driving XIN/REF with a CMOS Driver

In some cases, it is encouraged to have XIN/REF driven by a clock input for reasons like better SNR, multiple input select with device CLKIN, etc. The XIN/REF pin is able to take an input when its amplitude is between 500mV and 1.2V and the slew rate more than 0.2V/ns.

The XIN/REF input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating.

**Figure 10. Overdriving XIN with a CMOS Driver**



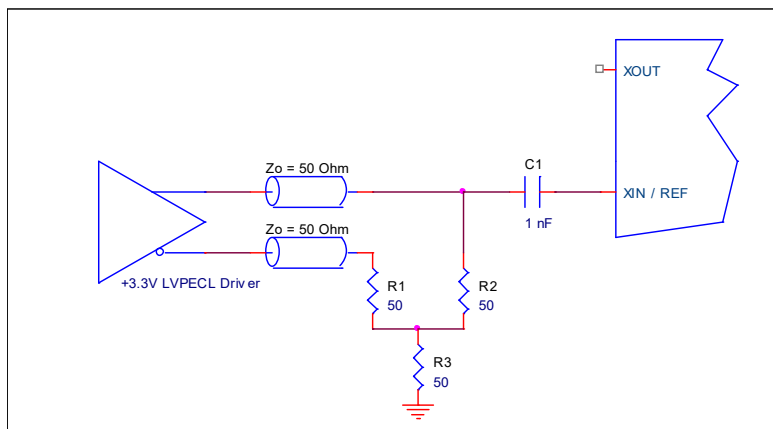
**Table 24. Nominal Voltage Divider Values for Overdriving XIN with Single-ended Driver**

LVCMOS Diver $V_{DD}$	$R_o + R_s$	$R_1$	$R_2$	$V_{XIN}$ (peak)	$R_o+R_s+R_1+R_2$
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

### Driving XIN with an LVPECL Driver

Figure 11 shows an example of the interface diagram for a +3.3V LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN/REF input. It is recommended that all components in the schematics be placed in the layout; though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input. If the driver is 2.5V LVPECL, the only change necessary is to use the appropriate value of R3.

**Figure 11. Overdriving XIN with an LVPECL Driver**



### Wiring the CLKIN Pin to Accept Single-ended Inputs

CLKIN cannot take a signal larger than 1.2V pk-pk due to the 1.2V regulated input inside. However, it is internally AC coupled so it is able to accept both LVDS and LVPECL input signals.

Occasionally, it is desired to have CLKIN to take CMOS levels. Below is an example showing how this can be achieved.

This configuration has three properties:

1. Total output impedance of  $R_o$  and  $R_s$  matches the 50Ω transmission line impedance.
2.  $V_{rx}$  voltage is generated at the CLKIN which maintains the LVCMOS driver voltage level across the transmission line for best S/N.
3.  $R_1$ – $R_2$  voltage divider values ensure that  $V_{rx}$  p-p at CLKIN is less than the maximum value of 1.2V.

**Figure 12. Recommended Schematic for Driving CLKIN with LVCMOS Driver**

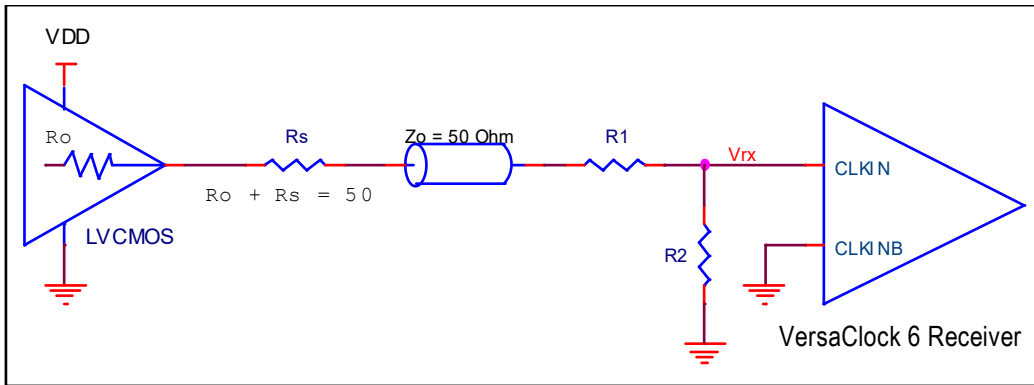


Table 25 shows resistor values that ensure the maximum drive level for the CLKIN port is not exceeded for all combinations of 5% tolerance on the driver  $V_{DD}$ ,  $V_{DD00}$  and 5% resistor tolerances. The values of the resistors can be adjusted to reduce the loading for slower and weaker LVCMOS driver by increasing the impedance of the  $R_1$ – $R_2$  divider. To better assist this assessment, the total load ( $R_o + R_s + R_1 + R_2$ ) on the driver is included in the table.

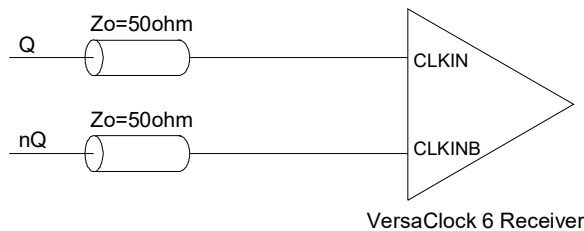
**Table 25. Nominal Voltage Divider Values for Overdriving CLKIN with Single-ended Driver**

LVCMOS Diver $V_{DD}$	$R_o + R_s$	$R_1$	$R_2$	$V_{rx}$ (peak)	$R_o+R_s+R_1+R_2$
3.3	50.0	130	75	0.97	255
2.5	50.0	100	100	1.00	250
1.8	50.0	62	130	0.97	242

### Driving CLKIN with Differential Clock

CLKIN/CLKINB will accept DC coupled HCSL/LVPECL/LVDS signals.

**Figure 13. CLKIN, CLKINB Input Driven by an HCSL Driver**

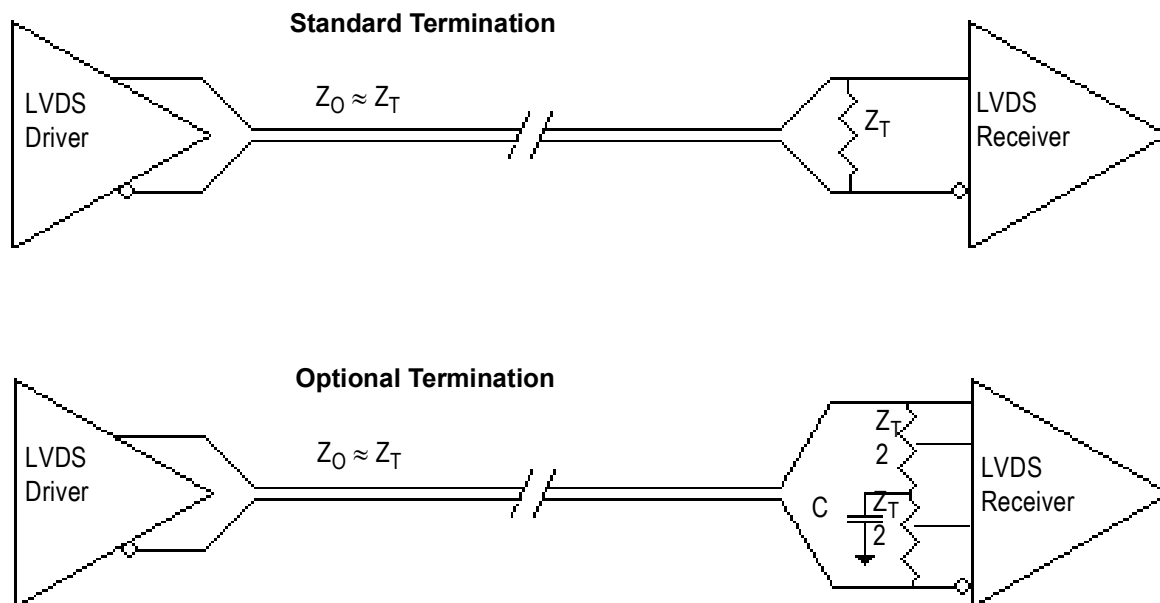


## Output – Single-ended or Differential Clock Terminations

### LVDS Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between  $90\Omega$  and  $132\Omega$ . The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a  $100\Omega$  parallel resistor at the receiver and a  $100\Omega$  differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. The standard termination schematic as shown in figure [Standard Termination](#) or the termination of figure [Optional Termination](#) can be used, which uses a center tap capacitance to help filter common mode noise. The capacitor value should be approximately  $50\text{pF}$ . In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the Renesas LVDS output. If using a non-standard termination, it is recommended to contact Renesas and confirm that the termination will function as intended. For example, the LVDS outputs can be AC coupled by placing capacitors between the LVDS outputs and the  $100\Omega$  shunt load. This is a common practice with receiver with internal self-bias circuitry. If using a non-standard termination, it is recommended to contact Renesas and confirm that the termination will function as intended.

**Figure 14. Standard and Optional Terminations**



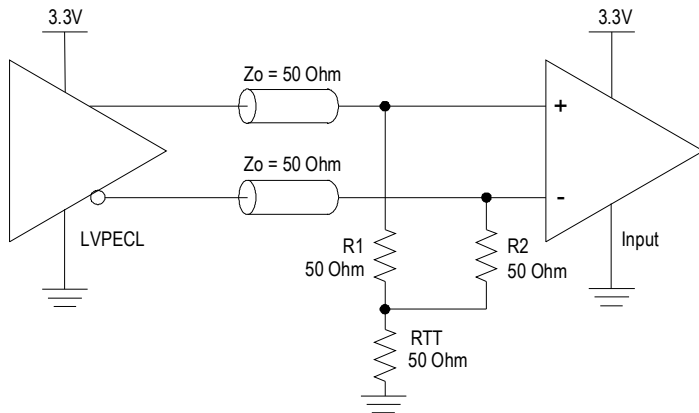
### LVPECL Termination

The clock layout topology shown below is a typical termination for LVPECL outputs.

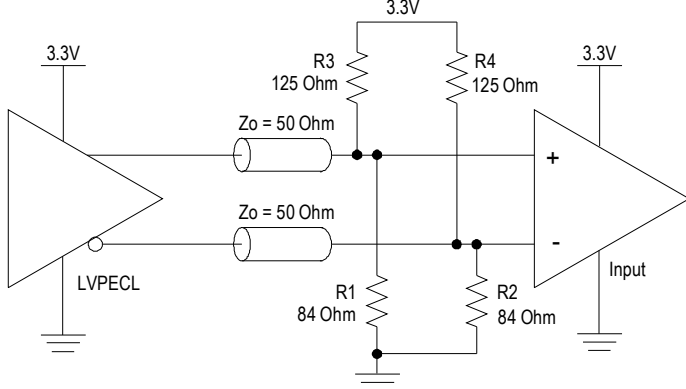
The differential outputs generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion.

For  $V_{DDO} = 2.5V$ , the  $V_{DDO} - 2V$  is very close to ground level. The R3 in 2.5V LVPECL output termination can be eliminated and the termination is shown in Figure 17, 2.5V LVPECL Output Termination.

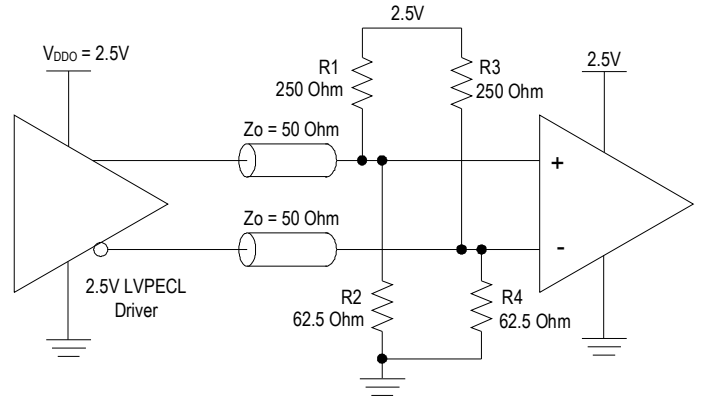
**Figure 15. 3.3V LVPECL Output Termination (1)**



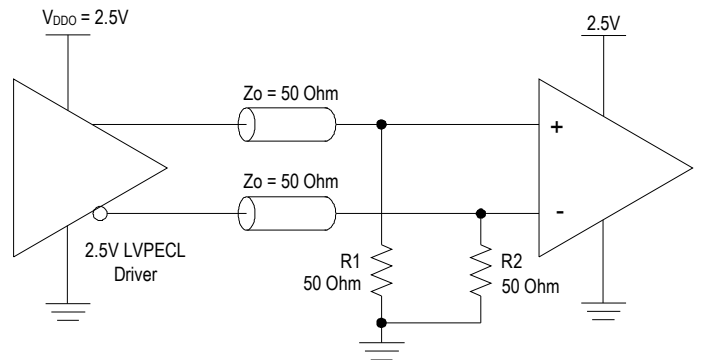
**Figure 16. 3.3V LVPECL Output Termination (2)**



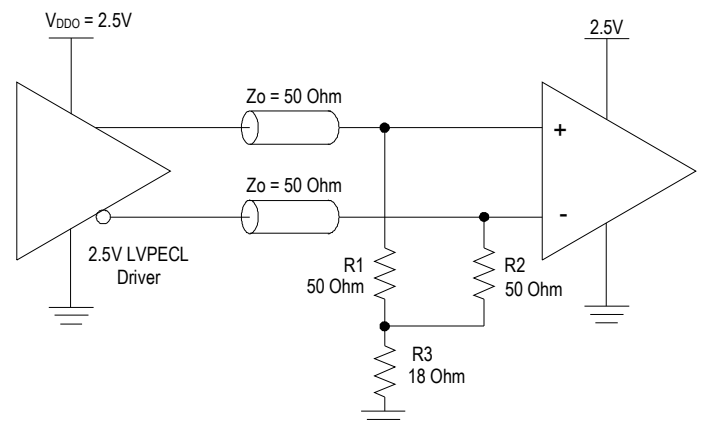
**Figure 17. 2.5V LVPECL Output Termination**



**Figure 18. 2.5V LVPECL Driver Termination (1)**



**Figure 19. 2.5V LVPECL Driver Termination (2)**

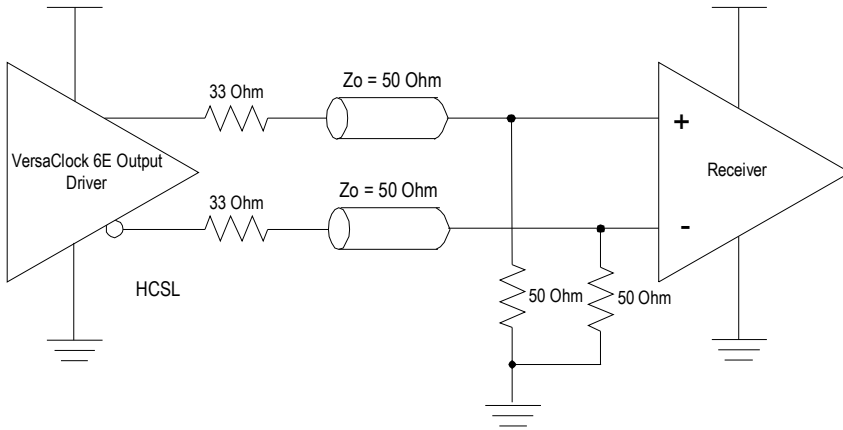




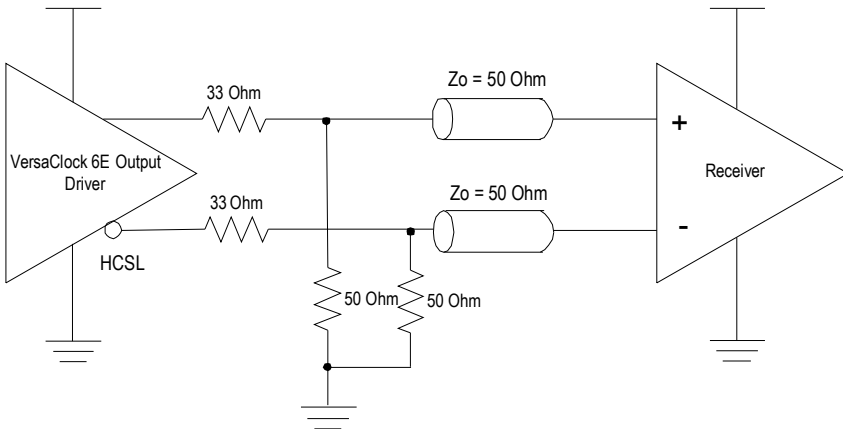
### HCSL Termination

HCSL termination scheme applies to both 3.3V and 2.5V  $V_{DDO}$ .

**Figure 20. HCSL Receiver Terminated**



**Figure 21. HCSL Source Terminated**

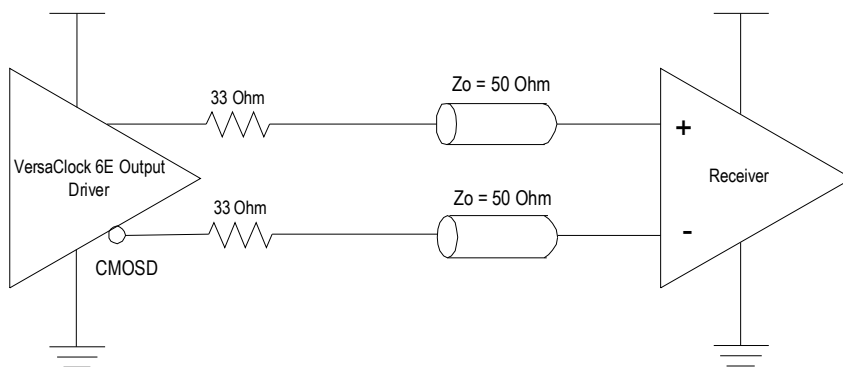


### LVC MOS Termination

Each output pair can be configured as a standalone CMOS or dual-CMOS output driver. CMOS driver termination example is shown below.

- CMOS1 - Single CMOS active on OUTx pin.
- CMOS2 - Single CMOS active on OUTxB pin.
- CMOSD - Dual CMOS outputs active on both OUTx and OUTxB pins, 180 degrees out of phase.
- CMOSX2 - Dual CMOS outputs active on both OUTx and OUTxB pins, in-phase.

**Figure 22. LVC MOS Termination**

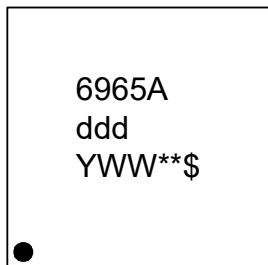


## Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

[www.idt.com/us/en/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-09-mm-body-05mm-pitch-epad-280-x-280-mm-nlg24p2](http://www.idt.com/us/en/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-09-mm-body-05mm-pitch-epad-280-x-280-mm-nlg24p2)

## Marking Diagram



- Line 1: truncated part number.
- Line 2: “ddd” denotes dash code.
- Line 3:
  - “YWW” is the last digit of the year and week that the part was assembled.
  - “\*\*” denotes sequential lot number.
  - “\$” denotes mark code.

## Ordering Information

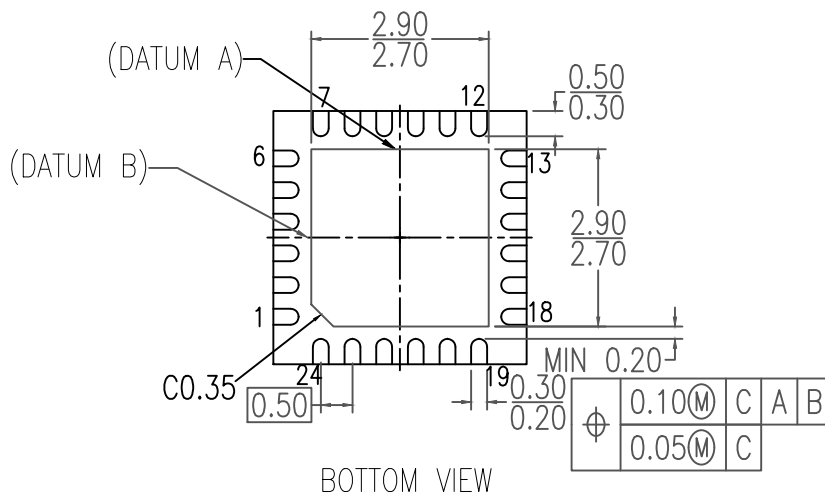
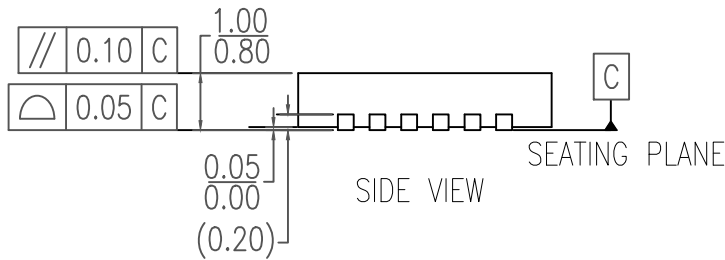
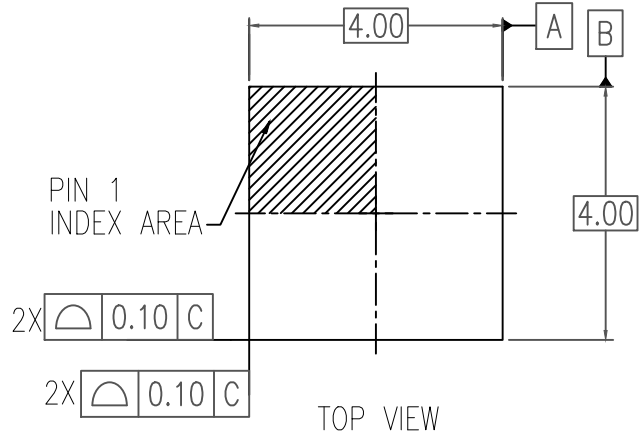
Orderable Part Number	Package	Carrier Type	Temperature
5P49V6965AdddNLGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tray	-40° to +85°C
5P49V6965AdddNLGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40° to +85°C
5P49V6965A000NLGI	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tray	-40° to +85°C
5P49V6965A000NLGI8	4 × 4 mm, 0.5mm pitch 24-VFQFPN	Tape and Reel	-40° to +85°C

<sup>1</sup> “ddd” denotes factory programmed configurations based on required settings. Contact factory for factory programming.

<sup>2</sup> “000” denotes un-programmed parts for user customization.

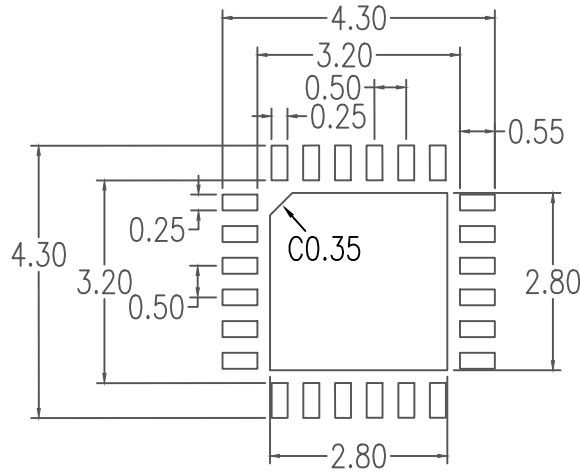
## Revision History

Revision Date	Description of Change
August 20, 2020	Updated the slew rate terminology in section <a href="#">Driving XIN/REF with a CMOS Driver</a> .
September 18, 2019	<ul style="list-style-type: none"> <li>▪ Updated Absolute Maximum Ratings table.</li> <li>▪ Updated PCI Express Jitter Performance tables (<a href="#">Table 17</a> and <a href="#">Table 18</a>).</li> <li>▪ Updated Electrical Characteristics tables (<a href="#">Table 9</a>, <a href="#">Table 11</a>, and <a href="#">Table 14</a>).</li> </ul>
June 19, 2019	<ul style="list-style-type: none"> <li>▪ PCIe specification updated.</li> <li>▪ Added recommended power ramp time.</li> <li>▪ Expanded spread spectrum value range.</li> <li>▪ I2C tolerant voltage footnote changed to 3.3V.</li> <li>▪ LVDS Termination section allows AC-coupling for LVDS signals.</li> </ul>
August 31, 2018	Updated schematics for <a href="#">Driving XIN/REF with a CMOS Driver</a> and <a href="#">Driving XIN with an LVPECL Driver</a> .
March 15, 2018	<ul style="list-style-type: none"> <li>▪ Updated absolute maximum ratings for supply voltage to 3.6V.</li> <li>▪ Updated typical and maximum values in <a href="#">Current Consumption</a> table.</li> <li>▪ Minor updates to <a href="#">AC Timing Characteristics</a>, <a href="#">Electrical Characteristics – CMOS Outputs</a>, and <a href="#">Electrical Characteristics – LVDS Outputs</a> tables.</li> </ul>
November 6, 2017	Initial release.



NOTES:

1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Nov 2, 2018	Rev 02	New Format, Recalculate Land Pattern
Oct 12, 2016	Rev 01	Add Chamfer

