11.2.3 HCSL Termination

HCSL termination scheme applies to both 3.3V and 2.5V VDDO.

Figure 18. HCSL Receiver Terminated

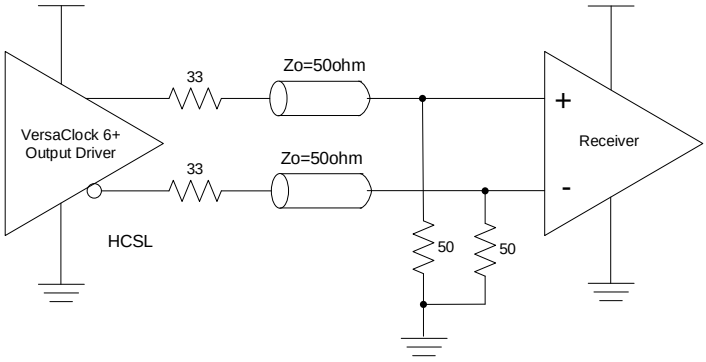
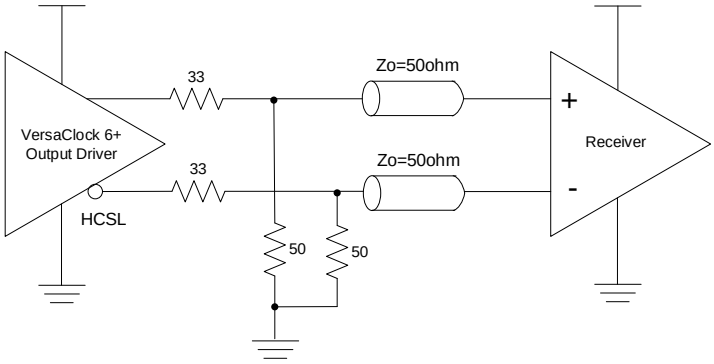


Figure 19. HCSL Source Terminated

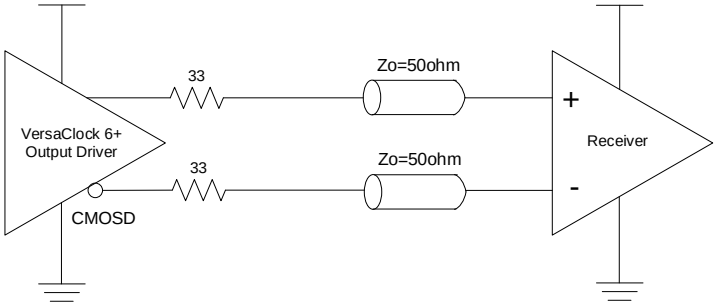


11.2.4 LVCMOS Termination

Each output pair can be configured as a standalone CMOS or dual-CMOS output driver. An example of CMOSD driver termination is shown in the following figure:

- CMOS1 – Single CMOS active on OUTx pin
- CMOS2 – Single CMOS active on OUTxB pin
- CMOSD – Dual CMOS outputs active on both OUTx and OUTxB pins, 180 degrees out of phase
- CMOSX2 – Dual CMOS outputs active on both OUTx and OUTxB pins, in-phase.

Figure 20. LVCMOS Termination

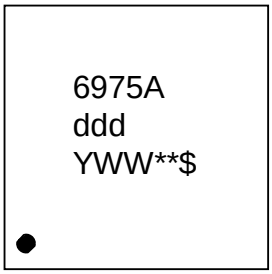


12. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.idt.com/document/psc/24-lga-package-outline-drawing-40-x-40-x-140-mm-body-05mm-pitch-ltg24t2

13. Marking Diagram



1. Line 1 is the truncated part number.
2. “ddd” denotes the dash code.
3. “YWW” is the last digit of the year and week that the part was assembled.
4. “**” denotes the sequential lot number.
5. “$” denotes the mark code.

14. Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
5P49V6975AdddLTGI	4 × 4 mm 24-LGA	Tray	-40° to +85°C
5P49V6975AdddLTGI8	4 × 4 mm 24-LGA	Tape and Reel	-40° to +85°C
5P49V6975A000LTGI	4 × 4 mm 24-LGA	Tray	-40° to +85°C
5P49V6975A000LTGI8	4 × 4 mm 24-LGA	Tape and Reel	-40° to +85°C

1. “ddd” denotes factory programmed configurations based on required settings. Please contact factory for factory programming.
2. “000” denotes un-programmed parts for user customization.

15. Revision History

Revision Date	Description of Change
October 4, 2019	▪ Updated Absolute Maximum Ratings table. ▪ Updated PCI Express Jitter Performance tables (Table 17 and Table 18). ▪ Updated Electrical Characteristics tables (Table 9, Table 11, and Table 14).
June 20, 2019	▪ PCIe specification updated. ▪ Added recommended power ramp time. ▪ Expanded spread spectrum value range. ▪ I2C tolerant voltage footnote changed to 3.3V. ▪ LVDS Termination section allows AC-coupling for LVDS signals.
April 27, 2018	Updated Supply Voltage, Current Consumption and AC Timing Characteristics electrical tables.
March 15, 2018	Updated Current Consumption, AC Timing, LVDS, and CMOS electrical tables.
February 15, 2018	Updated package outline drawings.
January 31, 2018	Updated ordering information package code designator from NLG to LTG.
January 10, 2018	Initial release.