

Features

- ◆ **High-speed access**
 - Commercial: 20ns (max.)
- ◆ **Low-power operation**
 - IDT7054L
 - Active: 750mW (typ.)
 - Standby: 1.5mW (typ.)
- ◆ **True FourPort memory cells which allow simultaneous access of the same memory locations**
- ◆ **Fully asynchronous operation from each of the four ports: P1, P2, P3, and P4**
- ◆ **TTL-compatible; single 5V (±10%) power supply**
- ◆ **Available in 128 pin Thin Quad Flatpack package**
- ◆ **Green parts available, see ordering information**

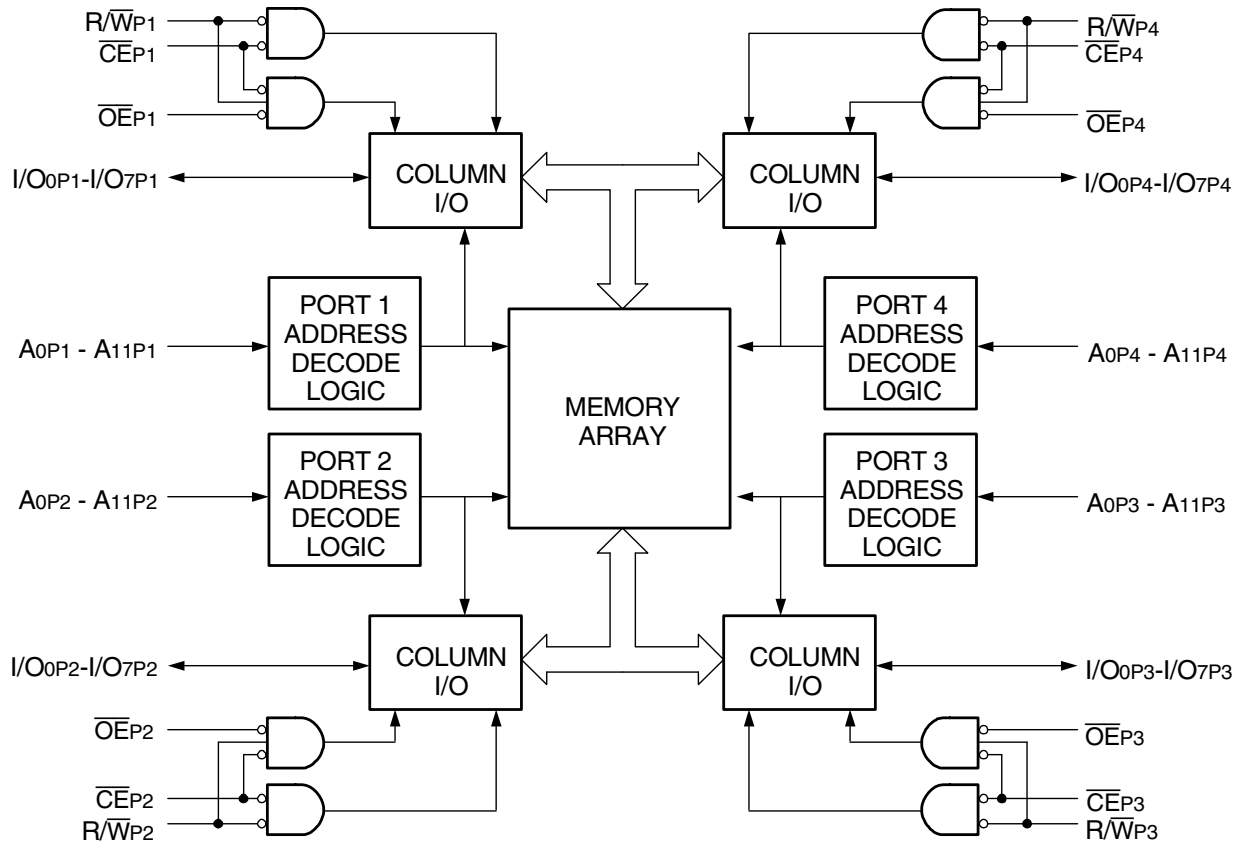
Description

The IDT7054 is a high-speed 4K x 8 FourPort™ Static RAM designed to be used in systems where multiple access into a common RAM is required. This FourPort Static RAM offers increased system performance in multiprocessor systems that have a need to communicate in real time and also offers added benefit for high-speed systems in which multiple access is required in the same cycle.

The IDT7054 is also designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrated or withstand contention when all ports simultaneously access the same FourPort RAM location.

The IDT7054 provides four independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for

Functional Block Diagram



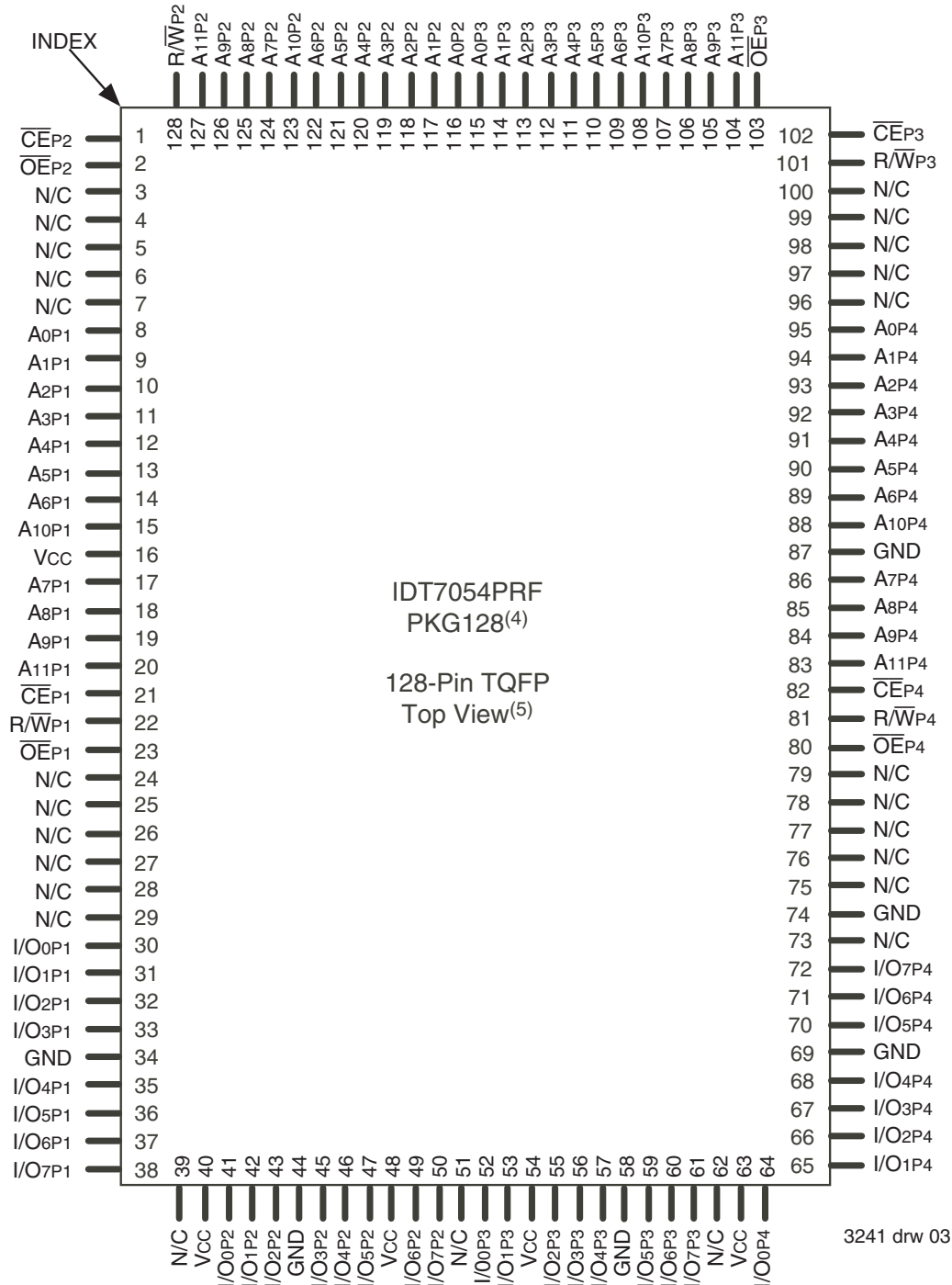
3241 drw 01

reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from all ports. An automatic power down feature, controlled by \overline{CE} , permits the on-chip circuitry of each port to enter a very low power standby power mode.

Fabricated using CMOS high-performance technology, this FourPort SRAM typically operates on only 750mW of power.

The IDT7054 is packaged in a 128-pin Thin Quad Flatpack (TQFP).

Pin Configuration^(1,2,3)



NOTES:

1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately 14mm x 20mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations^(1,2)

| Symbol | Pin Name |
|---------------------|------------------------|
| A0 P1 - A11 P1 | Address Lines - Port 1 |
| A0 P2 - A11 P2 | Address Lines - Port 2 |
| A0 P3 - A11 P3 | Address Lines - Port 3 |
| A0 P4 - A11 P4 | Address Lines - Port 4 |
| I/O0 P1 - I/O7 P1 | Data I/O - Port 1 |
| I/O0 P2 - I/O7 P2 | Data I/O - Port 2 |
| I/O0 P3 - I/O7 P3 | Data I/O - Port 3 |
| I/O0 P4 - I/O7 P4 | Data I/O - Port 4 |
| $\overline{R/W}$ P1 | Read/Write - Port 1 |
| $\overline{R/W}$ P2 | Read/Write - Port 2 |
| $\overline{R/W}$ P3 | Read/Write - Port 3 |
| $\overline{R/W}$ P4 | Read/Write - Port 4 |
| GND | Ground |
| \overline{CE} P1 | Chip Enable - Port 1 |
| \overline{CE} P2 | Chip Enable - Port 2 |
| \overline{CE} P3 | Chip Enable - Port 3 |
| \overline{CE} P4 | Chip Enable - Port 4 |
| \overline{OE} P1 | Output Enable - Port 1 |
| \overline{OE} P2 | Output Enable - Port 2 |
| \overline{OE} P3 | Output Enable - Port 3 |
| \overline{OE} P4 | Output Enable - Port 4 |
| Vcc | Power |

NOTES:

- All Vcc pins must be connected to the power supply.
- All GND pins must be connected to the ground supply.

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Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|--------------------|------|
| Vcc | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | — | 6.0 ⁽²⁾ | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10ns.
- V_{TERM} must not exceed Vcc + 10%.

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Capacitance⁽¹⁾

(TA = +25°C, f = 1.0MHz) TQFP ONLY

| Symbol | Parameter | Conditions ⁽²⁾ | Max. | Unit |
|------------------|--------------------|---------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 9 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 0V | 10 | pF |

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NOTES:

- This parameter is determined by device characterization but is not production tested.
- 3dV references the interpolated capacitance when the input and the output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

| Grade | Ambient Temperature | GND | Vcc |
|------------|---------------------|-----|------------|
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |

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NOTES:

- This is the parameter T_A. This is the "instant on" case temperature.

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial | Unit |
|----------------------------------|--------------------------------------|-------------------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| I _{OUT} | DC Output Current | 50 | mA |

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V_{TERM} ≥ Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,5) (V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Condition | Version | 7054X20 Com'l Only | | 7054X25 Com'l & Ind | | 7054X35 Com'l Only | | Unit | |
|--------|--|--|---------|---------------------|------|---------------------|------|---------------------|------|------|----|
| | | | | TYP. ⁽²⁾ | Max. | TYP. ⁽²⁾ | Max. | TYP. ⁽²⁾ | Max. | | |
| ICC1 | Operating Power Supply Current (All Ports Active) | $\overline{CE} = V_{IL}$ Outputs Disabled $f = 0^{(3)}$ | COML. | S | 150 | 300 | 150 | 300 | 150 | 300 | mA |
| | | | | L | 150 | 250 | 150 | 250 | 150 | 250 | |
| | | | IND. | S | — | — | 150 | 360 | 150 | 360 | mA |
| | | | | L | — | — | 150 | 300 | 150 | 300 | |
| ICC2 | Dynamic Operating Current (All Ports Active) | $\overline{CE} = V_{IL}$ Outputs Disabled $f = f_{MAX}^{(4)}$ | COML. | S | 240 | 370 | 225 | 350 | 210 | 335 | mA |
| | | | | L | 210 | 325 | 195 | 305 | 180 | 290 | |
| | | | IND. | S | — | — | 225 | 400 | 210 | 395 | mA |
| | | | | L | — | — | 195 | 340 | 180 | 330 | |
| ISB | Standby Current (All Ports - TTL Level Inputs) | $\overline{CE} = V_{IH}$ $f = f_{MAX}^{(4)}$ | COML. | S | 70 | 95 | 60 | 85 | 40 | 75 | mA |
| | | | | L | 60 | 80 | 50 | 70 | 35 | 60 | |
| | | | IND. | S | — | — | 60 | 115 | 40 | 110 | mA |
| | | | | L | — | — | 50 | 85 | 35 | 80 | |
| ISB1 | Full Standby Current (All Ports - All CMOS Level Inputs) | All Ports $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(3)}$ | COML. | S | 1.5 | 15 | 1.5 | 15 | 1.5 | 15 | mA |
| | | | | L | 0.3 | 1.5 | 0.3 | 1.5 | 0.3 | 1.5 | |
| | | | IND. | S | — | — | 1.5 | 30 | 1.5 | 30 | mA |
| | | | | L | — | — | 0.3 | 4.5 | 0.3 | 4.5 | |

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NOTES:

- 'X' in part number indicates power rating (S or L).
- V_{CC} = 5V, T_A = +25°C and are not production tested.
- f = 0 means no address or control lines change.
- At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- For the case of one port, divide the appropriate current above by four.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | 7054S | | 7054L | | Unit |
|-----------------|--------------------------------------|---|-------|------|-------|------|------|
| | | | Min. | Max. | Min. | Max. | |
| I _{LI} | Input Leakage Current ⁽¹⁾ | V _{CC} = 5.5V, V _{IN} = 0V to V _{CC} | — | 10 | — | 5 | μA |
| I _{LO} | Output Leakage Current | $\overline{CE} = V_{IH}$, V _{OUT} = 0V to V _{CC} | — | 10 | — | 5 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = 4mA | — | 0.4 | — | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -4mA | 2.4 | — | 2.4 | — | V |

NOTE:

- At V_{CC} ≤ 2.0V input leakages are undefined.

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AC Test Conditions

| | |
|-------------------------------|-----------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 3ns Max. |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1 and 2 |

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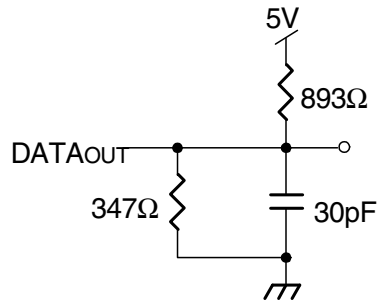
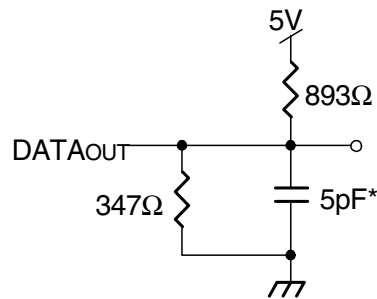


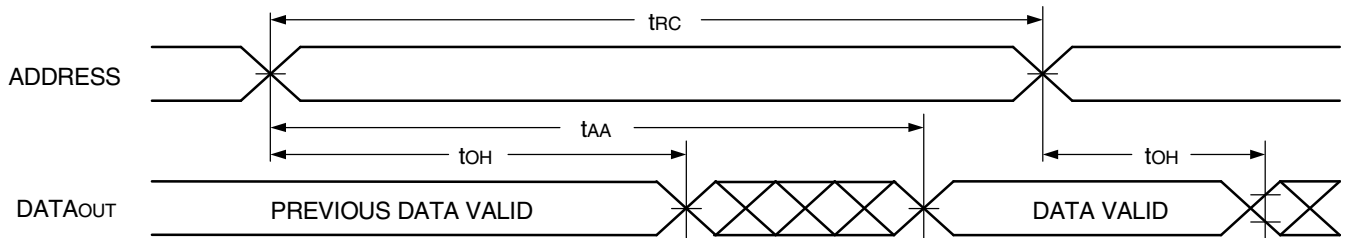
Figure 1. AC Output Test Load



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Figure 2. Output Test Load
(for t_{LZ} , t_{HZ} , t_{WZ} , t_{OW})
*Including scope and jig

Timing Waveform of Read Cycle No. 1, Any Port⁽¹⁾



3241 drw 05

NOTE:

1. $\overline{R}/\overline{W} = V_{IH}$, $\overline{OE} = V_{IL}$, and $\overline{CE} = V_{IL}$.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽³⁾

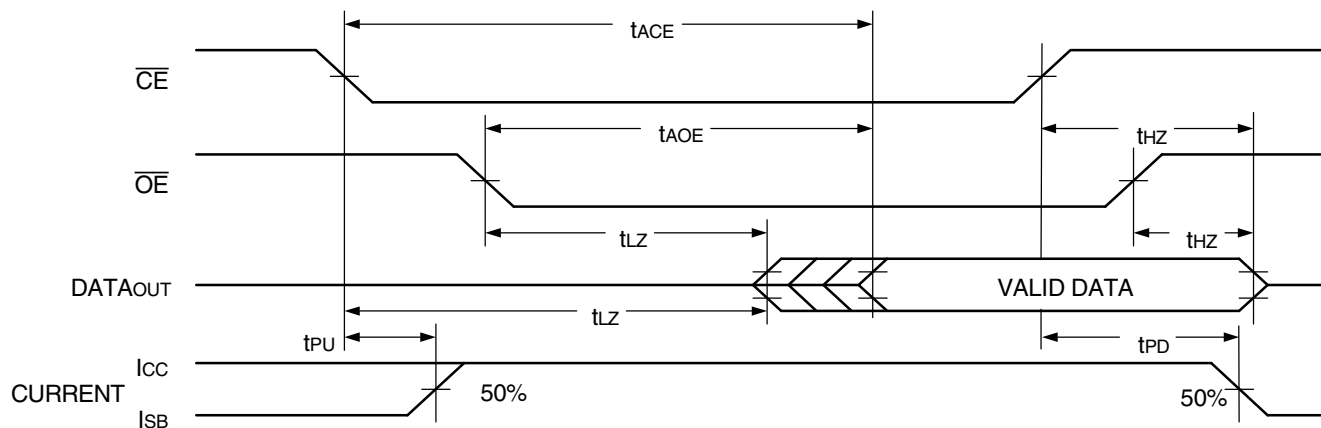
| Symbol | Parameter | 7054X20 Com'l Only | | 7054X25 Com'l & Ind | | 7054X35 Com'l Only | | Unit |
|-------------------|--|-----------------------|------|------------------------|------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | |
| t _{RC} | Read Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| t _{AA} | Address Access Time | — | 20 | — | 25 | — | 35 | ns |
| t _{ACE} | Chip Enable Access Time | — | 20 | — | 25 | — | 35 | ns |
| t _{AOE} | Output Enable Access Time | — | 10 | — | 15 | — | 25 | ns |
| t _{OH} | Output Hold from Address Change | 0 | — | 0 | — | 0 | — | ns |
| t _{LZ} | Output Low-Z Time ^(1,2) | 5 | — | 5 | — | 5 | — | ns |
| t _{HZ} | Output High-Z Time ^(1,2) | — | 12 | — | 15 | — | 15 | ns |
| t _{PU} | Chip Enable to Power Up Time ⁽²⁾ | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Chip Disable to Power Down Time ⁽²⁾ | — | 20 | — | 25 | — | 35 | ns |

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NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. 'X' in part number indicates power rating (S or L).

Timing Waveform of Read Cycle No. 2, Any Port^(1, 2)



3241 drw 06

NOTES:

1. R/W = V_{IH} for Read Cycles.
2. Addresses valid prior to or coincident with CE-bar transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁵⁾

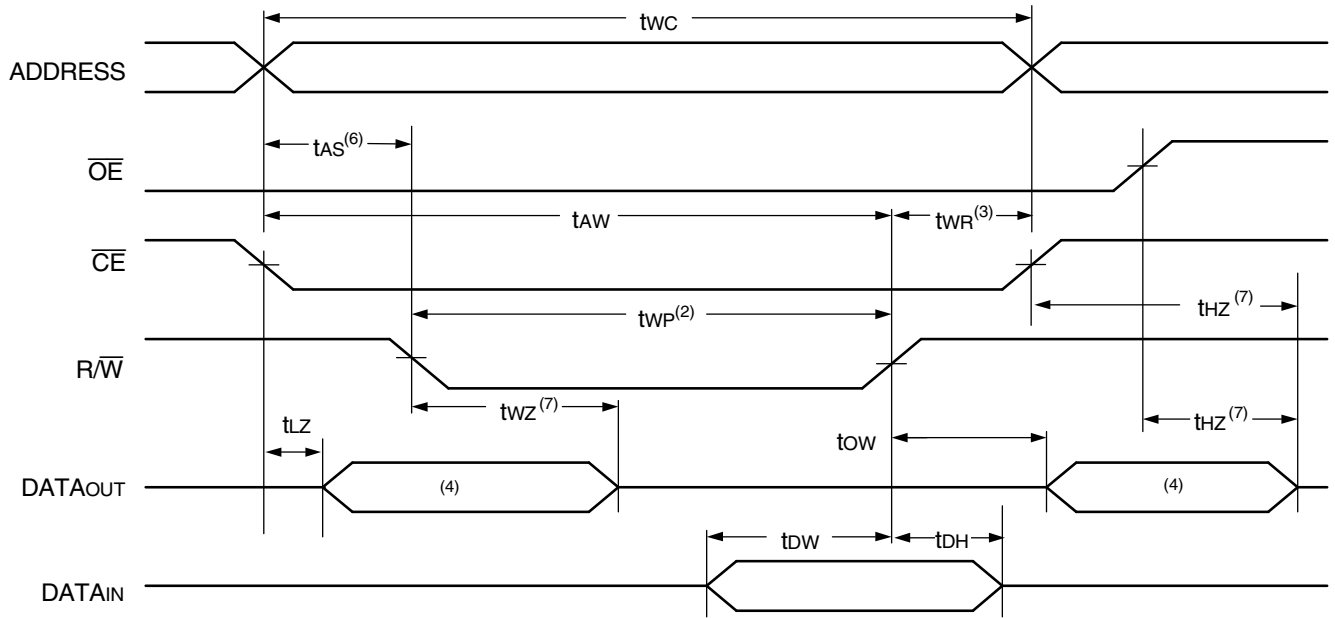
| Symbol | Parameter | 7054X20 Com'l Only | | 7054X25 Com'l & Ind | | 7054X35 Com'l Only | | Unit |
|--------------------|--|--------------------|------|---------------------|------|--------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE | | | | | | | | |
| t _{WC} | Write Cycle Time | 20 | — | 25 | — | 35 | — | ns |
| t _{EW} | Chip Enable to End-of-Write | 15 | — | 20 | — | 30 | — | ns |
| t _{AW} | Address Valid to End-of-Write | 15 | — | 20 | — | 30 | — | ns |
| t _{AS} | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| t _{WP} | Write Pulse Width ⁽³⁾ | 15 | — | 20 | — | 30 | — | ns |
| t _{WR} | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| t _{DW} | Data Valid to End-of-Write | 15 | — | 15 | — | 20 | — | ns |
| t _{HZ} | Output High-Z Time ^(1,2) | — | 15 | — | 15 | — | 15 | ns |
| t _{DH} | Data Hold Time | 0 | — | 0 | — | 0 | — | ns |
| t _{WZ} | Write Enable to Output in High-Z ^(1,2) | — | 12 | — | 15 | — | 15 | ns |
| t _{OW} | Output Active from End-of-Write ^(1,2) | 0 | — | 0 | — | 0 | — | ns |
| t _{WDD} | Write Pulse to Data Delay ⁽⁴⁾ | — | 35 | — | 45 | — | 55 | ns |
| t _{DDD} | Write Data Valid to Read Data Delay ⁽⁴⁾ | — | 30 | — | 35 | — | 45 | ns |

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NOTES:

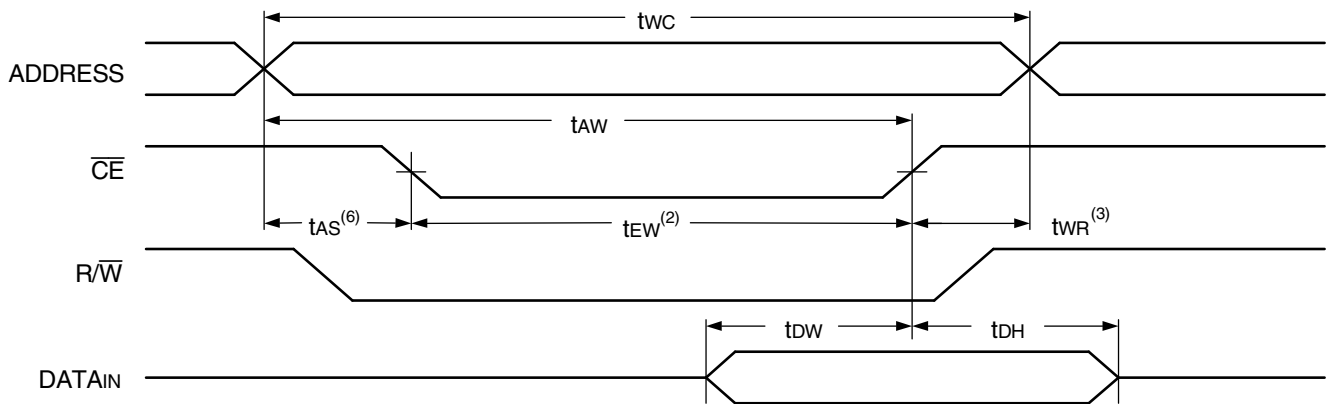
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but is not production tested.
3. If $\overline{OE} = V_{IL}$ during a $R\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{OW})$ to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW} . If $\overline{OE} = V_{IH}$ during an $R\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} . Specified for $\overline{OE} = V_{IH}$ (refer to "Timing Waveform of Write Cycle", Note 8).
4. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read".
5. 'X' in part number indicates power rating.

Timing Waveform of Write Cycle No. 1, $\overline{R/\overline{W}}$ Controlled Timing^(5,8)



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Timing Waveform of Write Cycle No. 2, \overline{CE} Controlled Timing^(1,5)

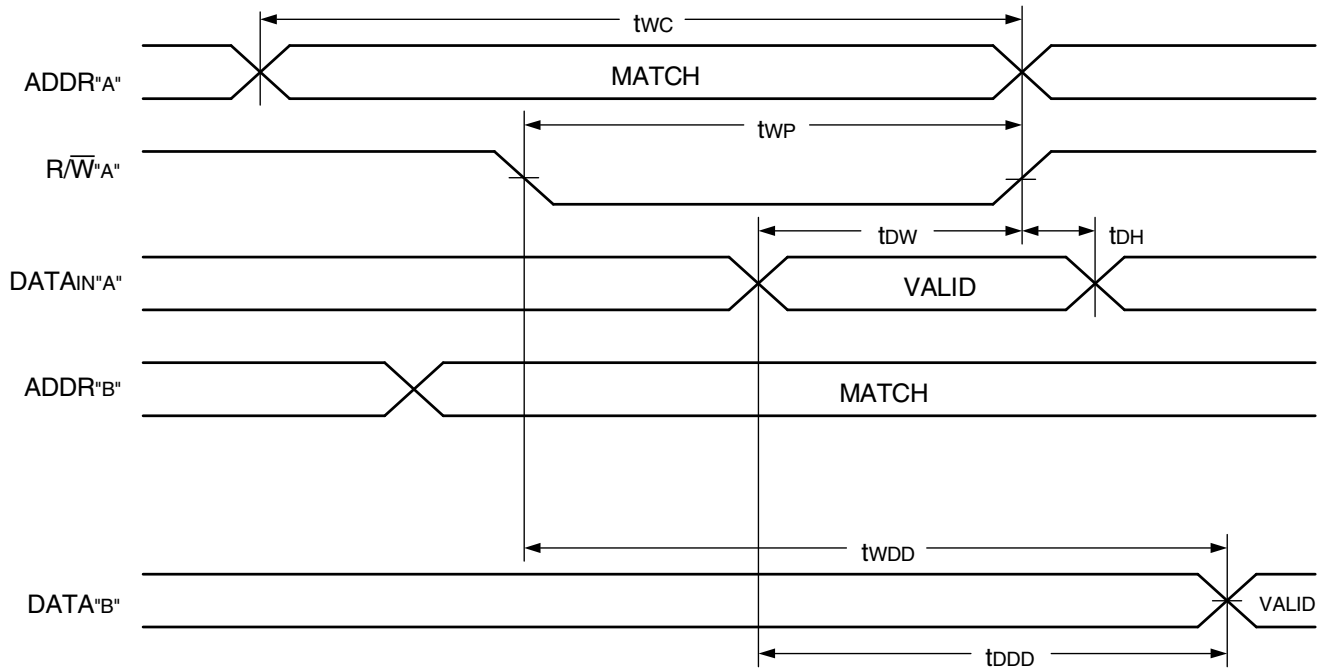


3241 drw 08

NOTES:

1. $\overline{R/\overline{W}}$ or $\overline{CE} = V_{IH}$ during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE} = V_{IL}$ and a $\overline{R/\overline{W}} = V_{IL}$.
3. t_{WR} is measured from the earlier of \overline{CE} or $\overline{R/\overline{W}} = V_{IH}$ to the end of write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} LOW transition occurs simultaneously with or after the $\overline{R/\overline{W}} = V_{IL}$ transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, \overline{CE} or $\overline{R/\overline{W}}$.
7. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed but is not production tested.
8. If $\overline{OE} = V_{IL}$ during a $\overline{R/\overline{W}}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WZ} + t_{DW})$ to allow the I/O drivers to turn off data to be placed on the bus for the required t_{OW} . If $\overline{OE} = V_{IH}$ during an $\overline{R/\overline{W}}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

Timing Waveform of Write with Port-to-Port Read^(1, 2)



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NOTES:

1. $\overline{OE} = V_{IL}$ for the reading ports.
2. All timing is the same for left and right ports. Port "A" may be either of the four ports and Port "B" is any other port.

Functional Description

The IDT7054 provides four ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls on-chip power down circuitry that permits the respective port to go into standby mode when not selected ($\overline{CE} = V_{IH}$). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control (\overline{OE}). In the read mode, the port's \overline{OE} turns on the output drivers when set LOW. READ/ WRITE conditions are illustrated in the table.

Table I – Read/Write Control

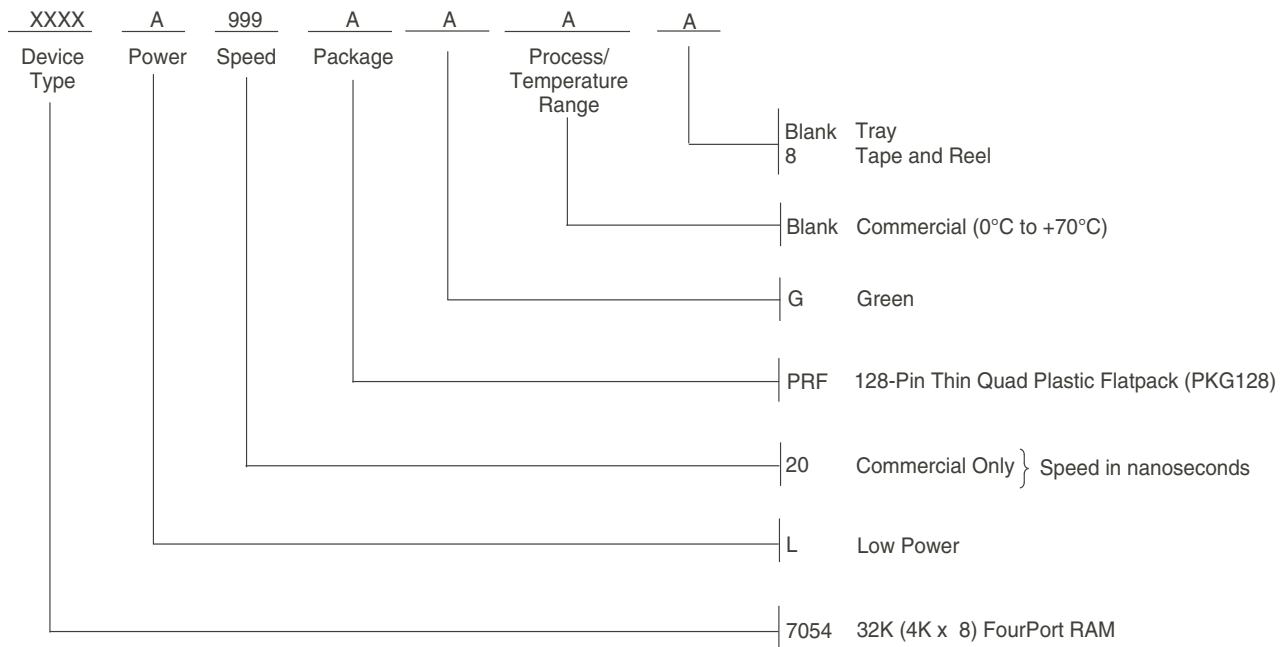
| Any Port ⁽¹⁾ | | | | Function |
|-------------------------|-----------------|-----------------|---------|---|
| R/W | \overline{CE} | \overline{OE} | D0-7 | |
| X | H | X | Z | Port Deselected: Power-Down |
| X | H | X | Z | $\overline{CEP1}=\overline{CEP2}=\overline{CEP3}=\overline{CEP4}=V_{IH}$ Power Down Mode ISB or ISB1 |
| L | L | X | DATAIN | Data on port written into memory ⁽²⁾ |
| H | L | L | DATAOUT | Data in memory output on port |
| X | X | H | Z | Outputs Disabled |

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NOTES:

1. "H" = V_{IH} , "L" = V_{IL} , "X" = Don't Care, "Z" = High Impedance
2. For valid write operation, no more than one port can write to the same address location at the same time.

Ordering Information



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NOTES:

LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02
 Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

Ordering Information

| Speed (ns) | Orderable Part ID | Pkg. Code | Pkg. Type | Temp. Grade |
|------------|-------------------|-----------|-----------|-------------|
| 20 | 7054L20PRFG | PKG128 | TQFP | C |
| | 7054L20PRFG8 | PKG128 | TQFP | C |

Datasheet Document History

- 01/18/99: Initiated datasheet document history
Converted to new format
Cosmetic typographical corrections
Added additional notes to pin configurations
- 06/04/99: Changed drawing format
Page 1 Corrected DSC number
- 09/01/99: Removed Preliminary
- 11/10/99: Replaced IDT logo
- 05/23/00: Page 4 Increased storage temperature parameter
Clarified TA parameter
Page 5 DC Electrical parameters—changed wording from "open" to "disabled"
Changed $\pm 200\text{mV}$ to 0mV in notes
- 10/22/01: Page 2 & 3 Added date revision for pin configurations
Page 5, 7 & 8 Added Industrial temp to column heading for 25ns speed to DC & AC Electrical Characteristics
Page 11 Added Industrial temp offering to 25ns ordering information
Page 4, 5, 7 & 8 Removed Industrial temp footnote from all tables
Page 6 Changed 5ns to 3ns in AC Test Conditions table
Page 1 & 11 Replaced TM logo with ® logo
- 02/20/15: Page 1 Added green availability to features
Page 2 Removed IDT in reference to fabrication
Page 2 2V battery backup for Low-power versions are no longer offered
Page 2,3 & 10 The package code PK128-1 changed to PK128 to match standard package codes
Page 10 Added Tape and Reel and Green to Ordering Information
Pages 1-10 Removed all military data including the G108 pin configuration, changed table headings and ordering information to indicate that there is no longer a military offering for this 7054 device
- 07/02/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018
- 07/11/19: Pages 1 & 10 Deleted obsolete Commercial 25/35ns and Industrial 25ns speed grades
Pages 1 & 10 Removed standard product offering and Industrial speed grade offering
Pages 2 & 10 Updated package code PK128 to PKG128
Page 10 Added Orderable Part Information

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