Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed clock to data access
  - Commercial: 7.5/9/12ns (max.)
  - Industrial: 9ns (max.)
- Low-power operation
  - IDT709379/69L
    - Active: 1.2W (typ.)
    - Standby: 2.5mW (typ.)
- Flow-Through or Pipelined output mode on either Port via the FT/PIPE pins
- Counter enable and reset features
- Dual chip enables allow for depth expansion without additional logic
- Full synchronous operation on both ports
  - 4ns setup to clock and 0ns hold on all control, data, and address inputs
  - Data input, address, and control registers
  - Fast 7.5ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 10ns cycle time, 100MHz operation in Pipelined output mode
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- TTL-compatible, single 5V (±10%) power supply
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Available in a 100-pin Thin Quad Flatpack (TQFP) package
- Green parts available, see ordering information

Functional Block Diagram

Note: A 14L is NC for IDT709369.
Description

The IDT709379/69 is a high-speed 32/16K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT709379/69 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by CE0 and CE1, permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using CMOS high-performance technology, these devices typically operate on only 1.2W of power.

Pin Configurations\(^{(1,2,3)}\)

![Diagram showing pin configurations](image)

709379/69PF PN100\(^{(5)}\)
100-Pin TQFP Top View\(^{(6)}\)

NOTES:
1. A14x is a NC for IDT709369.
2. All Vcc pins must be connected to power supply.
3. All GND pins must be connected to ground.
4. Package body is approximately 14mm x 14mm x 1.4mm
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.
## Pin Names

<table>
<thead>
<tr>
<th>Left Port</th>
<th>Right Port</th>
<th>Names</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEIL, CEIR</td>
<td>CEIL, CEIR</td>
<td>Chip Enables(1)</td>
</tr>
<tr>
<td>R/WIL</td>
<td>R/WIR</td>
<td>Read/Write Enable</td>
</tr>
<tr>
<td>OEL</td>
<td>OER</td>
<td>Output Enable</td>
</tr>
<tr>
<td>A0L - A14(1)</td>
<td>A0R - A14R(1)</td>
<td>Address</td>
</tr>
<tr>
<td>VOIL - VO17L</td>
<td>VOIR - VO17R</td>
<td>Data Input/Output</td>
</tr>
<tr>
<td>CLKIL</td>
<td>CLKIR</td>
<td>Clock</td>
</tr>
<tr>
<td>UBIL</td>
<td>UBIR</td>
<td>Upper Byte Select(2)</td>
</tr>
<tr>
<td>LBIL</td>
<td>LBIR</td>
<td>Lower Byte Select(2)</td>
</tr>
<tr>
<td>ADSIL</td>
<td>ADSIR</td>
<td>Address Strobe</td>
</tr>
<tr>
<td>CNTENIL</td>
<td>CNTENIR</td>
<td>Counter Enable</td>
</tr>
<tr>
<td>CNTRSTIL</td>
<td>CNTRSTIR</td>
<td>Counter Reset</td>
</tr>
<tr>
<td>FT/PIPEL</td>
<td>FT/PIPEIR</td>
<td>Flow-Through/Pipeline</td>
</tr>
<tr>
<td></td>
<td>VCC</td>
<td>Power</td>
</tr>
<tr>
<td></td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>

### NOTES:
1. A14x is an NC for IDT709369.
2. LB and UB are single buffered regardless of state of FT/PIPE.
3. CE0 and CE1 are single buffered when FT/PIPE = VI0, CE0 and CE1 are double buffered when FT/PIPE = VIOH, i.e. the signals take two cycles to deselect.

## Truth Table I—Read/Write and Enable Control(1,2,3)

<table>
<thead>
<tr>
<th>OE</th>
<th>CLK</th>
<th>CE0</th>
<th>CE1</th>
<th>UB</th>
<th>LB</th>
<th>R/W</th>
<th>Upper Byte</th>
<th>Lower Byte</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>↑</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Deselected—Power Down</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Deselected—Power Down</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Both Bytes Deselected</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>DATAIN</td>
<td>High-Z</td>
<td>Write to Upper Byte Only</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>High-Z</td>
<td>DATAIN</td>
<td>Write to Lower Byte Only</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>DATAIN</td>
<td>DATAIN</td>
<td>Write to Both Bytes</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>DATAOUT</td>
<td>High-Z</td>
<td>Read Upper Byte Only</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>DATAOUT</td>
<td>DATAOUT</td>
<td>Read Lower Byte Only</td>
</tr>
<tr>
<td>L</td>
<td>↑</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>DATAOUT</td>
<td>DATAOUT</td>
<td>Read Both Bytes</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>High-Z</td>
<td>High-Z</td>
<td>Outputs Disabled</td>
</tr>
</tbody>
</table>

### NOTES:
1. "H" = VIH, "L" = VIL, "X" = Don't Care.
2. ADS, CNTEN, CNTRST = X.
3. OE is an asynchronous input signal.
### Truth Table II—Address Counter Control\(^{1,2,6}\)

<table>
<thead>
<tr>
<th>External Address</th>
<th>Previous Internal Address</th>
<th>Internal Address Used</th>
<th>CLK</th>
<th>ADS</th>
<th>CN TEN</th>
<th>CN TRST</th>
<th>I/O(^{(1)})</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>An</td>
<td>X</td>
<td>An</td>
<td>↑</td>
<td>L(^{(4)})</td>
<td>X</td>
<td>H</td>
<td>Dvo (n)</td>
<td>External Address Used</td>
</tr>
<tr>
<td>X</td>
<td>An</td>
<td>An + 1</td>
<td>↑</td>
<td>H</td>
<td>L(^{(5)})</td>
<td>H</td>
<td>Dvo(n+1)</td>
<td>Counter Enabled—Internal Address generation</td>
</tr>
<tr>
<td>X</td>
<td>An + 1</td>
<td>An + 1</td>
<td>↑</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>Dvo(n+1)</td>
<td>External Address Blocked—Counter disabled (An + 1 reused)</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>A0</td>
<td>↑</td>
<td>X</td>
<td>X</td>
<td>L(^{(4)})</td>
<td>Dvo(0)</td>
<td>Counter Reset to Address 0</td>
</tr>
</tbody>
</table>

**NOTES:**
1. "H" = \(V_{IH}\), "L" = \(V_{IL}\), "X" = Don’t Care.
2. \(CE_0, UB, LB,\) and \(OE = VIH\); \(CE_1, UB\) and \(LB\).
3. Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
4. \(ADS\) is independent of all other signals including \(CE_0, CE_1, UB\) and \(LB\).
5. The address counter advances if \(CNTEN = VIH\), on the rising edge of \(CLK\), regardless of all other signals including \(CE_0, CE_1, UB\) and \(LB\).
6. While an external address is being loaded \((ADS = VIH)\), \(WI/W = VHL\) is recommended to ensure data is not written arbitrarily.

### Recommended Operating Temperature and Supply Voltage

<table>
<thead>
<tr>
<th>Grade</th>
<th>Ambient Temperature(^{(2)})</th>
<th>GND</th>
<th>Vcc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>(-40°C) to (+70°C)</td>
<td>0V</td>
<td>5.0V ± 10%</td>
</tr>
<tr>
<td>Industrial</td>
<td>(-40°C) to (+85°C)</td>
<td>0V</td>
<td>5.0V ± 10%</td>
</tr>
</tbody>
</table>

**NOTES:**
1. This is the parameter \(T_A\). This is the "instant on" case temperature.

### Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Commercial &amp; Industrial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{TERM})(^{(3)})</td>
<td>Terminal Voltage with Respect to GND</td>
<td>-0.5 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>(T_{BIAS})</td>
<td>Temperature Under Bias</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>(T_{STG})</td>
<td>Storage Temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>(T_{JN})</td>
<td>Junction Temperature</td>
<td>+150</td>
<td>°C</td>
</tr>
<tr>
<td>(I_{OUT})</td>
<td>DC Output Current</td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. \(V_{TERM}\) must not exceed \(V_CC + 10\%\) for more than 25% of the cycle time or 10ns maximum, and is limited to \(< 20\text{mA}\) for the period of \(V_{TERM} \geq V_CC + 10\%\).

### Capacitance\(^{(1)}\)

\((TA = +25°C, f = 1.0MHz)\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions(^{(5)})</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(CN)</td>
<td>Input Capacitance</td>
<td>(VIN = 3\text{V})</td>
<td>9</td>
<td>pF</td>
</tr>
<tr>
<td>(C_{OUT})</td>
<td>Output Capacitance</td>
<td>(VOUT = 3\text{V})</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
1. These parameters are determined by device characterization, but are not production tested.
2. \(3\text{V}\) references the interpolated capacitance when the input and output switch from \(0\text{V}\) to \(3\text{V}\) or from \(3\text{V}\) to \(0\text{V}\).
3. \(C_{OUT}\) also references \(C_{IO}\).
## DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range (Vcc = 5.0V ± 10%)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>709379/69L</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICcL</td>
<td>Input Leakage Current</td>
<td>VCC = 5.5V, VIN = 0V to VCC</td>
<td>—</td>
</tr>
<tr>
<td>ICcO</td>
<td>Output Leakage Current</td>
<td>CE0 = VIH or CE1 = VIL, VOUT = 0V to VCC</td>
<td>—</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>IOL = +4mA</td>
<td>—</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>IOH = -4mA</td>
<td>2.4</td>
</tr>
</tbody>
</table>

**NOTES:**
1. At Vcc < 2.0V input leakages are undefined.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5V ± 10%)  

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter Description</th>
<th>Test Conditions</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Dynamic Operating Current (Both Ports Active)</td>
<td>CE and CE0 = VIH, CE1 = VIL, Outputs Disabled, f = fMAX(1)</td>
<td>COML L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
</tr>
<tr>
<td>ISB1</td>
<td>Standby Current (Both Ports - TTL Level Inputs)</td>
<td>CE0 = CE1 = VIL, f = fMAX(1)</td>
<td>COML L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
</tr>
<tr>
<td>ISB2</td>
<td>Standby Current (One Port - TTL Level Inputs)</td>
<td>CE0' = VIH and CE1' = VIL(3), Active Port Outputs Disabled, f = fMAX(3)</td>
<td>COML L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
</tr>
<tr>
<td>ISB3</td>
<td>Full Standby Current (Both Ports - CMOS Level Inputs)</td>
<td>CE0 &lt; 0.2V and CE0' &gt; VCC - 0.2V(3), VIN &gt; VCC - 0.2V or VIN &lt; 0.2V, Active Port Outputs Disabled, f = fMAX(3)</td>
<td>COML L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
</tr>
<tr>
<td>ISB4</td>
<td>Full Standby Current (One Port - CMOS Level Inputs)</td>
<td>CE0' &lt; 0.2V and CE0' &gt; VCC - 0.2V(3), VIN &gt; VCC - 0.2V or VIN &lt; 0.2V, Active Port Outputs Disabled, f = fMAX(3)</td>
<td>COML L</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
</tr>
</tbody>
</table>

**NOTES:**
1. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/tcyc, using “AC TEST CONDITIONS” at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port “A” may be either left or right port. Port “B” is the opposite from port “A”.
4. Vcc = 5V, TA = 25°C for Typ, and are not production tested. ICC(=l) = 150mA (Typ).
5. CE0x = VIH means CE0x = VIH or CE0x = VIL
CE0x = VIL means CE0x = VIH or CE0x = VIL
CE0x < 0.2V means CE0x < 0.2V and CE0x > VCC - 0.2V
CE0x > VCC - 0.2V means CE0x > VCC - 0.2V or CE0x < 0.2V
6. “X” represents “L” for left port or “R” for right port.
AC Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Times</td>
<td>3ns Max.</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>Figures 1, 2, and 3</td>
</tr>
</tbody>
</table>

Figure 1. AC Output Test load.

Figure 2. Output Test Load (For tCKLZ, tCKHZ, tOLZ, and tOHZ).

*Including scope and jig.

Figure 3. Typical Output Derating (Lumped Capacitive Load).

10pF is the I/O capacitance of this device, and 30pF is the AC Test Load Capacitance.
## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) (3) (VCC = 5V ± 10%)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>709379/69L7 Com'1 Only</th>
<th>709379/69L9 Com'1 &amp; Ind</th>
<th>709379/69L12 Com'1 Only</th>
</tr>
</thead>
<tbody>
<tr>
<td>tCYC1</td>
<td>Clock Cycle Time (Flow-Through) (2)</td>
<td>22 — 25</td>
<td>30 —</td>
<td>ns</td>
</tr>
<tr>
<td>tCYC2</td>
<td>Clock Cycle Time (Pipelined) (2)</td>
<td>12 — 15</td>
<td>20 —</td>
<td>ns</td>
</tr>
<tr>
<td>tCH1</td>
<td>Clock High Time (Flow-Through) (2)</td>
<td>7.5 — 12</td>
<td>12 —</td>
<td>ns</td>
</tr>
<tr>
<td>tCL1</td>
<td>Clock Low Time (Flow-Through) (2)</td>
<td>7.5 — 12</td>
<td>12 —</td>
<td>ns</td>
</tr>
<tr>
<td>tCH2</td>
<td>Clock High Time (Pipelined) (2)</td>
<td>5 — 6</td>
<td>8 —</td>
<td>ns</td>
</tr>
<tr>
<td>tCL2</td>
<td>Clock Low Time (Pipelined) (2)</td>
<td>5 — 6</td>
<td>8 —</td>
<td>ns</td>
</tr>
<tr>
<td>tR</td>
<td>Clock Rise Time</td>
<td>— 3</td>
<td>3 — 3</td>
<td>ns</td>
</tr>
<tr>
<td>tF</td>
<td>Clock Fall Time</td>
<td>— 3</td>
<td>3 — 3</td>
<td>ns</td>
</tr>
<tr>
<td>tSA</td>
<td>Address Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHA</td>
<td>Address Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tSC</td>
<td>Chip Enable Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHC</td>
<td>Chip Enable Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tSE</td>
<td>Byte Enable Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHS</td>
<td>Byte Enable Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tSW</td>
<td>R/W Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHW</td>
<td>R/W Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tSD</td>
<td>Input Data Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHD</td>
<td>Input Data Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tSAD</td>
<td>ADS Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHAD</td>
<td>ADS Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tSCN</td>
<td>CNTEN Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHCN</td>
<td>CNTEN Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tRST</td>
<td>CNTRST Setup Time</td>
<td>4 — 4</td>
<td>4 —</td>
<td>ns</td>
</tr>
<tr>
<td>tHRS</td>
<td>CNTRST Hold Time</td>
<td>0 — 1</td>
<td>1 —</td>
<td>ns</td>
</tr>
<tr>
<td>tOE</td>
<td>Output Enable to Data Valid</td>
<td>— 7.5</td>
<td>9 —</td>
<td>12 ns</td>
</tr>
<tr>
<td>tOL2</td>
<td>Output Enable to Output Low-Z (1)</td>
<td>2 — 2</td>
<td>2 —</td>
<td>ns</td>
</tr>
<tr>
<td>tOH2</td>
<td>Output Enable to Output High-Z (1)</td>
<td>1 — 1</td>
<td>1 —</td>
<td>7 ns</td>
</tr>
<tr>
<td>tCD1</td>
<td>Clock to Data Valid (Flow-Through) (2)</td>
<td>— 18</td>
<td>20 —</td>
<td>25 ns</td>
</tr>
<tr>
<td>tCD2</td>
<td>Clock to Data Valid (Pipelined) (2)</td>
<td>— 7.5</td>
<td>9 —</td>
<td>12 ns</td>
</tr>
<tr>
<td>tDC</td>
<td>Data Output Hold After Clock High</td>
<td>2 — 2</td>
<td>2 —</td>
<td>ns</td>
</tr>
<tr>
<td>tOH2</td>
<td>Clock High to Output High-Z (2)</td>
<td>2 — 2</td>
<td>2 —</td>
<td>9 ns</td>
</tr>
<tr>
<td>tOL2</td>
<td>Clock High to Output Low-Z (2)</td>
<td>2 — 2</td>
<td>2 —</td>
<td>9 ns</td>
</tr>
</tbody>
</table>

### Port-to-Port Delay
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>709379/69L7 Com'1 Only</th>
<th>709379/69L9 Com'1 &amp; Ind</th>
<th>709379/69L12 Com'1 Only</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPWDD</td>
<td>Write Port Clock High to Read Data Delay</td>
<td>— 28</td>
<td>— 35</td>
<td>— 40 ns</td>
</tr>
<tr>
<td>tCCS</td>
<td>Clock-to-Clock Setup Time</td>
<td>— 10</td>
<td>— 15</td>
<td>— 15 ns</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (tCC2, tCD2) to either the Left or Right ports when FT/PIPE = VIL. Flow-Through parameters (tCC1, tCD1) apply when FT/PIPE = VIL for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (OE), FT/PIPE, and FT/PIPEL.
Timing Waveform of Read Cycle for Flow-Through Output ($FT/PIPE\text{"x"} = V_{IL}$)$^{(3,7)}$

Timing Waveform of Read Cycle for Pipelined Operation ($FT/PIPE\text{"x"} = V_{IH}$)$^{(3,7)}$

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $OE$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3. $ADS = V_L$ and $CNTRST = V_H$.
4. The output is disabled (High-Impedance state) by $CE_0 = V_H$, $CE_1 = V_L$, $UB = V_H$, or $LB = V_L$ following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since $ADS = V_L$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If $UB$ or $LB$ was HIGH, then the Upper Byte and/or Lower Byte of DATAOUT for $Q_{n+2}$ would be disabled (High-Impedance state).
7. "X" here denotes Left or Right port. The diagram is with respect to that port.
Timing Waveform of a Bank Select Pipelined Read\(^{(1,2)}\)

Timing Waveform of Write with Port-to-Port Flow-Through Read\(^{(4,5,7)}\)

NOTES:
1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT709379/69 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. UB, LB, O\(E\), and ADS = V\(IL\); CE\(O\), CE\(B\), R/W, and CNTRST = V\(IH\).
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. CE\(O\), UB, LB, and ADS = V\(IL\); CE\(B\), and CNTRST = V\(IH\).
5. O\(E\) = V\(IL\) for the Right Port, which is being read from. O\(E\) = V\(IH\) for the Left Port, which is being written to.
6. If tccs \(\leq\) maximum specified, then data from right port READ is not valid until the maximum specified for tccw.
   If tccs > maximum specified, then data from right port READ is not valid until tccs + tcc0. tccw0 does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".
Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)(3)

![Timing Waveform Diagram](image)

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)(3)

![Timing Waveform Diagram](image)

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $CE_0$, $UB$, $LB$, and $ADS = V_{IL}$, $CE_1$ and $CNTRST = V_{IH}$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $ADS = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

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Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)\(^{(3)}\)

Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE}$ Controlled)\(^{(3)}\)

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_s$; $\overline{CE}_1$ and $\overline{CNTREST} = V_h$. "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_s$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.
Timing Waveform of Pipelined Read with Address Counter Advance\(^{(1)}\)

```
CLK
ADDRESS
ADS
CNTEN
DATAOUT
```

NOTES:
1. \( \text{CE}, \text{OE}, \text{UB}, \text{LB} = \text{VIL}; \text{CE1}, \text{R/W}, \text{CNTRST} = \text{VIH} \).
2. If there is no address change via \( \text{ADS} = \text{VIL} \) (loading a new address) or \( \text{CNTEN} = \text{VIL} \) (advancing the address), i.e. \( \text{ADS} = \text{VIH} \) and \( \text{CNTEN} = \text{VIH} \), then the data output remains constant for subsequent clocks.

Timing Waveform of Flow-Through Read with Address Counter Advance\(^{(1)}\)

```
CLK
ADDRESS
ADS
CNTEN
DATAOUT
```

NOTES:
1. \( \text{CE}, \text{OE}, \text{UB}, \text{LB} = \text{VIL}; \text{CE1}, \text{R/W}, \text{CNTRST} = \text{VIH} \).
2. If there is no address change via \( \text{ADS} = \text{VIL} \) (loading a new address) or \( \text{CNTEN} = \text{VIL} \) (advancing the address), i.e. \( \text{ADS} = \text{VIH} \) and \( \text{CNTEN} = \text{VIH} \), then the data output remains constant for subsequent clocks.
Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)

NOTES:
1. CE0, UB, LB, and R/W = VL; CE1 and CNTRST = VIL.
2. CE0, UB, LB = VL; CE1 = VIL.
3. The “Internal Address” is equal to the “External Address” when ADS = VL and equals the counter output when ADS = VIL.
4. Addresses do not have to be accessed sequentially since ADS = VL constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle.
7. CNTEN = VL advances Internal Address from ‘An’ to ‘An +1’. The transition shown indicates the time required for the counter to advance. The ‘An +1’ Address is written to during this cycle.

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A Functional Description

The IDT709379/69 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

\( CE_0 = V_{IH} \) or \( CE_1 = V_{IL} \) for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT709379/69’s for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with \( CE_0 = V_{IL} \) and \( CE_1 = V_{IH} \) to reactivate the outputs.

Depth and Width Expansion

The IDT709379/69 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT709379/69 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36-bit or wider applications.

NOTE:
1. \( A_{14} \) is for IDT709369.
## Ordering Information

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Power</th>
<th>Speed</th>
<th>Package</th>
<th>Process/ Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>XXXXX</td>
<td>A</td>
<td>99</td>
<td>A</td>
<td>A</td>
</tr>
</tbody>
</table>

1. Tube or Tray
2. Tape & Reel
3. Commercial (0 C to +70 C)
4. Industrial (-40 C to +85 C)
5. Green
6. 100-pin TQFP (PN100)

### Speed

- Commercial Only
- Commercial & Industrial

### Process/ Temperature Range

- Commercial Only
- Commercial & Industrial

### Package

- 709379 576K (32K x 18-Bit) Synchronous Dual-Port RAM
- 709369 288K (16K x 18-Bit) Synchronous Dual-Port RAM

### Notes:

1. Industrial temperature range is available. For other speeds, packages and powers contact your sales office.
2. Green parts available. For specific speeds, packages and powers contact your sales office.
3. LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02
4. Note that information regarding recently obsoleted parts is included in this datasheet for customer convenience.
Datasheet Document History

9/30/99: Initial Public Release
11/10/99: Replaced IDT logo
12/22/99: Page 1 Added nmissing diamond
1/12/01: Page 4 Changed information in Truth Table II
          Increased storage temperature parameter
          Clarified TA parameter
          Page 5 DC Electrical parameters–changed wording from "open" to "disabled"
          Changed ±200mV to 0mV in notes
          Removed Preliminary status
04/26/04: Consolidated multiple devices into one datasheet
          Removed I-temp footnote
          Page 2 Added date revision to pin configuration
          Page 4 Added Junction Temperature to Absolute Maximum Ratings Table
          Added Ambient Temperature footnote
          Page 5 Added I-temp numbers for 9ns speed to the DC Electrical Characteristics Table
          Added 6ns speed DC timing numbers to the DC Electrical Characteristics Table
          Page 7 Added I-temp for 9ns speed to AC Electrical Characteristics Table
          Added 6ns speed AC timing numbers to the AC Electrical Characteristics Table
          Page 15 Added 6ns speed grade and 9ns I-temp to ordering information
          Added IDT Clock Solution Table
          Page 1 & 16 Replaced old TM logo with new TM logo
01/29/09: Page 15 Removed "IDT" from orderable part number
07/26/10: Page 1 Added green parts availability to features
          Page 15 Added green indicator to ordering information
          Page 7 In order to correct the header notes of the AC Elect Chars Table and align them with the Industrial temp range
          values located in the table, the commercial TA header note has been removed
          Pages 8-11 In order to correct the footnotes of timing diagrams, CNTEN has been removed to reconcile the footnotes with
          the CNTEN logic definition found in Truth Table II - Address Counter Control
07/16/15: Page 1 Updated speed offerings by removing the 6.5ns commercial grade in Features
          Page 2 Removed IDT in reference to fabrication
          Page 2 & 15 The package code PN100-1 changed to PN100 to match standard package codes
          Page 5 Removed X6 speed grade from the DC Elec Chars table
          Page 6 Corrected typo in the Typical Output Derating drawing
          Page 7 Removed X6 speed grade from the AC Elec Chars table
          Page 16 Added Tape and Reel indicator to, removed X6 speed grade and updated the commercial offerings in
          Ordering Information
          Page 15 Removed the IDT Clock Solution table
02/08/18: Product Discontinuation Notice - PDN# SP-17-02
          Last time buy expires June 15, 2018
04/24/19: 709369 is obsolete
          709379 is still active
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