Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- High-speed access
  - Commercial: 15/20ns (max.)
  - Industrial: 20ns (max.)
- Low-power operation
  - IDT70V28L
    - Active: 440mW (typ.)
    - Standby: 660µW (typ.)
- Dual chip enables allow for depth expansion without external logic
- IDT70V28 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device

- M/Ś = Vih for BUSy output flag on Master,
  M/Ś = Vil for BUSy input on Slave
- Busy and Interrupt Flags
- On-chip port arbitration logic
- Full on-chip hardware support of semaphore signaling between ports
- Fully asynchronous operation from either port
- Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- LVTTL-compatible, single 3.3V (±0.3V) power supply
- Available in a 100-pin TQFP
- Industrial temperature range (–40°C to +85°C) is available for selected speeds
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**Functional Block Diagram**

**NOTES:**

1. BUSY is an input as a Slave (M/Ś=Vil) and an output when it is a Master (M/Ś=Vih).
2. BUSY and INT are non-tri-state totem-pole outputs (push-pull).
Description

The IDT70V28 is a high-speed 64K x 16 Dual-Port Static RAM. The IDT70V28 is designed to be used as a stand-alone 1024K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit-or-more word system. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by the chip enables (either \( \overline{CE}_0 \) or \( \overline{CE}_1 \)) permit the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 440mW of power.

The IDT70V28 is packaged in a 100-pin Thin Quad Flatpack (TQFP).

Pin Configurations\(^{(1,2,3)}\)

![Pin Configuration Diagram]

**NOTES:**

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground.
3. Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
### Absolute Maximum Ratings\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTERM(^{(2)})</td>
<td>Terminal Voltage</td>
<td>-0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>with Respect to GND</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TBIAS</td>
<td>Temperature Under Bias</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to < 20mA for the period of VTERM \(\geq\) Vcc + 0.3V.

### Recommended DC Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>—</td>
<td>Vcc + 0.3(^{(2)})</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.3(^{(1)})</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTES:**
1. VIL \(\geq\) -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 0.3V.

### Capacitance\(^{(1)}\) \((TA = +25°C, f = 1.0 MHz)\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions(^{(2)})</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN</td>
<td>Input Capacitance</td>
<td>VN = 3dV</td>
<td>9</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output Capacitance</td>
<td>VOUT = 3dV</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

### Maximum Operating Temperature and Supply Voltage

<table>
<thead>
<tr>
<th>Grade</th>
<th>Ambient Temperature(^{(3)})</th>
<th>GND</th>
<th>Vcc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>0V</td>
<td>3.3V ± 0.3V</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>0V</td>
<td>3.3V ± 0.3V</td>
</tr>
</tbody>
</table>

**NOTE:**
1. This is the parameter Ta. This is the "instant on" case temperature.
**Truth Table I – Chip Enable**

<table>
<thead>
<tr>
<th>CE0</th>
<th>CEb</th>
<th>CE1</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>VIL</td>
<td>VIL</td>
<td>Port Selected (TTL Active)</td>
</tr>
<tr>
<td></td>
<td>≤ 0.2V</td>
<td>≥VCC -0.2V</td>
<td>Port Selected (CMOS Active)</td>
</tr>
<tr>
<td>H</td>
<td>VIL</td>
<td>X</td>
<td>Port Deselected (TTL Inactive)</td>
</tr>
<tr>
<td></td>
<td>≥VCC -0.2V</td>
<td>X(3)</td>
<td>Port Deselected (CMOS Inactive)</td>
</tr>
<tr>
<td></td>
<td>X(3)</td>
<td>≤0.2V</td>
<td>Port Deselected (CMOS Inactive)</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Chip Enable references are shown above with the actual CE0 and CE1 levels; CE is a reference only.
2. ‘H’ = VIL and ‘L’ = VIL.
3. CMOS standby requires ‘X’ to be either ≤ 0.2V or ≥VCC-0.2V.

**Truth Table II – Non-Contention Read/Write Control**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE0</td>
<td>R/W</td>
<td>OE</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**NOTES:**
1. AIL — A15L ≠ A0R — A15R.
2. Refer to Truth Table I - Chip Enable.

**Truth Table III – Semaphore Read/Write Control**

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>CE0</td>
<td>R/W</td>
<td>OE</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>↑</td>
<td>X</td>
</tr>
<tr>
<td>X</td>
<td>↑</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**NOTES:**
1. There are eight semaphore flags written to I/Oi and read from all the I/Os (I/O0-I/O15). These eight semaphore flags are addressed by A0-A7.
2. Refer to Truth Table I - Chip Enable.
### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 3.3V ± 0.3V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>70V28L</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min.</td>
</tr>
<tr>
<td></td>
<td>ILI</td>
<td>Input Leakage Current(1)</td>
<td>Vcc = 3.6V, Vin = 0V to Vcc</td>
</tr>
<tr>
<td></td>
<td>ILO</td>
<td>Output Leakage Current CE(2) = VH, VOUT = 0V to Vcc</td>
<td>—</td>
</tr>
<tr>
<td>Vol</td>
<td>Output Low Voltage</td>
<td>IOL = +4mA</td>
<td>—</td>
</tr>
<tr>
<td>Voh</td>
<td>Output High Voltage</td>
<td>IOH = -4mA</td>
<td>2.4</td>
</tr>
</tbody>
</table>

**NOTES:**
1. At Vcc ≤ 2.0V, input leakages are undefined.
2. Refer to Truth Table I - Chip Enable.

### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 3.3V ± 0.3V) (5)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Version</th>
<th>70V28L15</th>
<th>70V28L20</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Typ.(1)</td>
<td>Max.</td>
</tr>
<tr>
<td>ILCC</td>
<td>Dynamic Operating Current (Both Ports Active)</td>
<td>CE = VL, Outputs Disabled SEM = VH f = fMAX(2)</td>
<td>COM/L</td>
<td>145</td>
<td>235</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
</tr>
<tr>
<td>ISB1</td>
<td>Standby Current (Both Ports - TTL Level Inputs)</td>
<td>CE = CE = VH SEM = SEM = VH f = fMAX(2)</td>
<td>COM/L</td>
<td>40</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
</tr>
<tr>
<td>ISB2</td>
<td>Standby Current (One Port - TTL Level Inputs)</td>
<td>CE = CE = VL and CE = CE = VH(3) Active Port Outputs Disabled, f = fMAX(2), SEMR = SEML = VH</td>
<td>COM/L</td>
<td>100</td>
<td>155</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
</tr>
<tr>
<td>ISB3</td>
<td>Full Standby Current (Both Ports - All CMOS Level Inputs)</td>
<td>Both Ports CE = CE &gt; Vcc - 0.2V, Vin &gt; Vcc - 0.2V or Vin &lt; 0.2V, f = 0(5) SEMR = SEML &gt; Vcc - 0.2V</td>
<td>COM/L</td>
<td>0.2</td>
<td>3.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
</tr>
<tr>
<td>ISB4</td>
<td>Full Standby Current (One Port - All CMOS Level Inputs)</td>
<td>CE = CE &lt; 0.2V and CE = CE &gt; Vcc - 0.2V(6), SEMR = SEML &gt;= Vcc - 0.2V, Vin &gt; Vcc - 0.2V or Vin &lt; 0.2V, Active Port Outputs Disabled, f = fMAX(2)</td>
<td>COM/L</td>
<td>95</td>
<td>150</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>IND L</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Vcc = 3.3V, Ta = +25°C, and are not production tested; ILCC = 90mA (Typ.)
2. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/16c and using "AC Test Conditions" of input levels of GND to 3V.
3. f = 0 means no address or control lines change.
4. Port "A" may be either left or right. Port "B" is the opposite from port "A".
5. Refer to Truth Table I - Chip Enable.
AC Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Times</td>
<td>3ns Max.</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>Figures 1 and 2</td>
</tr>
</tbody>
</table>

NOTES:
1. Timing depends on which signal is asserted last, OE, CE, LB or UB.
2. Timing depends on which signal is de-asserted first CE, OE, LB or UB.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. SEM = VIL.
6. Refer to Truth Table I-Chip Enable

Waveform of Read Cycles\(^{(5)}\)

Timing of Power-Up Power-Down

NOTES:
1. Timing depends on which signal is asserted last, CE, OE, LB or UB.
2. Timing depends on which signal is de-asserted first CE, OE, LB or UB.
3. tBDD delay is required only in cases where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA or tBDD.
5. SEM = VIL.
6. Refer to Truth Table I-Chip Enable

* Including scope and jig.
### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>70V28L15 Com’l Only</th>
<th>70V28L20 Com’l &amp; Ind</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td><strong>READ CYCLE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>tAA</td>
<td>Address Access Time</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>tACE</td>
<td>Chip Enable Access Time&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>tABE</td>
<td>Byte Enable Access Time&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>tAOE</td>
<td>Output Enable Access Time</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tOH</td>
<td>Output Hold from Address Change</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tLZ</td>
<td>Output Low-Z Time&lt;sup&gt;(1,2)&lt;/sup&gt;</td>
<td>3</td>
<td>—</td>
</tr>
<tr>
<td>tHZ</td>
<td>Output High-Z Time&lt;sup&gt;(1,2)&lt;/sup&gt;</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tRU</td>
<td>Chip Enable to Power Up Time&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>tPD</td>
<td>Chip Disable to Power Down Time&lt;sup&gt;(2)&lt;/sup&gt;</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>tSOP</td>
<td>Semaphore Flag Update Pulse (OE or SEM)</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>tSAA</td>
<td>Semaphore Address Access Time</td>
<td>—</td>
<td>15</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>70V28L15 Com’l Only</th>
<th>70V28L20 Com’l &amp; Ind</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td><strong>WRITE CYCLE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>15</td>
<td>20</td>
</tr>
<tr>
<td>tEW</td>
<td>Chip Enable to End-of-Write&lt;sup&gt;(5)&lt;/sup&gt;</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tAW</td>
<td>Address Valid to End-of-Write</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-up Time&lt;sup&gt;(3)&lt;/sup&gt;</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>tWP</td>
<td>Write Pulse Width</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>tDV</td>
<td>Data Valid to End-of-Write</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>tHZ</td>
<td>Output High-Z Time&lt;sup&gt;(1,2)&lt;/sup&gt;</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>tWZ</td>
<td>Write Enable to Output in High-Z&lt;sup&gt;(1,2)&lt;/sup&gt;</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tOW</td>
<td>Output Active from End-of-Write&lt;sup&gt;(2,4)&lt;/sup&gt;</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>tSRD</td>
<td>SEM Flag Write to Read Time</td>
<td>5</td>
<td>—</td>
</tr>
<tr>
<td>tPS</td>
<td>SEM Flag Contention Window</td>
<td>5</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, CE = VIL and SEM = VIL. To access semaphore, CE = VIL and SEM = VIH. Either condition must be valid for the entire tEW time.
4. The specification for tOW must be met by the device supplying write data to the RAM under all operating conditions. Although tOW values will vary over voltage and temperature, the actual tOW will always be smaller than the actual tOW.

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Timing Waveform of Write Cycle No. 1, R/W Controlled Timing\(^{(1,5,8)}\)

**NOTES:**
1. R/W or CE or UB and LB = V\text{IH} during all address transitions.
2. A write occurs during the overlap (twz or twp) of a CE = V\text{IL} and a R/W = V\text{IL} for memory array writing cycle.
3. twz is measured from the earlier of CE or R/W (or SEM or R/W) going HIGH to the end of write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CE or SEM = V\text{IL} transition occurs simultaneously with or after the R/W = V\text{IL} transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal is asserted last, CE or R/W.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If CE = V\text{IL} during R/W controlled write cycle, the write pulse width must be the larger of twp or (twz + tdw) to allow the I/O drivers to turn off and data to be placed on the bus for the required tdw. If CE = V\text{IL} during an R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified.
9. To access RAM, CE = V\text{IL} and SEM = V\text{IH}. To access semaphore, CE = V\text{IL} and SEM = V\text{IL}. twz must be met for either condition.
10. Refer to Truth Table I - Chip Enable.
Timing Waveform of Semaphore Read after Write Timing, Either Side\(^{(1)}\)

NOTES:
1. \(\overline{CE} = \overline{UB} = \text{VIH}\) or \(\overline{LB} = \text{VIH}\) for the duration of the above timing (both write and read cycle) (Refer to Chip Enable Truth Table).
2. "DATA OUT VALID" represents all I/O's (I/O0 - I/O15) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention\(^{(1,3,4)}\)

NOTES:
1. \(\overline{CE} = \overline{LB} = \overline{VIH}\) and \(\overline{UB} = \text{VIH}\) for the duration of the above timing (both write and read cycle) (Refer to Chip Enable Truth Table).
2. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from \(R/W\) or \(SEM\) going HIGH to \(R/W\) or \(SEM\) going HIGH.
4. If \(tsps\) is not satisfied the semaphore will fall positively to one side or the other, but there is no guarantee which side will be granted the semaphore flag.
## AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>70V28L15 Com‘l Only</th>
<th>70V28L20 Com‘l &amp; Ind</th>
<th>Unit</th>
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</thead>
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<tr>
<td>BUSY TIMING (M/Ś=Vih)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tBAA</td>
<td>BUSY Access Time from Address Match</td>
<td>---</td>
<td>15</td>
<td>---</td>
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<tr>
<td>tBDA</td>
<td>BUSY Disable Time from Address Not Matched</td>
<td>---</td>
<td>15</td>
<td>---</td>
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<tr>
<td>tBAC</td>
<td>BUSY Access Time from Chip Enable Low</td>
<td>---</td>
<td>15</td>
<td>---</td>
</tr>
<tr>
<td>tBDC</td>
<td>BUSY Access Time from Chip Enable High</td>
<td>---</td>
<td>15</td>
<td>---</td>
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<tr>
<td>tAPS</td>
<td>Arbitration Priority Set-up Time(2)</td>
<td>5</td>
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<td>5</td>
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<tr>
<td>tBDD</td>
<td>BUSY Disable to Valid Data(3)</td>
<td>---</td>
<td>15</td>
<td>---</td>
</tr>
<tr>
<td>tWH</td>
<td>Write Hold After BUSY(6)</td>
<td>12</td>
<td>---</td>
<td>15</td>
</tr>
<tr>
<td>BUSY TIMING (M/Ś=Vil)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWB</td>
<td>BUSY Input to Write(4)</td>
<td>0</td>
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<td>0</td>
</tr>
<tr>
<td>tWH</td>
<td>Write Hold After BUSY(6)</td>
<td>12</td>
<td>---</td>
<td>15</td>
</tr>
<tr>
<td>PORT-TO-PORT DELAY TIMING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWDD</td>
<td>Write Pulse to Data Delay(1)</td>
<td>---</td>
<td>30</td>
<td>---</td>
</tr>
<tr>
<td>tCDD</td>
<td>Write Data Valid to Read Data Delay(1)</td>
<td>---</td>
<td>25</td>
<td>---</td>
</tr>
</tbody>
</table>

### NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and BUSY (M/Ś = Vih)".
2. To ensure that the earlier of the two ports wins.
3. tACO is a calculated parameter and is the greater of 0, tWDD – tWP (actual), or tCDO – tCW (actual).
4. To ensure that the write cycle is inhibited on port “B” during contention on port “A”.
5. To ensure that a write cycle is completed on port “B” after contention on port “A”.

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Timing Waveform of Write with Port-to-Port Read and \( \text{BUSY} (M/S = \text{V\_IH})^{(2,4,5)} \)

![Timing Waveform Diagram]

NOTES:
1. To ensure that the earlier of the two ports wins, \( t\text{APS} \) is ignored for \( M/S = \text{V\_IL} \) (SLAVE).
2. \( \text{CE}_L = \text{CE}_R = \text{V\_IL} \), refer to Chip Enable Truth Table.
3. \( \text{CE} = \text{V\_IL} \) for the reading port.
4. If \( M/S = \text{V\_IL} \) (slave), \( \text{BUSY} \) is an input. Then for this example \( \text{BUSY}\_A = \text{V\_IH} \) and \( \text{BUSY}\_B \) input is shown above.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

Timing Waveform of Write with \( \text{BUSY} (M/S = \text{V\_IL}) \)

![Timing Waveform Diagram]

NOTES:
1. \( t\text{WH} \) must be met for both \( \text{BUSY} \) input (SLAVE) and output (MASTER).
2. \( \text{BUSY} \) is asserted on port "B" blocking \( \text{R/W} \), until \( \text{BUSY}\_B \) goes HIGH.
3. \( t\text{WH} \) is only for the 'slave' version.
Waveform of \textbf{BUSY} Arbitration Controlled by $\overline{CE}$ Timing ($M/S = V_{IH}$)$^{(1,3)}$

\begin{itemize}
  \item ADDR'^{A}$ and "B"
  \item ADDRESS "A" and "B"
  \item $\overline{CE}^{'A}$
  \item $\overline{CE}^{'B}$
  \item BUSY$^{'B}$
\end{itemize}

NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from port “A”.
2. If $t_{APS}$ is not satisfied, the BUSY signal will be asserted on one side or another but there is no guarantee on which side BUSY will be asserted.
3. Refer to Truth Table I - Chip Enable.

Waveform of \textbf{BUSY} Arbitration Cycle Controlled by Address Match Timing ($M/S = V_{IH}$)$^{(1)}$

\begin{itemize}
  \item ADDR"A" and "B"
  \item ADDRESS "N"
  \item MATCHING ADDRESS "N"
  \item $t_{APS}^{(2)}$
  \item $t_{BAC}$
  \item $t_{BDA}$
\end{itemize}

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|c|c|c|}
\hline
Symbol & Parameter & $70V28L15$ & & $70V28L20$ & \\
& & Min. & Max. & Min. & Max. & Unit \hline
INTERRUPT TIMING & & & & & & \\
IAS & Address Set-up Time & 0 & — & 0 & — & ns \\
INS & Write Recovery Time & 0 & — & 0 & — & ns \\
INS & Interrupt Set Time & — & 15 & — & 20 & ns \\
INR & Interrupt Reset Time & — & 15 & — & 20 & ns \\
\hline
\end{tabular}
\end{table}
Waveform of Interrupt Timing\(^{(1,5)}\)

NOTES:
1. All timing is the same for left and right ports. Port “A” may be either the left or right port. Port “B” is the port opposite from port “A”.
2. Refer to Interrupt Truth Table.
3. Timing depends on which enable signal (\(CE\) or \(R/W\)) is asserted last.
4. Timing depends on which enable signal (\(CE\) or \(R/W\)) is de-asserted first.
5. Refer to Truth Table I - Chip Enable.

Truth Table IV — Interrupt Flag\(^{(1,4,5)}\)

<table>
<thead>
<tr>
<th>Left Port</th>
<th>Right Port</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. Assumes \(BUSY_L = BUSY_R = V_H\).
2. If \(BUSY_L = V_L\), then no change.
3. If \(BUSY_R = V_L\), then no change.
4. \(INT_L\) and \(INT_R\) must be initialized at power-up.
5. Refer to Truth Table I - Chip Enable.
Functional Description

The IDT70V28 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT70V28 has an automatic power down feature controlled by CE. The CE0 and CE1 control the on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (CE = HIGH). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mailbox or message center) is assigned to each port. The left port interrupt flag (INTL) is asserted when the right port writes to memory location FFFE (HEX), where a write is defined as CE = R/W = VIL per Truth Table IV. The left port clears the interrupt through access of address location FFFE when CE0 = CE1 = VIL, R/W is a "don't care". Likewise, the right port interrupt flag (INTR) is asserted when the left port writes to memory location FFFF (HEX) and to clear the interrupt flag (INTR), the right port must read the memory location FFFF. The message (16 bits) at FFFE or FFFF is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations FFFE and FFFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table IV for the interrupt operation.
Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “Busy”. The BUSY pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a BUSY indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the BUSY logic can be disabled by placing the part in slave mode with the M/S pin. Once in slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT70V28 RAM in master mode, are push-pull type outputs and do not require pull up resistors to operate. If these RAMs are being expanded in depth, then the BUSY indication for the resulting array requires the use of an external AND gate.

![Diagram of BUSY Logic](image)

Figure 3. Busy and chip enable routing for both width and depth expansion with IDT70V28 RAMs.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT70V28 RAM array in width while using BUSY logic, one master part is used to decide which side of the RAMs array will receive a BUSY indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master use the BUSY signal as a write inhibit signal. Thus on the IDT70V28 RAM the BUSY pin is an output if the part is used as a master (M/S pin = VIL), and the BUSY pin is an input if the part used as a slave (M/S pin = VIH) as shown in Figure 3.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating BUSY on one side of the array and another master indicating BUSY on the other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration on a master is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a BUSY flag to be output from the master before the actual write pulse can be initiated with the R/W signal. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Semaphores

The IDT70V28 is an extremely fast Dual-Port 64K x 16 CMOS Static RAM with an additional 8 address locations dedicated to binary semaphore flags. These flags allow either processor on the left or right side of the Dual-Port RAM to claim a privilege over the other processor for functions defined by the system designer’s software. As an example, the semaphore can be used by one processor to inhibit the other from accessing a portion of the Dual-Port RAM or any other shared resource.

The Dual-Port RAM features a fast access time, with both ports being completely independent of each other. This means that the activity on the left port in no way slows the access time of the right port. Both ports are identical in function to standard CMOS Static RAM and can be read from or written to at the same time with the only possible conflict arising from the simultaneous writing of, or a simultaneous READ/_WRITE of, a non-semaphore location. Semaphores are protected against such ambiguous situations and may be used by the system program to avoid any conflicts in the non-semaphore portion of the Dual-Port RAM. These devices have an automatic power-down feature controlled by CE, the Dual-Port RAM enable, and SEM, the semaphore enable. The CE and SEM pins control on-chip power down circuitry that permits the respective port to go into standby mode when not selected. This is the condition which is shown in Truth Table III where CE and SEM are both HIGH.

Systems which can best use the IDT70V28 contain multiple processors or controllers and are typically very high-speed systems which are software controlled or software intensive. These systems can benefit from a performance increase offered by the IDT70V28s hardware semaphores, which provide a lockout mechanism without requiring complex programming.

Software handshaking between processors offers the maximum in system flexibility by permitting shared resources to be allocated in varying configurations. The IDT70V28 does not use its semaphore flags to control any resources through hardware, thus allowing the system designer total flexibility in system architecture.

An advantage of using semaphores rather than the more common methods of hardware arbitration is that wait states are never incurred in either processor. This can prove to be a major advantage in very high-speed systems.

How the Semaphore Flags Work

The semaphore logic is a set of eight latches which are independent of the Dual-Port RAM. These latches can be used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphores provide a hardware assist for a use assignment method called “Token Passing Allocation.” In this method, the state of a semaphore latch is used as a token indicating that a shared resource is in use. If the left processor wants to use this resource, it requests the token by setting the latch. This processor then
verifies its success in setting the latch by reading it. If it was successful, it
proceeds to assume control over the shared resource. If it was not
successful in setting the latch, it determines that the right side
processor has set the latch first, has the token and is using the shared
resource. The left processor can then either repeatedly request that
semaphore’s status or remove its request for that semaphore to
perform another task and occasionally attempt again to gain control of
the token via the set and test sequence. Once the right side has
relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by
writing a zero into a semaphore latch and is released when the same
side writes a one to that latch.

The eight semaphore flags reside within the IDT70V28 in a
separate memory space from the Dual-Port RAM. This address space
is accessed by placing a low input on the SEM pin (which acts as a chip
select for the semaphore flags) and using the other control pins
(Address, CE, and R/W) as they would be used in accessing a
standard Static RAM. Each of the flags has a unique address which
can be accessed by either side through address pins A0 – A2. When
accessing the semaphores, none of the other address pins has any
effect.

When writing to a semaphore, only data pin Do is used. If a low level
is written into an unused semaphore location, that flag will be set to a
zero on that side and a one on the other side (see Truth Table VI). That
semaphore can now only be modified by the side showing the zero.
When a one is written into the same location from the same side, the
flag will be set to a one for both sides (unless a semaphore request
from the other side is pending) and can then be written to by both sides.
The fact that the side which is able to write a zero into a semaphore
subsequently locks out writes from the other side is what makes
semaphore flags useful in interprocessor communications. (A thorough
discussion on the use of this feature follows shortly.) A zero
written into the same location from the other side will be stored in the
semaphore request latch for that side until the semaphore is freed by
the first side.

When a semaphore flag is read, its value is spread into all data bits
so that a flag that is a one reads as a one in all data bits and a flag
containing a zero reads as all zeros. The read value is latched into one
side’s output register when that side’s semaphore select (SEM) and
output enable (OE) signals go active. This serves to disallow the
semaphore from changing state in the middle of a read cycle due to a
write cycle from the other side. Because of this latch, a repeated read
of a semaphore in a test loop must cause either signal (SEM or OE) to
go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in
order to guarantee that no system level contention will occur. A
processor requests access to shared resources by attempting to write
a zero into a semaphore location. If the semaphore is already in use,
the semaphore request latch will contain a zero, yet the semaphore
flag will appear as one, a fact which the processor will verify by the
subsequent read (see Table VI). As an example, assume a processor
writes a zero to the left port at a free semaphore location. On a
subsequent read, the processor will verify that it has written success-
fully to that location and will assume control over the resource in
question. Meanwhile, if a processor on the right side attempts to write
a zero to the same semaphore flag it will fail, as will be verified by the

It is important to note that a failed semaphore request must be
followed by either repeated reads or by writing a one into the same
location. The reason for this is easily understood by looking at the
simple logic diagram of the semaphore flag in Figure 4. Two sema-
phore request latches feed into a semaphore flag. Whichever latch is
first to present a zero to the semaphore flag will force its side of the
semaphore flag LOW and the other side HIGH. This condition will
continue until a one is written to the same semaphore request latch.
Should the other side’s semaphore request latch have been written to

Figure 4. IDT70V28 Semaphore Logic

<table>
<thead>
<tr>
<th>L PORT</th>
<th>SEMAPHORE REQUEST FLIP FLOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>WRITE</td>
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<td>SEMAPHORE READ</td>
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<table>
<thead>
<tr>
<th>R PORT</th>
<th>SEMAPHORE REQUEST FLIP FLOP</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0</td>
<td>WRITE</td>
</tr>
<tr>
<td>SEMAPHORE READ</td>
<td></td>
</tr>
</tbody>
</table>

fact that a one will be read from that semaphore on the right side during
subsequent read. Had a sequence of READ/WRITE been used
instead, system contention problems could have occurred during the
gap between the read and write cycles.

The critical case of semaphore timing is when both sides request
a single token by attempting to write a zero into it at the same time. The
semaphore logic is specially designed to resolve this problem. If
simultaneous requests are made, the logic guarantees that only one
side receives the token. If one side is earlier than the other in making
the request, the first side to make the request will receive the token. If
both requests arrive at the same time, the assignment will be arbitrarily
made to one port or the other.

One caution that should be noted when using semaphores is that
semaphores alone do not guarantee that access to a resource is
secure. As with any powerful programming technique, if semaphores
are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be
handled via the initialization program at power-up. Since any sema-
phore request flag which contains a zero must be reset to a one,
all semaphores on both sides should have a one written into them
at initialization from both sides to assure that they will be free
when needed.
### Ordering Information

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Power</th>
<th>Speed</th>
<th>Package</th>
<th>Process/ Temperature Range</th>
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<td>A</td>
<td>A</td>
<td>A</td>
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</table>

- **Blank** Tray Tape and Reel
- **Blank**\(^{(1)}\) Commercial (0°C to +70°C) Industrial (-40°C to +85°C)
- **G** Green
- **PF** 100-pin TQFP (PNG100)
- **15** Commercial Only
- **20** Commercial & Industrial Speed in nanoseconds
- **L** Low Power

#### 70V28 1024K (64K x 16) Dual-Port RAM

**NOTES:**

1. Contact your sales office for Industrial Temperature range in other speeds, packages and powers.
2. LEAD FINISH (SnPb) are Obsolete - Product Discontinuation Notice - PDN#SP-17-02
   - Note that information regarding recently obsoleted parts is included in this datasheet for customer convenience.

### Orderable Part Information

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<th>Pkg. Type</th>
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</table>
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(Rev.4.0-1 November 2017)