HIGH SPEED  2K X 8 DUAL-PORT  STATIC RAM  WITH INTERRUPTS

Features

- **High-speed access**
  - Commercial: 20/35/55ns (max.)
  - Industrial: 25/55ns (max.)

- **Low-power operation**
  - IDT71321/IDT71421SA
    - Active: 325mW (typ.)
    - Standby: 5mW (typ.)
  - IDT71321/421LA
    - Active: 325mW (typ.)
    - Standby: 1mW (typ.)

- **Two INT flags for port-to-port communications**

- **MASTER IDT71321 easily expands data bus width to 16-or-more-bits using SLAVE IDT71421**

- **On-chip port arbitration logic (IDT71321 only)**

- **BUSY output flag on IDT71321; BUSY input on IDT71421**

- **Fully asynchronous operation from either port**

- **Battery backup operation – 2V data retention (LA only)**

- **TTL-compatible, single 5V ±10% power supply**

- **Available in 52-Pin PLCC, 52-Pin STQFP, 64-Pin TQFP, and 64-Pin STQFP**

- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**

- **Green parts available, see ordering information**

Functional Block Diagram

NOTES:

1. IDT71321 (MASTER): BUSY is open drain output and requires pullup resistor of 270Ω.
   IDT71421 (SLAVE): BUSY is input.
2. Open drain output: requires pullup resistor of 270Ω.
Description

The IDT71321/IDT71421 are high-speed 2K x 8 Dual-Port Static RAMs with internal interrupt logic for interprocessor communications. The IDT71321 is designed to be used as a stand-alone 8-bit Dual-Port Static RAM or as a "MASTER" Dual-Port Static RAM together with the IDT71421 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port Static RAM approach in 16-or-more-bit memory system applications results in full speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by \( CE \), permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using CMOS high-performance technology, these devices typically operate on only 325mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200\( \mu \)W from a 2V battery.

The IDT71321/IDT71421 devices are packaged in 52-pin PLCC, 52-pin STQFP, 64-pin TQFP, and 64-pin STQFP.

Pin Configurations\(^{(1,2,3)}\)

![Pin Configuration Diagram]

NOTES:

1. All \( V_{CC} \) pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PLG52 package body is approximately .75 in x .75 in x .17 in.
   PNG64 package body is approximately 14mm x 14mm x 1.4mm.
   PPG64 package body is approximately 10mm x 10mm x 1.4mm.
4. This package code is used to reference the package diagram.
Pin Configurations (continued)$^{(1,2,3)}$

![Diagram of pin configurations]

**NOTES:**
1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. PPG52 package body is approximately 10mm x 10mm x 1.4mm.
4. This package code is used to reference the package diagram.

---

**Capacitance$^{(1)}$**

(TA = +25°C, f = 1.0MHz) TQFP Only

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions$^{(2)}$</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td>V IN = 3dV</td>
<td>9</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output Capacitance</td>
<td>V OUT = 3dV</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

---

**Recommended Operating Temperature and Supply Voltage$^{(1,2)}$**

<table>
<thead>
<tr>
<th>Grade</th>
<th>Ambient Temperature</th>
<th>GND</th>
<th>Vcc</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>0V</td>
<td>5.0V ± 10%</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>0V</td>
<td>5.0V ± 10%</td>
</tr>
</tbody>
</table>

**NOTES:**
1. This is the parameter TA. This is the "instant on" case temperature.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

---

**Recommended DC Operating Conditions**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>Supply Voltage</td>
<td>4.5</td>
<td>5.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>VH</td>
<td>Input High Voltage</td>
<td>2.2</td>
<td></td>
<td>6.0$^{(2)}$</td>
<td>V</td>
</tr>
<tr>
<td>VL</td>
<td>Input Low Voltage</td>
<td>-0.5$^{(1)}$</td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTES:**
1. VIH (min.) = -1.5V for pulse width less than 10ns.
2. VTERM must not exceed VCC + 10%.

---

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ VCC + 10%.

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### DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range\(^{(1,4)}\) (Vcc = 5.0V ± 10%)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Version</th>
<th>71321X20</th>
<th>71421X20</th>
<th>71321X25</th>
<th>71421X25</th>
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<tr>
<td></td>
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<td>Typ</td>
<td>Max</td>
<td>Typ</td>
<td>Max</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>COM’L</td>
<td>SA</td>
<td>110</td>
<td>250</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>110</td>
<td>200</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND</td>
<td>SA</td>
<td>—</td>
<td>—</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>—</td>
<td>—</td>
<td>110</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>COM’L</td>
<td>SA</td>
<td>30</td>
<td>65</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>30</td>
<td>45</td>
<td>30</td>
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<td></td>
<td></td>
<td>IND</td>
<td>SA</td>
<td>—</td>
<td>—</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>—</td>
<td>—</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>COM’L</td>
<td>SA</td>
<td>65</td>
<td>165</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>65</td>
<td>125</td>
<td>65</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>IND</td>
<td>SA</td>
<td>—</td>
<td>—</td>
<td>65</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>LA</td>
<td>—</td>
<td>—</td>
<td>65</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>COM’L</td>
<td>SA</td>
<td>1.0</td>
<td>15</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>0.2</td>
<td>5</td>
<td>0.2</td>
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<td></td>
<td></td>
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<td>IND</td>
<td>SA</td>
<td>—</td>
<td>—</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>—</td>
<td>—</td>
<td>0.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>COM’L</td>
<td>SA</td>
<td>60</td>
<td>155</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<td>LA</td>
<td>60</td>
<td>115</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IND</td>
<td>SA</td>
<td>—</td>
<td>—</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>LA</td>
<td>—</td>
<td>—</td>
<td>60</td>
</tr>
</tbody>
</table>

### NOTES:
1. ‘X’ in part numbers indicates power rating (SA or LA).
2. At f = f_{\text{MAX}}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/\text{t_{RC}}, and using “AC TEST CONDITIONS” of input levels of GND to 3V.
3. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
4. Vcc = 5V, T_{\text{MAX}} = +25°C for Typ and is not production tested. Vcc DC = 100mA (Typ)
5. Port “A” may be either left or right port. Port “B” is opposite from port “A”.

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DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Input Leakage Current(1)</td>
<td>VCC = 5.5V, VIN = 0V to VCC</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Output Leakage Current(1)</td>
<td>ĈE = VIH, VOUT = 0V to VCC, VCC - 5.5V</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Output Low Voltage (IOL=IOL)</td>
<td>IOL = 4mA</td>
<td>—</td>
<td>0.4</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Open Drain Output Low Voltage (BUSY/INT)</td>
<td>IOL = 16mA</td>
<td>—</td>
<td>0.5</td>
<td>—</td>
<td>0.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Output High Voltage</td>
<td>IOH = -4mA</td>
<td>2.4</td>
<td>—</td>
<td>2.4</td>
<td>—</td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTE:**
1. At Vcc ≤ 2.0V leakages are undefined.

Data Retention Characteristics (LA Version Only)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Vcc for Data Retention</td>
<td>VCC = 2.0V, ĈE ≥ VCC - 0.2V</td>
<td>2.0</td>
<td>—</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Data Retention Current</td>
<td>VCC = 2.0V, ĈE ≥ VCC - 0.2V</td>
<td>COM'L</td>
<td>—</td>
<td>100</td>
<td>1500</td>
</tr>
<tr>
<td></td>
<td>Chip Deselect to Data Retention Time</td>
<td>0</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Operation Recovery Time</td>
<td>trC(2)</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**
1. Vcc = 2V, Ta = +25°C, and is not production tested.
2. trc = Read Cycle Time
3. This parameter is guaranteed but not production tested.

Data Retention Waveform
## AC Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Times</td>
<td>5ns</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>Figures 1, 2 and 3</td>
</tr>
</tbody>
</table>

*100pF for 55ns versions

---

**Figure 1. AC Output Test Load**

![AC Output Test Load](image1)

**Figure 2. Output Test Load**

(for tH, tL, tHZ, and tOW)

* Including scope and jig.

![Output Test Load](image2)

**Figure 3. BUSY and INT**

![BUSY and INT Test Load](image3)

*100pF for 55ns versions

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### AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range(2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>71321X20 71421X20</th>
<th>71321X25 71421X25</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td><strong>READ CYCLE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>tAA</td>
<td>Address Access Time</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>tAC</td>
<td>Chip Enable Access Time</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>tAOE</td>
<td>Output Enable Access Time</td>
<td>—</td>
<td>11</td>
</tr>
<tr>
<td>tOH</td>
<td>Output Hold from Address Change</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tLZ</td>
<td>Output Low-Z Time(1,3)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tHZ</td>
<td>Output High-Z Time(1,3)</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tPU</td>
<td>Chip Enable to Power Up Time(3)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tPD</td>
<td>Chip Disable to Power Down Time(3)</td>
<td>—</td>
<td>20</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>71321X35 71421X35</th>
<th>71321X55 71421X55</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td><strong>READ CYCLE</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>35</td>
<td>55</td>
</tr>
<tr>
<td>tAA</td>
<td>Address Access Time</td>
<td>—</td>
<td>35</td>
</tr>
<tr>
<td>tAC</td>
<td>Chip Enable Access Time</td>
<td>—</td>
<td>35</td>
</tr>
<tr>
<td>tAOE</td>
<td>Output Enable Access Time</td>
<td>—</td>
<td>20</td>
</tr>
<tr>
<td>tOH</td>
<td>Output Hold from Address Change</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>tLZ</td>
<td>Output Low-Z Time(1,3)</td>
<td>0</td>
<td>5</td>
</tr>
<tr>
<td>tHZ</td>
<td>Output High-Z Time(1,3)</td>
<td>—</td>
<td>15</td>
</tr>
<tr>
<td>tPU</td>
<td>Chip Enable to Power Up Time(3)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>tPD</td>
<td>Chip Disable to Power Down Time(3)</td>
<td>—</td>
<td>35</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Transition is measured 0mV from Low or High-impedance voltage Output Test Load (Figure 2).
2. 'X' in part numbers indicates power rating (SA or LA).
3. This parameter is guaranteed by device characterization, but is not production tested.
Timing Waveform of Read Cycle No. 1, Either Side (1)

NOTES:
1. R/W = Vih, CE = Vih, and OE = VIL. Address is valid prior to the coincidental with CE transition LOW.
2. tBDD delay is required only in the case where the opposite port is completing a write operation to the same address location. For simultaneous read operations BUSY has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

Timing Waveform of Read Cycle No. 2, Either Side (3)

NOTES:
1. Timing depends on which signal is asserted last, OE or CE.
2. Timing depends on which signal is de-asserted first, OE or CE.
3. R/W = Vih and OE = VIL, and the address is valid prior to or coincidental with CE transition LOW.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.
AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>71321X20</th>
<th>71421X20</th>
<th>71321X25</th>
<th>71421X25</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>WRITE CYCLE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>20</td>
<td>25</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tEW</td>
<td>Chip Enable to End-of-Write</td>
<td>15</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAW</td>
<td>Address Valid to End-of-Write</td>
<td>15</td>
<td>20</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tAS</td>
<td>Address Set-up Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWP</td>
<td>Write Pulse Width</td>
<td>15</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDW</td>
<td>Data Valid to End-of-Write</td>
<td>10</td>
<td>12</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tHZ</td>
<td>Output High-Z Time</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>0</td>
<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWE</td>
<td>Write Enable to Output in High-Z</td>
<td>10</td>
<td>10</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tOW</td>
<td>Output Active from End-of-Write</td>
<td>0</td>
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<td>WRITE CYCLE</td>
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<td>0</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>tWE</td>
<td>Write Enable to Output in High-Z</td>
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<td>30</td>
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<td>0</td>
<td>ns</td>
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NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
2. For Master/Slave combination, tWC = tAAB + tWP, since R/W = VIL must occur after tAAB.
3. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (tHZ + tOW) to allow the I/O drivers to turn off data to be placed on the bus for the required tOW. If OE is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.
4. ‘X’ in part numbers indicates power rating (SA or LA).
Timing Waveform of Write Cycle No. 1, (R/W Controlled Timing)$^{(1,5,8)}$

### Timing Waveform of Write Cycle No. 1, (R/W Controlled Timing)$^{(1,5,8)}$

#### Timing Waveform of Write Cycle No. 1, (R/W Controlled Timing)$^{(1,5,8)}$

**NOTES:**
1. R/W or CE must be HIGH during all address transitions.
2. A write occurs during the overlap ($t_{EW}$ or $t_{WP}$) of CE = VIL and R/W = VIL.
3. $t_{WR}$ is measured from the earlier of CE or R/W going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal (CE or R/W) is asserted last.
7. This parameter is determined to be device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
8. If CE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of $t_{WP}$ or ($twz + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required $t_{DW}$. If CE is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified $t_{WP}$.
### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (6)

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<td>tBAA</td>
<td>BUSY Access Time from Address</td>
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<tr>
<td>tBDA</td>
<td>BUSY Disable Time from Address</td>
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<td>tBAC</td>
<td>BUSY Access Time from Chip Enable</td>
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<td>tBDC</td>
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<td>tBDD</td>
<td>BUSY Disable to Valid Data(3)</td>
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<td>tBAA</td>
<td>BUSY Access Time from Address</td>
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<td></td>
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<td>Unit</td>
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<td>BUSY INPUT TIMING (For SLAVE 71421)</td>
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<td>tWB</td>
<td>Write to BUSY Input(4)</td>
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<td>0</td>
<td></td>
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</tr>
<tr>
<td>tWH</td>
<td>Write Hold After BUSY(5)</td>
<td>12</td>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>tWDD</td>
<td>Write Pulse to Data Delay(1)</td>
<td></td>
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<td>Write Data Valid to Read Data Delay(1)</td>
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</tbody>
</table>

### NOTES:

1. Port-to-port delay through RAM cells from the writing port to the reading port, refer to “Timing Waveform of Write with Port-to-Port Read and BUSY.”
2. To ensure that the earlier of the two ports wins.
3. tccc is a calculated parameter and is the greater of 0, tvcc – tww (actual) or tcce – tww (actual).
4. To ensure that a write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part numbers indicates power rating (SA or LA).

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Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}^{(2,3,4)}$

NOTES:
1. To ensure that the earlier of the two ports wins. $t_{APS}$ is ignored for Slave (IDT71421).
2. $CE_L = CE_R = V_L$.
3. $OE = V_L$ for the reading port.
4. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".

Timing Waveform of Write with $BUSY^{(4)}$

NOTES:
1. $t_{WH}$ must be met for both $BUSY$ input (IDT71421, slave) or output (IDT71321, Master).
2. $BUSY$ is asserted on port "B" blocking R/$W^*$, until $BUSY^*$ goes HIGH.
3. $t_{WB}$ is only for the slave version (IDT71421).
4. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is opposite from port "A".
### Timing Waveform of \textbf{BUSY} Arbitration Controlled by \textbf{CE} Timing\(^{(1)}\)

![Timing Diagram](image)

### Timing Waveform of \textbf{BUSY} Arbitration Controlled by Address Match Timing\(^{(1)}\)

![Timing Diagram](image)

#### NOTES:
1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
2. If \(t_{APS}\) is not satisfied, the \textbf{BUSY} will be asserted on one side or the other, but there is no guarantee on which side \textbf{BUSY} will be asserted (IDT71321 only).

### AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
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<td>(t_{AS})</td>
<td>Address Set-up Time</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{WR})</td>
<td>Write Recovery Time</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>(t_{INS})</td>
<td>Interrupt Set Time</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>25</td>
<td>ns</td>
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<tr>
<td>(t_{INR})</td>
<td>Interrupt Reset Time</td>
<td>—</td>
<td>20</td>
<td>—</td>
<td>25</td>
<td>ns</td>
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#### NOTE:
1. "X" in part numbers indicates power rating (SA or LA).
AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range\(^{(1)}\)

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<td></td>
<td>Com'I Only</td>
<td>Com'I &amp; Ind</td>
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<tr>
<td>TAS</td>
<td>Address Set-up Time</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
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<td>—</td>
</tr>
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<td>TNS</td>
<td>Interrupt Set Time</td>
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<td>25</td>
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<td>45</td>
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<tr>
<td>TNR</td>
<td>Interrupt Reset Time</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>45</td>
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</table>

**NOTE:**
1. ‘X’ in part numbers indicates power rating (SA or LA).

Timing Waveform of Interrupt Mode\(^{(1)}\)

**Set INT**

Set INT

**Clear INT**

Clear INT

**NOTES:**
1. All timing is the same for left and right ports. Port “A” may be either left or right port. Port “B” is the opposite from port “A”.
2. See Interrupt Truth Table.
3. Timing depends on which enable signal (CE or R/W) is asserted last.
4. Timing depends on which enable signal (CE or R/W) is de-asserted first.
Truth Tables

Truth Table I. Non-Contention Read/Write Control\(^{(4)}\)

<table>
<thead>
<tr>
<th>Left or Right Port(^{(3)})</th>
<th>R/W</th>
<th>CE</th>
<th>OE</th>
<th>D0-7</th>
<th>Function</th>
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<tbody>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
<td>Z</td>
<td>Port Disabled and in Power-Down Mode, ISB2 or ISB4</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
<td>Z</td>
<td>(\overline{CE}_R = \overline{CE}_L = V_H), Power-Down Mode, ISB1 or ISB3</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>DATAIN</td>
<td>Data on Port Written Into Memory(^{(2)})</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>DATAOUT</td>
<td>Data in Memory Output on Port(^{(5)})</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>Z</td>
<td>High Impedance Outputs</td>
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</tr>
</tbody>
</table>

NOTES:
1. \(A_{0L} = A_{10L} \neq A_{0R} = A_{10R}\).
2. If \(BUSY = L\), data is not written.
3. If \(BUSY = L\), data may not be valid, see \(t_{dCC}\) and \(t_{dCO}\) timing.
4. '\(H' = V_H', '\(L' = V_L', '\(X' = DON'T\ CARE', '\(Z' = HIGH\ IMPEDANCE\)

Truth Table II. Interrupt Flag\(^{(1,4)}\)

<table>
<thead>
<tr>
<th>Left Port</th>
<th>R/W</th>
<th>CE</th>
<th>OE</th>
<th>A10-A0L</th>
<th>INTR</th>
<th>Right Port</th>
<th>R/W</th>
<th>CE</th>
<th>OE</th>
<th>A10-A0R</th>
<th>INTR</th>
<th>Function</th>
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</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>X</td>
<td>7F</td>
<td>(X)</td>
<td>(X)</td>
<td>L(^{(2)})</td>
<td>Set Right INTR Flag</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>(X)</td>
<td>(L)</td>
<td>Reset Right INTR Flag</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>(L)(^{(3)})</td>
<td>(L)</td>
<td>(L)</td>
<td>(7FE)</td>
<td>Set Left INTR Flag</td>
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<td></td>
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<tr>
<td>X</td>
<td>L</td>
<td>L</td>
<td>(7FE)</td>
<td>(H)(^{(4)})</td>
<td>(X)</td>
<td>(X)</td>
<td>(X)</td>
<td>X</td>
<td>Reset Left INTR Flag</td>
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</tbody>
</table>

NOTES:
1. Assumes \(BUSY_L = BUSY_R = V_H\)
2. If \(BUSY_L = V_H\), then No Change.
3. If \(BUSY_R = V_H\), then No Change.
4. '\(H' = HIGH', '\(L' = LOW', '\(X' = DON'T\ CARE\)

Truth Table III — Address \(BUSY\) Arbitration

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Outputs</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CEL</td>
<td>(CE_R)</td>
<td>(A10-A0L)</td>
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<td>X</td>
<td>X</td>
<td>NO MATCH</td>
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<tr>
<td>H</td>
<td>X</td>
<td>MATCH</td>
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<tr>
<td>X</td>
<td>H</td>
<td>MATCH</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>MATCH</td>
</tr>
</tbody>
</table>

NOTES:
1. Pins \(BUSY_L\) and \(BUSY_R\) are both outputs for \(IDT71321\) (Master). Both are inputs for \(IDT71421\) (Slave). \(BUSY_X\) outputs on the \(IDT71321\) are open drain, not push-pull outputs. On slaves the \(BUSY_X\) input internally inhibits writes.
2. '\(L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. '\(H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If \(t_{APS}\) is not met, either \(BUSY_L\) or \(BUSY_R\) = LOW will result. \(BUSY_L\) and \(BUSY_R\) outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when \(BUSY_L\) outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when \(BUSY_R\) outputs are driving LOW regardless of actual logic level on the pin.
**Functional Description**

The IDT71321/IDT71421 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71321/IDT71421 has an automatic power down feature controlled by \( \text{CE} \). The \( \text{CE} \) controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected (\( \text{CE} = \text{VH} \)). When a port is enabled, access to the entire memory array is permitted.

**Interrupts**

If the user chooses the interrupt function, a memory location (mailbox or message center) is assigned to each port. The left port interrupt flag (INTL) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the \( \text{CE} = \text{R/W} = \text{VIL} \), per Truth Table II. The left port clears the interrupt by accessing address location 7FE when \( \text{CEL} = \text{CEL} = \text{VIL}, \text{R/W} \) is a "don't care". Likewise, the right port interrupt flag (INTR) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag (INTR), the right port must access the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mailboxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

**Busy Logic**

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “Busy”. The BUSY pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY Logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT71321 (Master) are open drain type outputs and require open drain resistors to operate. If these SRAMs are being expanded in depth, then the BUSY indication for the resulting array does not require the use of an external AND gate.

**Width Expansion with Busy Logic Master/Slave Arrays**

When expanding an SRAM array in width while using BUSY logic, one master part is used to decide which side of the SRAM array will receive a BUSY indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the BUSY signal as a write inhibit signal. Thus on the IDT71321/IDT71421 SRAMs the BUSY pin is an output if the part is Master (IDT71321), and the BUSY pin is an input if the part is a Slave (IDT71421) as shown in Figure 3.

![Figure 3. Busy and chip enable routing for both width and depth expansion with IDT71321 (Master) and (Slave) IDT71421 SRAMs.](image)

If two or more master parts were used when expanding in width, a split decision could result with one master indicating BUSY on one side of the array and another master indicating BUSY on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The BUSY arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a BUSY flag to be output from the master before the actual write pulse can be initiated with either the R/W signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.
Ordering Information

- **Device Type**: XXXX
- **Power**: A
- **Speed**: 999
- **Package**: A

**Process/Temperature Range**
- Blank: Tube or Tray
- 8: Tape and Reel
- **Temperature Range**
  - Blank: Commercial (0°C to +70°C)
  - 1(1): Industrial (-40°C to +85°C)

**Lead Finish**
- **G**: Green
- **J**: 52-pin PLCC (PLG52)
- **PF**: 64-pin TQFP (PNG64)
- **PP**: 52-pin TQFP (PPG52)
- **TF**: 64-pin TQFP (PPG64)

**Orderable Part Information**

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**Notes:**
1. Contact your sales office for industrial temperature range availability in other speeds, packages and powers.
2. LEAD FINISH (SnPb) parts are Obsolete. Product Discontinuation Notice - PDN# SP-17-02
3. Note that information regarding recently obsoleted parts are included in this datasheet for customer convenience.

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Datasheet Document History

03/24/99: Initiated datasheet document history
Converted to new format
Cosmetic typographical corrections
Pages 2 & 3 Added additional notes to pin configurations
06/07/99: Changed drawing format
11/10/99: Replaced IDT logo
08/23/01: Page 3 Increased storage temperature parameters
Clariﬁed TA parameter
Page 4 DC Electrical parameters–changed wording from "open" to "disabled"
Page 16 Fixed part numbers in "Width Expansion" paragraph
Changed ±500mV to 0mV in notes
Page 4 Industrial temperature range offering added to DC Electrical Characteristics for 25ns and removed for 35ns
Page 7 & 9 Industrial temperature range added to AC Electrical Characteristics for 25ns
Page 17 Industrial offering removed for 35ns ordering information
01/17/06: Page 1 Added green availability to features
Page 17 Added green indicator to ordering information
Page 1 & 17 Replaced old IDT™ logo with new IDT™ logo
08/25/06: Page 14 Changed INT“A” to INT“B” in the CLEAR INT drawing in the Timing Waveform of Interrupt Mode
10/29/08: Page 17 Removed "IDT" from orderable part number
09/10/12: Page 1 & 2 52-pin STQFP added to the features and description
Page 3 PP52-1 pin conﬁguration added
Page 9 Typo corrected
Page 17 Added T&R indicator and PP52-1 package information to the ordering information
06/10/16: Page 2 Changed diagram for the J52 pin conﬁguration by rotating package pin labels and pin numbers 90 degrees clockwise to reﬂect pin1 orientation and added pin 1 dot at pin 1
Removed J52 chamfers and aligned the top and bottom pin labels in the standard direction
Changed diagram for the PN64/PP64 pin conﬁguration by rotating package pin labels and pin numbers 90 degrees counter clockwise to reﬂect pin 1 orientation and added pin 1 dot at pin 1
Page 3 PP52 pin conﬁguration. Added the IDT logo, changed the text to be in alignment with new diagram marking specs
Removed footnote 5 and its references
Pages 2 & 17 In pin conﬁguration footnotes and in the Ordering Information: The package codes J52-1, PN64-1, PP64-1 and PP52-1 changed to J52, PN64, PP64 & PP52 respectively to match standard package codes
02/20/18: Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018
09/24/19: Pages 1 & 17 Deleted obsolete Commercial 25ns speed grade
Pages 2 & 3 Updated package codes
Page 3 Rotated PPG52 STQFP pin conﬁguration to accurately reﬂect pin 1 orientation
Page 5 Typo corrected in the Data Retention Characteristics table 06
Page 17 Added Orderable Part Information
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(Rev.1.0 Mar 2020)

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