Features

- 512K x 36, 1M x 18 memory configurations
- Supports high performance system speed - 200 MHz (3.2 ns Clock-to-Data Access)
- ZBT™ Feature - No dead cycles between write and read cycles
- Internally synchronized output buffer enable eliminates the need to control OE
- Single R/W (READ/WRITE) control pin
- Positive clock-edge triggered address, data, and control signal registers for fully pipelined applications

- 4-word burst capability (interleaved or linear)
- Individual byte write (BW1 - BW4) control (May tie active)
- Three chip enables for simple depth expansion
- 2.5V power supply (±5%)
- 2.5V I/O Supply (VDDQ)
- Power down controlled by ZZ input
- Boundary Scan JTAG Interface (IEEE 1149.1 Compliant)
- Packaged in a JEDEC standard 100-pin plastic thin quad flatpack (TQFP), 119 ball grid array (BGA)
- Green parts available, see Ordering Information

Functional Block Diagram - 512K x 36
Description

The IDT71T75602/802 are 2.5V high-speed 18,874,368-bit (18 Megabit) synchronous SRAMs. They are designed to eliminate dead bus cycles when turning the bus around between reads and writes, or writes and reads. Thus, they have been given the name ZBT™, or Zero Bus Turnaround.

Address and control signals are applied to the SRAM during one clock cycle, and two cycles later the associated data cycle occurs, be it read or write.

The IDT71T75602/802 contain data I/O, address and control signal registers. Output enable is the only asynchronous signal and can be used to disable the outputs at any given time.

A Clock Enable CEN pin allows operation of the IDT71T75602/802 to be suspended as long as necessary. All synchronous inputs are ignored when (CEN) is high and the internal device registers will hold their previous values.

Functional Block Diagram - 1M x 18

There are three chip enable pins (CE1, CE2, CE2) that allow the user to deselect the device when desired. If any one of these three is not asserted when ADV/ŁD is low, no new memory operation can be initiated.

However, any pending data transfers (reads or writes) will be completed. The data bus will tri-state two cycles after the chip is deselected or a write is initiated.

The IDT71T75602/802 have an on-chip burst counter. In the burst mode, the IDT71T75602/802 can provide four cycles of data for a single address presented to the SRAM. The order of the burst sequence is defined by the LBO input pin. The LBO pin selects between linear and interleaved burst sequence. The ADV/ŁD signal is used to load a new external address (ADV/ŁD = LOW) or increment the internal burst counter (ADV/ŁD = HIGH).

The IDT71T75602/802 SRAMs utilize a high-performance 2.5V CMOS process, and are packaged in a JEDEC Standard 14mm x 20mm 100pin thin plastic quad flatpack (TQFP) as well as a 119 ball grid array (BGA).
## Pin Description Summary

<table>
<thead>
<tr>
<th>Pin Description</th>
<th>Type</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A19 Address Inputs</td>
<td>Input</td>
<td>Synchronous</td>
</tr>
<tr>
<td>CE1, CE2, CE2 Chip Enables</td>
<td>Input</td>
<td>Synchronous</td>
</tr>
<tr>
<td>OE Output Enable</td>
<td>Input</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>R/W Read/Write Signal</td>
<td>Input</td>
<td>Synchronous</td>
</tr>
<tr>
<td>CEN Clock Enable</td>
<td>Input</td>
<td>Synchronous</td>
</tr>
<tr>
<td>BW1, BW2, BW3, BW4 Individual Byte Write Selects</td>
<td>Input</td>
<td>Synchronous</td>
</tr>
<tr>
<td>CLK Clock</td>
<td>Input</td>
<td>N/A</td>
</tr>
<tr>
<td>ADV/BD Advance burst address / Load new address</td>
<td>Input</td>
<td>Synchronous</td>
</tr>
<tr>
<td>LB0 Linear / Interleaved Burst Order</td>
<td>Input</td>
<td>Static</td>
</tr>
<tr>
<td>TMS Test Mode Select</td>
<td>Input</td>
<td>N/A</td>
</tr>
<tr>
<td>TDI Test Data Input</td>
<td>Input</td>
<td>N/A</td>
</tr>
<tr>
<td>TCK Test Clock</td>
<td>Input</td>
<td>N/A</td>
</tr>
<tr>
<td>TDO Test Data Input</td>
<td>Output</td>
<td>N/A</td>
</tr>
<tr>
<td>TRST JTAG Reset (Optional)</td>
<td>Input</td>
<td>Asynchronous</td>
</tr>
<tr>
<td>ZZ Sleep Mode</td>
<td>Input</td>
<td>Synchronous</td>
</tr>
<tr>
<td>VO0-VO3, VOP1-VOOp4 Data Input / Output</td>
<td>I/O</td>
<td>Synchronous</td>
</tr>
<tr>
<td>VDD, VDDQ Core Power, I/O Power</td>
<td>Supply</td>
<td>Static</td>
</tr>
<tr>
<td>VSS Ground</td>
<td>Supply</td>
<td>Static</td>
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</table>
### Pin Definitions(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin Function</th>
<th>I/O</th>
<th>Active</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A19</td>
<td>Address Inputs</td>
<td>I</td>
<td>N/A</td>
<td>Synchronous Address inputs. The address register is triggered by a combination of the rising edge of CLK, ADV/LD low, CEN low, and true chip enables.</td>
</tr>
<tr>
<td>ADV/LD</td>
<td>Advance / Load</td>
<td>I</td>
<td>N/A</td>
<td>ADV/LD is a synchronous input that is used to load the internal registers with new address and control when it is sampled low at the rising edge of clock with the chip selected. When ADV/LD is low with the chip deselected, any burst in progress is terminated. When ADV/LD is sampled high then the internal burst counter is advanced for any burst that was in progress. The external addresses are ignored when ADV/LD is sampled high.</td>
</tr>
<tr>
<td>R/W</td>
<td>Read / Write</td>
<td>I</td>
<td>N/A</td>
<td>R/W signal is a synchronous input that identifies whether the current load cycle initiated is a Read or Write access to the memory array. The data bus activity for the current cycle takes place two clock cycles later.</td>
</tr>
<tr>
<td>CEN</td>
<td>Clock Enable</td>
<td>I</td>
<td>LOW</td>
<td>Synchronous Clock Enable input. When CEN is sampled high, all other synchronous inputs, including clock are ignored and outputs remain unchanged. The effect of CEN sampled high on the device outputs is as if the low to high clock transition did not occur. For normal operation, CEN must be sampled low at rising edge of clock.</td>
</tr>
<tr>
<td>BW-BW4</td>
<td>Individual Byte Write Enables</td>
<td>I</td>
<td>LOW</td>
<td>Synchronous byte write enables. Each 8-bit byte has its own active low byte write enable. On load write cycles (when R/W and ADV/LD are sampled low) the appropriate byte write signal (BW-BW4) must be valid. The byte write signal must also be valid on each cycle of a burst write. Byte Write signals are ignored when R/W is sampled high. The appropriate byte(s) of data are written into the device two cycles later. BW-BW4 can all be tied low if always doing write to the entire 36-bit word.</td>
</tr>
<tr>
<td>CE1, CE2</td>
<td>Chip Enables</td>
<td>I</td>
<td>LOW</td>
<td>Synchronous active low chip enable. CE1 and CE2 are used with CE1 to enable the IDT71T75602/802 (CE1 or CE2 sampled high or CE1 sampled low) and ADV/LD low at the rising edge of clock, initiates a deselect cycle. The ZBT™ has a two cycle deselect, i.e., the data bus will tri-state two clock cycles after deselect is initiated.</td>
</tr>
<tr>
<td>CE2</td>
<td>Chip Enable</td>
<td>I</td>
<td>HIGH</td>
<td>Synchronous active high chip enable. CE2 is used with CE1 and CE2 to enable the chip. CE2 has inverted polarity but otherwise identical to CE1 and CE2.</td>
</tr>
<tr>
<td>CLK</td>
<td>Clock</td>
<td>I</td>
<td>N/A</td>
<td>This is the clock input to the IDT71T75602/802. Except for CE, all timing references for the device are made with respect to the rising edge of CLK.</td>
</tr>
<tr>
<td>I/O1+I/O11</td>
<td>Data Input/Output</td>
<td>I/O</td>
<td>N/A</td>
<td>Synchronous data input/output (I/O) pins. Both the data input path and data output path are registered and triggered by the rising edge of CLK.</td>
</tr>
<tr>
<td>LBO</td>
<td>Linear Burst Order</td>
<td>I</td>
<td>LOW</td>
<td>Burst order selection input. When LBO is high the Interleaved burst sequence is selected. When LBO is low the Linear burst sequence is selected. LBO is a static input and it must not change during device operation.</td>
</tr>
<tr>
<td>OE</td>
<td>Output Enable</td>
<td>I</td>
<td>LOW</td>
<td>Asynchronous output enable. OE must be low to read data from the IDT71T75602/802. When OE is high the I/O pins are in a high-impedance state. OE does not need to be actively controlled for read and write cycles. In normal operation, OE can be tied low.</td>
</tr>
<tr>
<td>TMS</td>
<td>Test Mode Select</td>
<td>I</td>
<td>N/A</td>
<td>Gives input command for TAP controller. Sampled on rising edge of TCK. This pin has an internal pullup.</td>
</tr>
<tr>
<td>TDI</td>
<td>Test Data Input</td>
<td>I</td>
<td>N/A</td>
<td>Serial input of registers placed between TDI and TDO. Sampled on rising edge of TCK. This pin has an internal pullup.</td>
</tr>
<tr>
<td>TCK</td>
<td>Test Clock</td>
<td>I</td>
<td>N/A</td>
<td>Clock input of TAP controller. Each TAP event is clocked. Test inputs are captured on rising edge of TCK, while test outputs are driven from the falling edge of TCK. This pin has an internal pullup.</td>
</tr>
<tr>
<td>TDO</td>
<td>Test Data Output</td>
<td>O</td>
<td>N/A</td>
<td>Serial output of registers placed between TDI and TDO. This output is active depending on the state of the TAP controller.</td>
</tr>
<tr>
<td>TRST</td>
<td>JTAG Reset (Optional)</td>
<td>I</td>
<td>LOW</td>
<td>Optional asynchronous JTAG reset. Can be used to reset the TAP controller, but not required. JTAG reset occurs automatically at power up and also resets using TMS and TCK per IEEE 1149.1. If not used TRST can be left floating. This pin has an internal pullup. Only available in BGA package.</td>
</tr>
<tr>
<td>ZZ</td>
<td>Sleep Mode</td>
<td>I</td>
<td>HIGH</td>
<td>Synchronous sleep mode input. ZZ HIGH will gate the CLK internally and power down the IDT71T75602/802 to its lowest power consumption level. Data retention is guaranteed in Sleep Mode. This pin has an internal pulldown.</td>
</tr>
<tr>
<td>Vcc</td>
<td>Power Supply</td>
<td>N/A</td>
<td>N/A</td>
<td>2.5V core power supply.</td>
</tr>
<tr>
<td>VSS</td>
<td>Power Supply</td>
<td>N/A</td>
<td>N/A</td>
<td>2.5V I/O Supply.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>N/A</td>
<td>N/A</td>
<td>Ground.</td>
</tr>
</tbody>
</table>

NOTE:
1. All synchronous inputs must meet specified setup and hold times with respect to CLK.

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1. **NOTE:**
   - 2.5V I/O, Burst Counter, and Pipelined Outputs
   - Commercial and Industrial Temperature Ranges
   - IDT71T75602, IDT71T75802, 512K x 36, 1M x 18, 2.5V Synchronous ZBT™ SRAMs with
Recommended DC Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Core Supply Voltage</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>VDDQ</td>
<td>I/O Supply Voltage</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>VH</td>
<td>Input High Voltage - Inputs</td>
<td>1.7</td>
<td>—</td>
<td>VH+0.3</td>
<td>V</td>
</tr>
<tr>
<td>VL</td>
<td>Input Low Voltage</td>
<td>-0.3(1)</td>
<td>—</td>
<td>0.7</td>
<td>V</td>
</tr>
</tbody>
</table>

NOTE:
1. VIL (min.) = -0.8V for pulse width less than tCYC/2, once per cycle.

Recommended Operating Temperature and Supply Voltage

<table>
<thead>
<tr>
<th>Grade</th>
<th>Ambient Temperature(2)</th>
<th>VSS</th>
<th>VDD</th>
<th>VDDQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0° C to +70° C</td>
<td>OV</td>
<td>2.5V±5%</td>
<td>2.5V ±5%</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40° C to +85° C</td>
<td>OV</td>
<td>2.5V±5%</td>
<td>2.5V ±5%</td>
</tr>
</tbody>
</table>

NOTE:
1. During production testing, the case temperature equals the ambient temperature.

Pin Configuration — 512K x 36

**Top View**

100 TQFP

NOTES:
1. Pins 14, 16, and 66 do not have to be connected directly to VDD as long as the input voltage is ≥ VIH.
2. Pins 38, 39 and 43 will be pulled internally to VDD if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. Pins 38, 39 and 43 could be tied to VDD or VSS and pin 42 should be left unconnected. Or all JTAG inputs (TMS, TDI and TCK) pins 38, 39 and 43 could be left unconnected “NC” and the JTAG circuit will remain disabled from power up.
NOTES:
1. Pins 14, 16, and 66 do not have to be connected directly to VDD as long as the input voltage is ≥ VIL.
2. Pins 38, 39 and 43 will be pulled internally to VDD if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. Pins 38, 39 and 43 could be tied to VDD or VSS and pin 42 should be left unconnected. Or all JTAG inputs (TMS, TDI and TCK) pins 38, 39 and 43 could be left unconnected "NC" and the JTAG circuit will remain disabled from power up.
### Pin Configuration — 512K X 36, 119 BGA\(^{(1,2)}\)

**Top View**

<table>
<thead>
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<th>1</th>
<th>2</th>
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<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>VDDQ</td>
<td>A1</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
</tr>
<tr>
<td>B</td>
<td>NC</td>
<td>CE1</td>
<td>A19</td>
<td>ADV/LD</td>
<td>A19</td>
<td>CE1</td>
</tr>
<tr>
<td>C</td>
<td>NC</td>
<td>A1</td>
<td>A16</td>
<td>VDD</td>
<td>A12</td>
<td>A11</td>
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<tr>
<td>D</td>
<td>VO16</td>
<td>VO15</td>
<td>VSS</td>
<td>NC</td>
<td>VSS</td>
<td>VO14</td>
</tr>
<tr>
<td>E</td>
<td>VO17</td>
<td>VO14</td>
<td>VSS</td>
<td>CE1</td>
<td>VSS</td>
<td>VO13</td>
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<tr>
<td>F</td>
<td>VDDQ</td>
<td>VO18</td>
<td>VSS</td>
<td>CE</td>
<td>VSS</td>
<td>VO12</td>
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<tr>
<td>G</td>
<td>VO30</td>
<td>VO31</td>
<td>BW5</td>
<td>A17</td>
<td>BW4</td>
<td>VO10</td>
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<tr>
<td>H</td>
<td>VO32</td>
<td>VO33</td>
<td>VSS</td>
<td>RW</td>
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<td>VO9</td>
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<td>J</td>
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</tr>
<tr>
<td>K</td>
<td>VO34</td>
<td>VO35</td>
<td>VSS</td>
<td>CLK</td>
<td>VSS</td>
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<td>L</td>
<td>VO36</td>
<td>VO37</td>
<td>BW4</td>
<td>NC</td>
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<td>VO5</td>
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<td>VDDQ</td>
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<td>VO41</td>
<td>VO42</td>
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<td>VDD</td>
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<tr>
<td>T</td>
<td>NC</td>
<td>NC</td>
<td>A10</td>
<td>A11</td>
<td>A12</td>
<td>NC</td>
</tr>
<tr>
<td>U</td>
<td>VDDQ</td>
<td>NC/TMS(1)</td>
<td>NC/TDO(1)</td>
<td>NC/TCK(1)</td>
<td>NC/TDO(1)</td>
<td>NC/TMS(1)</td>
</tr>
</tbody>
</table>

### Pin Configuration — 1M X 18, 119 BGA\(^{(1,2)}\)

**Top View**

<table>
<thead>
<tr>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>VDDQ</td>
<td>A1</td>
<td>A16</td>
<td>A15</td>
<td>A14</td>
<td>A13</td>
</tr>
<tr>
<td>B</td>
<td>NC</td>
<td>CE1</td>
<td>A19</td>
<td>ADV/LD</td>
<td>A19</td>
<td>CE1</td>
</tr>
<tr>
<td>C</td>
<td>NC</td>
<td>A1</td>
<td>A16</td>
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<td>A12</td>
<td>A11</td>
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<tr>
<td>D</td>
<td>VO16</td>
<td>VO15</td>
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<td>VSS</td>
<td>VO14</td>
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<td>VSS</td>
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<td>A17</td>
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<td>A12</td>
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<tr>
<td>U</td>
<td>VDDQ</td>
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<td>NC/TDO(1)</td>
<td>NC/TCK(1)</td>
<td>NC/TDO(1)</td>
<td>NC/TMS(1)</td>
</tr>
</tbody>
</table>

**NOTES:**

1. J3, R5, and J5 do not have to be directly connected to Vcc as long as the input voltage is \( \geq V_{IH} \).
2. U2, U3, U4 and U6 will be pulled internally to Vcc if not actively driven. To disable the TAP controller without interfering with normal operation, several settings are possible. U2, U3, U4 and U6 could be tied to VDD or VSS and U5 should be left unconnected. Or all JTAG inputs (TMS, TDI, and TCK and TRST) U2, U3, U4 and U6 could be left unconnected "NC" and the JTAG circuit will remain disabled from power on.
3. TRST is offered as an optional JTAG reset if required in the application. If not needed, can be left floating and will internally be pulled to Vcc.
IDT71T75602, IDT71T75802, 512K x 36, 1M x 18, 2.5V Synchronous ZBT™ SRAMs with 2.5V I/O, Burst Counter, and Pipelined Outputs
Commercial and Industrial Temperature Ranges

**Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTERM(1)</td>
<td>Terminal Voltage with Respect to GND</td>
<td>-0.5 to +3.6</td>
<td>-0.5 to +3.6</td>
<td>V</td>
</tr>
<tr>
<td>VTERM(2)</td>
<td>Terminal Voltage with Respect to GND</td>
<td>-0.5 to VDD</td>
<td>-0.5 to VDD</td>
<td>V</td>
</tr>
<tr>
<td>VTERM(3)</td>
<td>Terminal Voltage with Respect to GND</td>
<td>-0.5 to VDDQ +0.5</td>
<td>-0.5 to VDDQ +0.5</td>
<td>V</td>
</tr>
<tr>
<td>VTERM(4)</td>
<td>Terminal Voltage with Respect to GND</td>
<td>-0.5 to VDDQ +0.5</td>
<td>-0.5 to VDDQ +0.5</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Ambient Temperature</td>
<td>0 to +70</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>TBIAS</td>
<td>Temperature Under Bias</td>
<td>-55 to +125</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>TTSTG</td>
<td>Storage Temperature</td>
<td>-55 to +125</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>PT</td>
<td>Power Dissipation</td>
<td>2.0</td>
<td>2.0</td>
<td>W</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>50</td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

**100-Pin TQFP Capacitance**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN</td>
<td>Input Capacitance</td>
<td>VOUT = 3dV</td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>I/O Capacitance</td>
<td>VOUT = 3dV</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

**119 BGA Capacitance**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN</td>
<td>Input Capacitance</td>
<td>VIN = 3dV</td>
<td>7</td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>I/O Capacitance</td>
<td>VOUT = 3dV</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vco terminals only.
3. VDDQ terminals only.
4. Input terminals only.
5. I/O terminals only.
6. This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any input or I/O pin cannot exceed VDDQ during power supply ramp up.
7. During production testing, the case temperature equals TA.
Synchronous Truth Table(1)

<table>
<thead>
<tr>
<th>CEN</th>
<th>R/W</th>
<th>Chip(5) Enable</th>
<th>ADV/ŁD</th>
<th>BWx</th>
<th>ADDRESS USED</th>
<th>PREVIOUS CYCLE</th>
<th>CURRENT CYCLE</th>
<th>I/O (2 cycles later)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>Select</td>
<td>L</td>
<td>Valid</td>
<td>External</td>
<td>X</td>
<td>LOAD WRITE</td>
<td>D(7)</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>Select</td>
<td>L</td>
<td>X</td>
<td>External</td>
<td>X</td>
<td>LOAD READ</td>
<td>Q(7)</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>Valid</td>
<td>Internal</td>
<td>LOAD WRITE / BURST WRITE</td>
<td>BURST WRITE (Advance burst counter)(2)</td>
<td>D(7)</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>Internal</td>
<td>LOAD READ / BURST READ</td>
<td>BURST READ (Advance burst counter)(2)</td>
<td>Q(7)</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>Deselect</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DESELECT or STOP(5)</td>
<td>H\text{I\text{Z}}</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>DESELECT / NOOP</td>
<td>NOOP</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>SUSPEND(5)</td>
<td>Previous Value</td>
</tr>
</tbody>
</table>

NOTES:
1. L = VIL, H = VIH, X = Don't Care.
2. When ADV/ŁD signal is sampled high, the internal burst counter is incremented. The R/W signal is ignored when the counter is advanced. Therefore the nature of the burst cycle (Read or Write) is determined by the status of the R/W signal when the first address is loaded at the beginning of the burst cycle.
3. Deselect cycle is initiated when either (CE1, or CE2) is sampled high or CE2 is sampled low and ADV/ŁD is sampled low at rising edge of clock. The data bus will tri-state two cycles after deselect is initiated.
4. When CEN is sampled high at the rising edge of clock, that clock edge is blocked from propagating through the part. The state of all the internal registers and the I/Os remains unchanged.
5. To select the chip requires CE1 = L, CE2 = L, CE2 = H on these chip enables. Chip is deselected if any one of the chip enables is false.
6. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.
7. Q - Data read from the device, D - data written to the device.

Partial Truth Table for Writes(1)

<table>
<thead>
<tr>
<th>OPERATION</th>
<th>R/W</th>
<th>BW1</th>
<th>BW2</th>
<th>BW3(8)</th>
<th>BW4(9)</th>
</tr>
</thead>
<tbody>
<tr>
<td>READ</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>WRITE ALL BYTES</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>WRITE BYTE 1 (I/O[0:7], I/O[1])(2)</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>WRITE BYTE 2 (I/O[8:15], I/O[2])(2)</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>WRITE BYTE 3 (I/O[16:23], I/O[3])(2,3)</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>WRITE BYTE 4 (I/O[24:31], I/O[4])(2,3)</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>NO WRITE</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

NOTES:
1. L = VIL, H = VIH, X = Don't Care.
2. Multiple bytes may be selected during the same cycle.
3. N/A for X18 configuration.
**IDT71T75602, IDT71T75802, 512K x 36, 1M x 18, 2.5V Synchronous ZBT™ SRAMs with 2.5V I/O, Burst Counter, and Pipelined Outputs**

**Commercial and Industrial Temperature Ranges**

---

### Interleaved Burst Sequence Table (LBO=VDD)

<table>
<thead>
<tr>
<th></th>
<th>Sequence 1</th>
<th>Sequence 2</th>
<th>Sequence 3</th>
<th>Sequence 4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A1</td>
<td>A0</td>
<td>A1</td>
<td>A0</td>
</tr>
<tr>
<td>First Address</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Second Address</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Third Address</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Fourth Address</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

### Linear Burst Sequence Table (LBO=Vss)

<table>
<thead>
<tr>
<th></th>
<th>Sequence 1</th>
<th>Sequence 2</th>
<th>Sequence 3</th>
<th>Sequence 4</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>A1</td>
<td>A0</td>
<td>A1</td>
<td>A0</td>
</tr>
<tr>
<td>First Address</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Second Address</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Third Address</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Fourth Address</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Upon completion of the Burst sequence the counter wraps around to its initial state and continues counting.

### Functional Timing Diagram(1)

**CYCLE**

<table>
<thead>
<tr>
<th>n+29</th>
<th>n+30</th>
<th>n+31</th>
<th>n+32</th>
<th>n+33</th>
<th>n+34</th>
<th>n+35</th>
<th>n+36</th>
<th>n+37</th>
</tr>
</thead>
</table>

**CLOCK**

<table>
<thead>
<tr>
<th></th>
<th>n+29</th>
<th>n+30</th>
<th>n+31</th>
<th>n+32</th>
<th>n+33</th>
<th>n+34</th>
<th>n+35</th>
<th>n+36</th>
<th>n+37</th>
</tr>
</thead>
<tbody>
<tr>
<td>A29</td>
<td>A30</td>
<td>A31</td>
<td>A32</td>
<td>A33</td>
<td>A34</td>
<td>A35</td>
<td>A36</td>
<td>A37</td>
<td></td>
</tr>
<tr>
<td>C29</td>
<td>C30</td>
<td>C31</td>
<td>C32</td>
<td>C33</td>
<td>C34</td>
<td>C35</td>
<td>C36</td>
<td>C37</td>
<td></td>
</tr>
<tr>
<td>D/Q27</td>
<td>D/Q28</td>
<td>D/Q29</td>
<td>D/Q30</td>
<td>D/Q31</td>
<td>D/Q32</td>
<td>D/Q33</td>
<td>D/Q34</td>
<td>D/Q35</td>
<td></td>
</tr>
</tbody>
</table>

**ADDRESS**(2)

(A0 - A18)

**CONTROL**(2)

(R/W, ADV/LD, BWx)

**DATA**(2)

(I/O[0:31], I/O P[1:4])

**NOTES:**
1. This assumes CEN, CE1, CE2, CE3 are all true.
2. All Address, Control and Data_In are only required to meet set-up and hold time with respect to the rising edge of clock. Data_Out is valid after a clock-to-data delay from the rising edge of clock.
### Device Operation - Showing Mixed Load, Burst, Deselect and NOOP Cycles (2)

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Address</th>
<th>R/W</th>
<th>ADV/LD</th>
<th>CE&lt;1&gt;</th>
<th>CE&lt;2&gt;</th>
<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>A0</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Load read</td>
</tr>
<tr>
<td>n+1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Burst read</td>
</tr>
<tr>
<td>n+2</td>
<td>A1</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Q0</td>
<td></td>
<td>Load read</td>
</tr>
<tr>
<td>n+3</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Q0+1</td>
<td>Deselect or STOP</td>
</tr>
<tr>
<td>n+4</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Q1</td>
<td>NOOP</td>
</tr>
<tr>
<td>n+5</td>
<td>A2</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Load read</td>
</tr>
<tr>
<td>n+6</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Burst read</td>
</tr>
<tr>
<td>n+7</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Q2</td>
<td>Deselect or STOP</td>
</tr>
<tr>
<td>n+8</td>
<td>A3</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Q2+1</td>
<td>Load write</td>
</tr>
<tr>
<td>n+9</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>Z</td>
<td>Burst write</td>
</tr>
<tr>
<td>n+10</td>
<td>A4</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>D0</td>
<td>Load write</td>
</tr>
<tr>
<td>n+11</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>D0+1</td>
<td>Deselect or STOP</td>
</tr>
<tr>
<td>n+12</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>D0</td>
<td>NOOP</td>
</tr>
<tr>
<td>n+13</td>
<td>A5</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>D5</td>
<td>Load write</td>
</tr>
<tr>
<td>n+14</td>
<td>A6</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Load read</td>
</tr>
<tr>
<td>n+15</td>
<td>A7</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>D5</td>
<td>Load write</td>
</tr>
<tr>
<td>n+16</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Q6</td>
<td>Burst write</td>
</tr>
<tr>
<td>n+17</td>
<td>A8</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>D7</td>
<td>Load read</td>
</tr>
<tr>
<td>n+18</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>D7+1</td>
<td>Burst read</td>
</tr>
<tr>
<td>n+19</td>
<td>A9</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>Q8</td>
<td>Load write</td>
</tr>
</tbody>
</table>

**NOTES:**
1. CE = L is defined as CE<1> = L, CE<2> = L and CE2 = H. CE = H is defined as CE<1> = H, CE<2> = H or CE2 = L.
2. H = High; L = Low; X = Don’t Care; Z = High Impedance.

### Read Operation (1)

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Address</th>
<th>R/W</th>
<th>ADV/LD</th>
<th>CE&lt;1&gt;</th>
<th>CE&lt;2&gt;</th>
<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>A0</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Address and Control meet setup</td>
</tr>
<tr>
<td>n+1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Clock Setup Valid</td>
</tr>
<tr>
<td>n+2</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>Q0</td>
<td>Contents of Address A0 Read Out</td>
</tr>
</tbody>
</table>

**NOTES:**
1. H = High; L = Low; X = Don’t Care; Z = High Impedance.
2. CE = L is defined as CE<1> = L, CE<2> = L and CE2 = H. CE = H is defined as CE<1> = H, CE<2> = H or CE2 = L.
Burst Read Operation(1)

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Address</th>
<th>R/W</th>
<th>ADV/LD</th>
<th>CE(1)</th>
<th>CEN</th>
<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
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<tbody>
<tr>
<td>n</td>
<td>A0</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Address and Control meet setup</td>
</tr>
<tr>
<td>n+1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
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<tr>
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<td>X</td>
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<td>L</td>
<td>Q0</td>
<td>Address A0 Read Out, Inc. Count</td>
</tr>
<tr>
<td>n+3</td>
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<td>X</td>
<td>X</td>
<td>H</td>
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<td>L</td>
<td>Q0+1</td>
<td>Address A0+1 Read Out, Inc. Count</td>
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<tr>
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<td>Q0+2</td>
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<td>Q0+3</td>
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</tr>
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<td>n+6</td>
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<td>Q0</td>
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</tr>
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<td>X</td>
<td>L</td>
<td>Q1</td>
<td>Address A1 Read Out, Inc. Count</td>
</tr>
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<td>X</td>
<td>L</td>
<td>Q1+1</td>
<td>Address A1+1 Read Out, Load A2</td>
</tr>
</tbody>
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NOTES:
1. H = High; L = Low; X = Don’t Care; Z = High Impedance.
2. CE = L is defined as CE1 = L, CE2 = L and CE2 = H. CE = H is defined as CE1 = H, CE2 = H or CE2 = L.

Write Operation(1)

<table>
<thead>
<tr>
<th>Cycle</th>
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<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
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<tr>
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<td>X</td>
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</tr>
<tr>
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</tr>
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<td>X</td>
<td>Write to Address A0</td>
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</tbody>
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NOTES:
1. H = High; L = Low; X = Don’t Care; Z = High Impedance.
2. CE = L is defined as CE1 = L, CE2 = L and CE2 = H. CE = H is defined as CE1 = H, CE2 = H or CE2 = L.

Burst Write Operation(1)

<table>
<thead>
<tr>
<th>Cycle</th>
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<th>CEN</th>
<th>BWx</th>
<th>OE</th>
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<th>Comments</th>
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<td>Address and Control meet setup</td>
</tr>
<tr>
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<td>X</td>
<td>X</td>
<td>H</td>
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<td>X</td>
<td>L</td>
<td>X</td>
<td>Clock Setup Valid, Inc. Count</td>
</tr>
<tr>
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<td>X</td>
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<td>L</td>
<td>X</td>
<td>X</td>
<td>Address A0+3 Write, Load A1</td>
</tr>
<tr>
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<td>Address A0 Write, Inc. Count</td>
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<td>Address A1 Write, Inc. Count</td>
</tr>
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<td>X</td>
<td>D1</td>
<td>D1+1</td>
<td>Address A1+1 Write, Load A2</td>
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</table>

NOTES:
1. H = High; L = Low; X = Don’t Care; Z = High Impedance.
2. CE = L is defined as CE1 = L, CE2 = L and CE2 = H. CE = H is defined as CE1 = H, CE2 = H or CE2 = L.
Read Operation with Clock Enable Used\(^{(1)}\)

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Address</th>
<th>R/W</th>
<th>ADV/LD</th>
<th>CE(^{(1)})</th>
<th>CEN</th>
<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
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</thead>
<tbody>
<tr>
<td>n</td>
<td>A(_0)</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Address and Control meet setup.</td>
</tr>
<tr>
<td>n+1</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
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<td>Clock n+1 Ignored.</td>
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<tr>
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<td>A(_1)</td>
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<td>L</td>
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<td></td>
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<td>Clock Valid.</td>
</tr>
<tr>
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<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>Q(_0)</td>
<td>Q(_0) is on the bus.</td>
</tr>
<tr>
<td>n+4</td>
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<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>L</td>
<td>Q(_0)</td>
<td>Q(_0) is on the bus.</td>
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<tr>
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<td>L</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Q(_0)</td>
<td>Address A(_0) Read out (bus trans.)</td>
</tr>
<tr>
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<td>A(_3)</td>
<td>H</td>
<td>L</td>
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<td>L</td>
<td>X</td>
<td>L</td>
<td>Q(_1)</td>
<td>Address A(_1) Read out (bus trans.)</td>
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<tr>
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<td>X</td>
<td>L</td>
<td>Q(_2)</td>
<td>Address A(_2) Read out (bus trans.)</td>
</tr>
</tbody>
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NOTES:
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2. CE = L is defined as CE\(_1\) = L, CE\(_2\) = L and CE\(_2\) = H. CE = H is defined as CE\(_1\) = H, CE\(_2\) = H or CE\(_2\) = L.

Write Operation with Clock Enable Used\(^{(1)}\)

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Address</th>
<th>R/W</th>
<th>ADV/LD</th>
<th>CE(^{(1)})</th>
<th>CEN</th>
<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
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</thead>
<tbody>
<tr>
<td>n</td>
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<td>L</td>
<td>L</td>
<td>L</td>
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<td>X</td>
<td>X</td>
<td>Address and Control meet setup.</td>
</tr>
<tr>
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<tr>
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<td>X</td>
<td>X</td>
<td>X</td>
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<td>H</td>
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</tr>
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<td>X</td>
<td>X</td>
<td>X</td>
<td>Clock Ignored.</td>
</tr>
<tr>
<td>n+3</td>
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<td>X</td>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
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</tr>
<tr>
<td>n+4</td>
<td>X</td>
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<td>X</td>
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<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Clock Ignored.</td>
</tr>
<tr>
<td>n+5</td>
<td>A(_2)</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>X</td>
<td>D(_0)</td>
<td>Write Data D(_0)</td>
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<tr>
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<td>L</td>
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<td>D(_1)</td>
<td>Write Data D(_1)</td>
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<tr>
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<td>A(_4)</td>
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<td>L</td>
<td>X</td>
<td>D(_2)</td>
<td>Write Data D(_2)</td>
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NOTES:
1. H = High; L = Low; X = Don’t Care; Z = High Impedance.
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### Read Operation with Chip Enable Used

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Address</th>
<th>R/W</th>
<th>ADV/LD</th>
<th>CE1</th>
<th>CEN</th>
<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>?</td>
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</tr>
<tr>
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<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>?</td>
<td>Deselected.</td>
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<td>X</td>
<td>X</td>
<td>Z</td>
<td>Address and Control meet setup.</td>
</tr>
<tr>
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<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Deselected or STOP.</td>
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<tr>
<td>n+4</td>
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<td>H</td>
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<td>L</td>
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<td>X</td>
<td>L</td>
<td>Q0</td>
<td>Address A0 Read out. Load A1.</td>
</tr>
<tr>
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<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Deselected or STOP.</td>
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<tr>
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<td>X</td>
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<td>H</td>
<td>L</td>
<td>X</td>
<td>L</td>
<td>Q1</td>
<td>Address A1 Read out. Deselected.</td>
</tr>
<tr>
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<td>X</td>
<td>Z</td>
<td>Address and control meet setup.</td>
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<td>Q2</td>
<td>Address A2 Read out. Deselected.</td>
</tr>
</tbody>
</table>

**NOTES:**
1. H = High; L = Low; X = Don’t Care; ? = Don’t Know; Z = High Impedance.
2. CE = L is defined as CE1 = L, CE2 = L and CE2 = H. CE = H is defined as CE1 = H, CE2 = H or CE2 = L.
3. Device Outputs are ensured to be in High-Z after the first rising edge of clock upon power-up.

### Write Operation with Chip Enable Used

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Address</th>
<th>R/W</th>
<th>ADV/LD</th>
<th>CE1</th>
<th>CEN</th>
<th>BWx</th>
<th>OE</th>
<th>I/O</th>
<th>Comments</th>
</tr>
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<tbody>
<tr>
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<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>?</td>
<td>Deselected.</td>
</tr>
<tr>
<td>n+1</td>
<td>X</td>
<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>?</td>
<td>Deselected.</td>
</tr>
<tr>
<td>n+2</td>
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<td>L</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Address and Control meet setup.</td>
</tr>
<tr>
<td>n+3</td>
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<td>X</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>X</td>
<td>X</td>
<td>Z</td>
<td>Deselected or STOP.</td>
</tr>
<tr>
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<td>X</td>
<td>D0</td>
<td>Address D0 Write in. Load A1.</td>
<td></td>
</tr>
<tr>
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<td>X</td>
<td>X</td>
<td>Z</td>
<td>Deselected or STOP.</td>
</tr>
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<td>L</td>
<td>X</td>
<td>D1</td>
<td>Address D1 Write in. Deselected.</td>
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<td>X</td>
<td>Z</td>
<td>Address and control meet setup.</td>
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<td>Z</td>
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<td>X</td>
<td>D2</td>
<td>Address D2 Write in. Deselected.</td>
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</table>

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DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (\(V_{DD} = 2.5V \pm 5\%\))

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>200MHz(4)</th>
<th>166MHz</th>
<th>150MHz</th>
<th>133MHz</th>
<th>100MHz</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{OP}</td>
<td>Operating Power Supply Current</td>
<td>Device Selected, Outputs Open, (AVD/VDD = X, V_{CC} = Max., V_H &gt; V_{IH} \text{ or } \leq V_L, f = f_{MAX})(2)</td>
<td>275</td>
<td>295</td>
<td>245</td>
<td>265</td>
<td>215</td>
<td>235</td>
</tr>
<tr>
<td>I_{SS1}</td>
<td>CMOS Standby Power Supply Current</td>
<td>Device Deselected, Outputs Open, (V_{CC} = Max., V_H &gt; V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX})(2)</td>
<td>40</td>
<td>60</td>
<td>40</td>
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<td>40</td>
<td>60</td>
</tr>
<tr>
<td>I_{SS2}</td>
<td>Clock Running Power Supply Current</td>
<td>Device Deselected, Outputs Open, (V_{CC} = Max., V_H &gt; V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX})(2)</td>
<td>80</td>
<td>100</td>
<td>70</td>
<td>90</td>
<td>60</td>
<td>80</td>
</tr>
<tr>
<td>I_{SS3}</td>
<td>Idle Power Supply Current</td>
<td>Device Selected, Outputs Open, (CEN &gt; V_{IH}, V_{CC} = Max., V_H &gt; V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX})(2)</td>
<td>60</td>
<td>80</td>
<td>60</td>
<td>80</td>
<td>60</td>
<td>80</td>
</tr>
<tr>
<td>I_{ZZ}</td>
<td>Full Sleep Mode Supply Current</td>
<td>Device Selected, Outputs Open, (CEN &lt; V_{IH}, V_{CC} = Max., V_H &gt; V_{IH} \text{ or } \leq V_{IL}, f = f_{MAX})(2), ZZ &gt; (V_{CC})</td>
<td>40</td>
<td>60</td>
<td>40</td>
<td>60</td>
<td>40</td>
<td>60</td>
</tr>
</tbody>
</table>

NOTES:
1. All values are maximum guaranteed values.
2. If \(f = f_{MAX}\), inputs are cycling at the maximum frequency of read cycles of 1/t_{CYC}; \(f = 0\) means no input lines are changing.
3. For I/Os \(V_{HD} = V_{CC} - 0.2V, V_{LD} = 0.2V\). For other inputs \(V_{HD} = V_{CC} - 0.2V, V_{LD} = 0.2V\).
4. 200MHz is for 717T5802 only.

AC Test Load

**Figure 1. AC Test Load**

**Figure 2. Lumped Capacitive Load, Typical Derating**

AC Test Conditions

- Input Pulse Levels: 0 to 2.5V
- Input Rise/Fall Times: 2ns
- Input Timing Reference Levels: \(V_{DDQ}/2\)
- Output Timing Reference Levels: \(V_{DDQ}/2\)
- AC Test Load: See Figure 1
## AC Electrical Characteristics

**(VDD = 2.5V +/-5%, Commercial and Industrial Temperature Ranges)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>200MHz(6)</th>
<th>166MHz</th>
<th>150MHz</th>
<th>133MHz</th>
<th>100MHz</th>
</tr>
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<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
</tr>
<tr>
<td>τCYC</td>
<td>Clock Cycle Time</td>
<td>5</td>
<td>6</td>
<td>6.7</td>
<td>7.5</td>
<td>10</td>
</tr>
<tr>
<td>τF(1)</td>
<td>Clock Frequency</td>
<td>200</td>
<td>166</td>
<td>150</td>
<td>133</td>
<td>100</td>
</tr>
<tr>
<td>τCH(2)</td>
<td>Clock High Pulse Width</td>
<td>1.8</td>
<td>1.8</td>
<td>2.0</td>
<td>2.2</td>
<td>3.2</td>
</tr>
<tr>
<td>τCL(2)</td>
<td>Clock Low Pulse Width</td>
<td>1.8</td>
<td>1.8</td>
<td>2.0</td>
<td>2.2</td>
<td>3.2</td>
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### Output Parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
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<th>Max.</th>
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<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
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<tbody>
<tr>
<td>τCD</td>
<td>Clock High to Valid Data</td>
<td>3.2</td>
<td>3.5</td>
<td>3.8</td>
<td>4.2</td>
<td>5</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td>τCDC</td>
<td>Clock High to Data Change</td>
<td>1.0</td>
<td>1.0</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>ns</td>
</tr>
<tr>
<td>τCLZ(3,4,5)</td>
<td>Clock High to Output Active</td>
<td>1.0</td>
<td>3.0</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
<td>ns</td>
</tr>
<tr>
<td>τCHZ(3,4,5)</td>
<td>Clock High to Data High-Z</td>
<td>1.0</td>
<td>3.0</td>
<td>1.5</td>
<td>3.0</td>
<td>1.5</td>
<td>3.3</td>
<td>ns</td>
</tr>
<tr>
<td>τOE</td>
<td>Output Enable Access Time</td>
<td>3.2</td>
<td>3.5</td>
<td>3.8</td>
<td>4.2</td>
<td>5</td>
<td>5</td>
<td>ns</td>
</tr>
<tr>
<td>τOLZ(3,4)</td>
<td>Output Enable Low to Data Active</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ns</td>
</tr>
<tr>
<td>τOHZ(3,4)</td>
<td>Output Enable High to Data High-Z</td>
<td>3.2</td>
<td>3.5</td>
<td>3.8</td>
<td>4.2</td>
<td>5</td>
<td>5</td>
<td>ns</td>
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### Set Up Times

<table>
<thead>
<tr>
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<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>τSE</td>
<td>Clock Enable Setup Time</td>
<td>1.4</td>
<td>1.5</td>
<td>1.5</td>
<td>1.7</td>
<td>2.0</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>τSA</td>
<td>Address Setup Time</td>
<td>1.4</td>
<td>1.5</td>
<td>1.5</td>
<td>1.7</td>
<td>2.0</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>τSD</td>
<td>Data In Setup Time</td>
<td>1.4</td>
<td>1.5</td>
<td>1.5</td>
<td>1.7</td>
<td>2.0</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>τSW</td>
<td>Read/Write (R/W) Setup Time</td>
<td>1.4</td>
<td>1.5</td>
<td>1.5</td>
<td>1.7</td>
<td>2.0</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>τSADV</td>
<td>Advance/Load (ADV/LD) Setup Time</td>
<td>1.4</td>
<td>1.5</td>
<td>1.5</td>
<td>1.7</td>
<td>2.0</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>τSC</td>
<td>Chip Enable/Select Setup Time</td>
<td>1.4</td>
<td>1.5</td>
<td>1.5</td>
<td>1.7</td>
<td>2.0</td>
<td>2.0</td>
<td>ns</td>
</tr>
<tr>
<td>τSB</td>
<td>Byte Write Enable (BWx) Setup Time</td>
<td>1.4</td>
<td>1.5</td>
<td>1.5</td>
<td>1.7</td>
<td>2.0</td>
<td>2.0</td>
<td>ns</td>
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</table>

### Hold Times

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>τHE</td>
<td>Clock Enable Hold Time</td>
<td>0.4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>ns</td>
</tr>
<tr>
<td>τHA</td>
<td>Address Hold Time</td>
<td>0.4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>ns</td>
</tr>
<tr>
<td>τHD</td>
<td>Data In Hold Time</td>
<td>0.4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>ns</td>
</tr>
<tr>
<td>τMW</td>
<td>Read/Write (R/W) Hold Time</td>
<td>0.4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>ns</td>
</tr>
<tr>
<td>τMADV</td>
<td>Advance/Load (ADV/LD) Hold Time</td>
<td>0.4</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>ns</td>
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<tr>
<td>τHC</td>
<td>Chip Enable/Select Hold Time</td>
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<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>ns</td>
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<tr>
<td>τHB</td>
<td>Byte Write Enable (BWx) Hold Time</td>
<td>0.4</td>
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<td>0.5</td>
<td>0.5</td>
<td>0.5</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Notes:

1. $\tau_F = 1/\tau_{CYC}$
2. Measured as HIGH above 0.6VDDQ and LOW below 0.4VDDQ.
3. Transition is measured $\pm200$mV from steady-state.
4. These parameters are guaranteed with the AC load (Figure 1) by device characterization. They are not production tested.
5. To avoid bus contention, the output buffers are designed such that $\tau_{CLZ}$ (device turn-off) is faster than $\tau_{CHZ}$ (device turn-on) at a given temperature and voltage. The specs as shown do not imply bus contention because $\tau_{CLZ}$ is a Min. parameter that is worse case at totally different test conditions (0 deg. C, 2.625V) than $\tau_{CHZ}$, which is a Max. parameter (worse case at 70 deg. C, 2.375V)
6. 200MHz is for 71T75802 only.

---

5313 titl 24
NOTES:
1. $Q(A1)$ represents the first output from the external address $A_1$; $Q(A2)$ represents the first output from the external address $A_2$; $Q(A2+1)$ represents the next output data in the burst sequence of the base address $A_2$, etc. where address bits $A_0$ and $A_1$ are advancing for the four word burst in the sequence defined by the state of the $LBO$ input.
2. $CE_2$ timing transitions are identical but inverted to the $CE_1$ and $CE_2$ signals. For example, when $CE_1$ and $CE_2$ are LOW on this waveform, $CE_2$ is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling $ADV/$. 
4. $R/W$ is don't care when the SRAM is bursting ($ADV/LD$ sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the $R/W$ signal when new address and control are loaded into the SRAM.
NOTES:
1. D (A1) represents the first input to the external address A1. D (A2) represents the first input to the external address A2; D (A2+1) represents the next input data in the burst sequence of the base address A2, etc. where address bits A0 and A1 are advancing for the four word burst in the sequence defined by the state of the LBO input.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. Burst ends when new address and control are loaded into the SRAM by sampling ADV/CE LOW.
4. R/W is don't care when the SRAM is bursting (ADV/CE sampled HIGH). The nature of the burst access (Read or Write) is fixed by the state of the R/W signal when new address and control are loaded into the SRAM.
5. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.
Timing Waveform of Combined Read and Write Cycles\(^{(1,2,3)}\)

**NOTES:**
1. Q(A1) represents the first output from the external address A1. D(Aj) represents the input data to the SRAM corresponding to address A2.
2. CE \(1 \) and CE \( 2 \) timing transitions are identical but inverted to each other. For example, when CE \( 1 \) and CE \( 2 \) are LOW on this waveform, CE \( 2 \) is HIGH.
3. Individual Byte Write signals (\( BWx \)) must be valid on all write and burst-write cycles. A write cycle is initiated when the \( R/W \) signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.
NOTES:
1. Q (A1) represents the first output from the external address A1. D (A2) represents the input data to the SRAM corresponding to address A2.
2. CE2 timing transitions are identical but inverted to the CE1 and CE2 signals. For example, when CE1 and CE2 are LOW on this waveform, CE2 is HIGH.
3. CEN when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals (BWx) must be valid on all write and burst-write cycles. A write cycle is initiated when R/W signal is sampled LOW. The byte write information comes in two cycles before the actual data is presented to the SRAM.
Timing Waveform of $\overline{CS}$ Operation$^{(1,2,3,4)}$

NOTES:
1. $Q(A_1)$ represents the first output from the external address $A_1$, $D(A_3)$ represents the input data to the SRAM corresponding to address $A_3$.
2. $CE_1$ and $CE_2$ timing transitions are identical but inverted to the $CE_1$ and $CE_2$ signals. For example, when $CE_1$ and $CE_2$ are LOW on this waveform, $CE_1$ is HIGH.
3. $CEN$ when sampled high on the rising edge of clock will block that L-H transition of the clock from propagating into the SRAM. The part will behave as if the L-H clock transition did not occur. All internal registers in the SRAM will retain their previous state.
4. Individual Byte Write signals ($BW_x$) must be valid on all write and burst-write cycles. A write cycle is initiated when $R/W$ signal is sampled LOW. The byte write information comes in two cycles before the data is presented to the SRAM.
IDT71T75602, IDT71T75802, 512K x 36, 1M x 18, 2.5V Synchronous ZBT™ SRAMs with 2.5V I/O, Burst Counter, and Pipelined Outputs

Commercial and Industrial Temperature Ranges

JTAG Interface Specification

![Diagram of JTAG interface]

Device Inputs\( ^{(1)} \)/TDI/TMS

Device Outputs\( ^{(2)} \)/TDO

TRST\( ^{(3)} \)

NOTES:
1. Device inputs = All device inputs except TDI, TMS and TRST.
2. Device outputs = All device outputs except TDO.
3. During power up, TRST could be driven low or not be used since the JTAG circuit resets automatically. TRST is an optional JTAG reset.

JTAG AC Electrical Characteristics\( ^{(1,2,3,4)} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{JCY} )</td>
<td>JTAG Clock Input Period</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JCH} )</td>
<td>JTAG Clock HIGH</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JCL} )</td>
<td>JTAG Clock Low</td>
<td>40</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JR} )</td>
<td>JTAG Clock Rise Time</td>
<td></td>
<td>5( ^{(1)} )</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JF} )</td>
<td>JTAG Clock Fall Time</td>
<td></td>
<td>5( ^{(1)} )</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JRST} )</td>
<td>JTAG Reset</td>
<td>50</td>
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<td>ns</td>
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<tr>
<td>( t_{JRSR} )</td>
<td>JTAG Reset Recovery</td>
<td>50</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JCD} )</td>
<td>JTAG Data Output Hold</td>
<td>20</td>
<td></td>
<td>ns</td>
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<tr>
<td>( t_{JDC} )</td>
<td>JTAG Data Output</td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JS} )</td>
<td>JTAG Setup</td>
<td>25</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{JH} )</td>
<td>JTAG Hold</td>
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<td>ns</td>
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Scan Register Sizes

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<th>Bit Size</th>
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<td>Instruction (IR)</td>
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<tr>
<td>Bypass (BYR)</td>
<td>1</td>
</tr>
<tr>
<td>JTAG Identification (JIDR)</td>
<td>32</td>
</tr>
<tr>
<td>Boundary Scan (BSR)</td>
<td>Note (1)</td>
</tr>
</tbody>
</table>

NOTE:
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

NOTES:
1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.
JTAG Identification Register Definitions

<table>
<thead>
<tr>
<th>Instruction Field</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision Number (31:28)</td>
<td>0x2</td>
<td>Reserved for version number.</td>
</tr>
<tr>
<td>IDT Device ID (27:12)</td>
<td>0x220, 0x222</td>
<td>Defines IDT part number 71T75602 and 71T75802, respectively.</td>
</tr>
<tr>
<td>IDT JEDEC ID (11:1)</td>
<td>0x33</td>
<td>Allows unique identification of device vendor as IDT.</td>
</tr>
<tr>
<td>ID Register Indicator Bit (Bit 0)</td>
<td>1</td>
<td>Indicates the presence of an ID register.</td>
</tr>
</tbody>
</table>

Available JTAG Instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
<th>OPCODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXTEST</td>
<td>Forces contents of the boundary scan cells onto the device outputs(^1). Places the boundary scan register (BSR) between TDI and TDO.</td>
<td>0000</td>
</tr>
<tr>
<td>SAMPLE/PRICELOAD</td>
<td>Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(^2) and outputs(^1) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.</td>
<td>0001</td>
</tr>
<tr>
<td>DEVICE_ID</td>
<td>Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO.</td>
<td>0010</td>
</tr>
<tr>
<td>HIGHZ</td>
<td>Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.</td>
<td>0011</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRICELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions.</td>
<td>0100</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Same as above.</td>
<td>0101</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Same as above.</td>
<td>0110</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Same as above.</td>
<td>0111</td>
</tr>
<tr>
<td>CLAMP</td>
<td>Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.</td>
<td>1000</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Same as above.</td>
<td>1001</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Same as above.</td>
<td>1010</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Same as above.</td>
<td>1011</td>
</tr>
<tr>
<td>RESERVED</td>
<td>Same as above.</td>
<td>1100</td>
</tr>
<tr>
<td>VALIDATE</td>
<td>Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits ‘01’ are mandated by the IEEE std. 1149.1 specification.</td>
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<td>Same as above.</td>
<td>1110</td>
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<tr>
<td>BYPASS</td>
<td>The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.</td>
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NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and TRST.
Timing Waveform of OE Operation(1)

NOTE:
1. A read operation is assumed to be in progress.

Ordering Information

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<td>119 Ball Grid Array (BGG119)</td>
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Orderable Part Information

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IDT71T5602, IDT71T5802, 512K x 36, 1M x 18, 2.5V Synchronous ZBT™ SRAMs with 2.5V I/O, Burst Counter, and Pipelined Outputs

Commercial and Industrial Temperature Ranges

Datasheet Document History

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<td>Pg.1,2,14,23,24</td>
<td>Added 166MHz speed grade offering</td>
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<td>Pg.23</td>
<td>Corrected error in ZZ Sleep Mode</td>
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<td>Added BQ165 Package Diagram Outline</td>
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<td>Corrected 119BGA Package Diagram Outline</td>
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<td>Pg.26</td>
<td>Corrected topmark on ordering information</td>
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<td>Pg.1,2,24</td>
<td>Removed reference of BQ165 Package</td>
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<td>Removed page of the 165 BGA pin configuration</td>
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<td>Removed page of the 165 BGA package diagram outline</td>
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<td>3</td>
<td>10/16/01</td>
<td>Pg.6</td>
<td>Corrected 3.3V to 2.5V in Note 2</td>
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<tr>
<td></td>
<td>10/29/01</td>
<td>Pg.13</td>
<td>Improved DC Electrical characteristics-parameters improved: Icc, ISB2, ISB3, IZz.</td>
</tr>
<tr>
<td>4</td>
<td>12/21/01</td>
<td>Pg.4,6</td>
<td>Added clarification to JTAG pins, allow for NC. Added 36M address pin locations.</td>
</tr>
<tr>
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<td>Pg.14</td>
<td>Revised 166MHz tcoc(min), tclz(min) and tchz(min) to 1.0ns</td>
</tr>
<tr>
<td>5</td>
<td>06/07/02</td>
<td>Pg.1-3,6,13,20,21</td>
<td>Added complete JTAG functionality.</td>
</tr>
<tr>
<td></td>
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<td>Pg.2,13</td>
<td>Added notes for ZZ pin internal pulldown and ZZ leakage current.</td>
</tr>
<tr>
<td></td>
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<td>Pg.13,14,24</td>
<td>Added 200MHz and 225MHz to DC and AC Electrical Characteristics. Updated supply current for Idd, ISB1, ISB3 and Izz.</td>
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<tr>
<td>6</td>
<td>11/19/02</td>
<td>Pg.1-24</td>
<td>Changed datasheet from Advanced Information to Final Release.</td>
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<td>Pg.13</td>
<td>Updated DC Electrical characteristics temperature and voltage range table.</td>
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<tr>
<td>7</td>
<td>05/23/03</td>
<td>Pg.4,5,13,14,24</td>
<td>Added I-temp to the datasheet.</td>
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<td>Updated 165 BGA Capacitance table.</td>
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<tr>
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<td>Pg.1</td>
<td>Updated logo with new design.</td>
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<td>Pg.4,5</td>
<td>Clarified ambient and case operating temperatures.</td>
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<td>Pg.6</td>
<td>Updated pin I/O number order for the 119 BGA.</td>
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<td>Pg.23</td>
<td>Updated 119BGA Package Diagram Drawing.</td>
</tr>
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<td>9</td>
<td>10/01/08</td>
<td>Pg.1,13,14,24</td>
<td>Deleted 225MHz part, added 200MHz Industrial grade and added green packages. Updated the ordering information by removing the “IDT” notation.</td>
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<tr>
<td>10</td>
<td>04/04/12</td>
<td>Pg.2,22</td>
<td>Updated text on page 2 last paragraph. Added Note to ordering information and updated to include tube or tray and tape &amp; reel.</td>
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<td>10/04/17</td>
<td>Pg.1 &amp; 26</td>
<td>Updated IDT logo from Trademark to Registered</td>
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<td>Pg.1-4</td>
<td>In Features: Added text: “Green parts available, see Ordering Information”</td>
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<tr>
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<td>Pg.5 &amp; 6</td>
<td>Moved the 512Kx36 FBD from page 3 to page 1, moved the 1Mx18 FBD from page 3 to page 2, moved the Pin Description Summary from page 1 to page 3 and moved the Pin Definitions from page 2 to page 4 in accordance with our standard datasheet format</td>
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<td>Pg.6</td>
<td>Updated the TQFP pin configurations for the 512kx36 and 1Mx18 by rotating package pin labels and pin numbers 90 degrees counter clockwise, added IDT logo &amp; in accordance with the packaging code, changed the PK100 designation to PKG100, changed the text to be in alignment with new diagram marking specs</td>
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<td>Removed “? = don't know” from Burst Write Operation footnote 1 as it does not apply to this table</td>
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<td>Pg.15</td>
<td>Updated DC Chars table added footnote 4 &amp; reference 4 for the 512K x 36, 119 BGA 200MHz speed offered only for the 71T75802 device</td>
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<td>Updated AC Chars table added footnote 6 &amp; reference 6 for the 1M x 18, 119 BGA 200MHz speed offered only for the 71T75802 device</td>
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<td>Ordering Information updated to Tray and Green indicator</td>
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<td>Updated package codes TQFP to PKG100 and BGA to BGG119</td>
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