3.3V CMOS Static RAM
1 Meg (128K x 8-Bit)
Center Power &
Ground Pinout

Features
• 128K x 8 advanced high-speed CMOS static RAM
• JEDEC revolutionary pinout (center power/GND) for reduced noise
• Equal access and cycle times
  - Commercial: 10/12/15ns
  - Industrial: 12/15ns
• One Chip Select plus one Output Enable pin
• Inputs and outputs are LVTTL-compatible
• Single 3.3V supply
• Low power consumption via chip deselect
• Available in a 32-pin 300- and 400-mil Plastic SOJ, and 32-pin Type II TSOP packages.

Description
The IDT71V124 is a 1,048,576-bit high-speed static RAM organized as 128K x 8. It is fabricated using high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC center power/GND pinout reduces noise generation and improves system performance.

The IDT71V124 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns available. All bidirectional inputs and outputs of the IDT71V124 are LVTTL-compatible and operation is from a single 3.3V supply. Fully static asynchronous circuitry is used; no clocks or refreshes are required for operation.

Functional Block Diagram
IDT71V124SA, 3.3V CMOS Static RAM
1 Meg (128K x 8-Bit) Center Power & Ground Pinout
Commercial and Industrial Temperature Ranges

Pin Configuration

SOJ and TSOP
Top View

Truth Table(1)

<table>
<thead>
<tr>
<th>CS</th>
<th>OE</th>
<th>WE</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>DATAOUT Read Data</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>L</td>
<td>L</td>
<td>DATAIN Write Data</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>High-Z Output Disabled</td>
</tr>
<tr>
<td>H</td>
<td>X</td>
<td>X</td>
<td></td>
<td>High-Z Deselected – Standby</td>
</tr>
</tbody>
</table>

NOTE:
1. H = VIH, L = VIL, X = Don’t care.

Capacitance
(TA = +25°C, f = 1.0MHz, SOJ package)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter(2)</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td>VIN = 3dV</td>
<td>6</td>
<td>pF</td>
</tr>
<tr>
<td>CIO</td>
<td>I/O Capacitance</td>
<td>VOUT = 3dV</td>
<td>7</td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTE:
1. This parameter is guaranteed by device characterization, but is not production tested.

Absolute Maximum Ratings(1)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Supply Voltage Relative to GND</td>
<td>-0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td>VIN, VOUT</td>
<td>Terminal Voltage Relative to GND</td>
<td>-0.5 to VDD+0.5</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Commercial Operating Temperature</td>
<td>-0 to +70</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Industrial Operating Temperature</td>
<td>-40 to +85</td>
<td>°C</td>
</tr>
<tr>
<td>TBIAS</td>
<td>Temperature Under Bias</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>-55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>PT</td>
<td>Power Dissipation</td>
<td>1.25</td>
<td>W</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Temperature and Supply Voltage

<table>
<thead>
<tr>
<th>Grade</th>
<th>Temperature</th>
<th>GND</th>
<th>Vdd</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0°C to +70°C</td>
<td>0V</td>
<td>See Below</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40°C to +85°C</td>
<td>0V</td>
<td>See Below</td>
</tr>
</tbody>
</table>

Recommended DC Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD(1)</td>
<td>Supply Voltage</td>
<td>3.15</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VDD(2)</td>
<td>Supply Voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VSS</td>
<td>Ground</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>—</td>
<td>VDD+0.3(3)</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>−0.9(1)</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
</tbody>
</table>

NOTES:
1. For 71V124SA10 only.
2. For all speed grades except 71V124SA10.
3. VIL (max.) = VDD+2V for pulse width less than 5ns, once per cycle.
4. VIL (min.) = −2V for pulse width less than 5ns, once per cycle.

DC Electrical Characteristics
(VDD = Min. to Max., Commercial and Industrial Temperature Ranges)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ILI</td>
<td>Input Leakage Current</td>
<td>VDD = Max., VIN = GND to VDD</td>
<td>—</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td>VDD = Max., CS = VIN, VOUT = GND to VDD</td>
<td>—</td>
<td>5</td>
<td>µA</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Low Voltage</td>
<td>IOL = 8mA, VDD = Min.</td>
<td>—</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>IOH = −4mA, VDD = Min.</td>
<td>2.4</td>
<td>—</td>
<td>V</td>
</tr>
</tbody>
</table>
DC Electrical Characteristics\(^{(1, 2)}\)
(V\textsubscript{DD} = Min. to Max., V\textsubscript{LC} = 0.2V, V\textsubscript{HC} = V\textsubscript{DD} – 0.2V)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>71V124SA10</th>
<th>71V124SA12</th>
<th>71V124SA15</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC</td>
<td>Dynamic Operating Current() CS (&lt;) V\textsubscript{LC}, Outputs Open, V\textsubscript{DD} = Max., f = f\textsubscript{MAX}(^{(3)})()</td>
<td>145</td>
<td>130</td>
<td>140</td>
</tr>
<tr>
<td>Isb</td>
<td>Dynamic Standby Power Supply Current() CS (\geq) V\textsubscript{HC}, Outputs Open, V\textsubscript{DD} = Max., f = f\textsubscript{MAX}(^{(3)})()</td>
<td>45</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>Isb1</td>
<td>Full Standby Power Supply Current (static)() CS (\geq) V\textsubscript{HC}, Outputs Open, V\textsubscript{DD} = Max., f = 0(^{(3)})()</td>
<td>10</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

NOTES:
1. All values are maximum guaranteed values.
2. All inputs switch between 0.2V (Low) and V\textsubscript{DD}–0.2V (High).
3. f\textsubscript{MAX} = 1/RC (all address inputs are cycling at f\textsubscript{MAX}); f = 0 means no address input lines are changing.

AC Test Conditions

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Times</td>
<td>3ns</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>AC Test Load</td>
<td>See Figure 1 and 2</td>
</tr>
</tbody>
</table>

Figure 1. AC Test Load

Figure 2. AC Test Load\(^*\)
(for t\textsubscript{CLZ}, t\textsubscript{OLZ}, t\textsubscript{CHZ}, t\textsubscript{OHZ}, t\textsubscript{OW}, and t\textsubscript{WHZ})

\(^*\)Including jig and scope capacitance.
**AC Electrical Characteristics**  
*(VDD = Min. to Max., Commercial and Industrial Temperature Ranges)*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>71V124SA10</th>
<th>71V124SA12</th>
<th>71V124SA15</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
<td>Min.</td>
<td>Max.</td>
</tr>
</tbody>
</table>

**READ CYCLE**
- **tRC**: Read Cycle Time  
  - Symbol: tRC  
  - Min.: 10 ns  
  - Max.: 12 ns  
  - 71V124SA10: 15 ns

- **tAA**: Address Access Time  
  - Min.: 10 ns  
  - Max.: 12 ns  
  - 71V124SA12: 15 ns

- **tACS**: Chip Select Access Time  
  - Min.: 10 ns  
  - Max.: 12 ns  
  - 71V124SA15: 15 ns

- **tcz(1)**: Chip Select to Output in Low-Z  
  - Symbol: tcz(1)  
  - Min.: 4 ns  
  - Max.: 4 ns  
  - 71V124SA10: 4 ns

- **tcoz(1)**: Chip Deselect to Output in High-Z  
  - Symbol: tcoz(1)  
  - Min.: 0 ns  
  - Max.: 5 ns  
  - 71V124SA12: 6 ns  
  - 71V124SA15: 7 ns

- **toe**: Output Enable to Output Valid  
  - Symbol: toe  
  - Min.: 5 ns  
  - Max.: 6 ns  
  - 71V124SA15: 7 ns

- **tolz(1)**: Output Enable to Output in Low-Z  
  - Symbol: tolz(1)  
  - Min.: 0 ns  
  - Max.: 0 ns  
  - 71V124SA10: 0 ns

- **tox(1)**: Output Disable to Output in High-Z  
  - Symbol: tox(1)  
  - Min.: 0 ns  
  - Max.: 5 ns  
  - 71V124SA12: 6 ns  
  - 71V124SA15: 7 ns

- **tch**: Output Hold from Address Change  
  - Symbol: tch  
  - Min.: 4 ns  
  - Max.: 4 ns  
  - 71V124SA10: 4 ns

**WRITE CYCLE**
- **tWC**: Write Cycle Time  
  - Symbol: tWC  
  - Min.: 10 ns  
  - Max.: 12 ns  
  - 71V124SA15: 15 ns

- **tAW**: Address Valid to End-of-Write  
  - Symbol: tAW  
  - Min.: 7 ns  
  - Max.: 8 ns  
  - 71V124SA12: 10 ns

- **tcW**: Chip Select to End-of-Write  
  - Symbol: tcW  
  - Min.: 7 ns  
  - Max.: 8 ns  
  - 71V124SA15: 10 ns

- **tAS**: Address Set-up Time  
  - Symbol: tAS  
  - Min.: 0 ns  
  - Max.: 0 ns  
  - 71V124SA10: 0 ns

- **tWP**: Write Pulse Width  
  - Symbol: tWP  
  - Min.: 7 ns  
  - Max.: 8 ns  
  - 71V124SA15: 10 ns

- **tWR**: Write Recovery Time  
  - Symbol: tWR  
  - Min.: 0 ns  
  - Max.: 0 ns  
  - 71V124SA10: 0 ns

- **tdW**: Data Valid to End-of-Write  
  - Symbol: tdW  
  - Min.: 5 ns  
  - Max.: 6 ns  
  - 71V124SA15: 7 ns

- **tDH**: Data Hold Time  
  - Symbol: tDH  
  - Min.: 0 ns  
  - Max.: 0 ns  
  - 71V124SA10: 0 ns

- **tox(2)**: Output Active from End-of-Write  
  - Symbol: tox(2)  
  - Min.: 3 ns  
  - Max.: 3 ns  
  - 71V124SA15: 3 ns

- **twhz(2)**: Write Enable to Output in High-Z  
  - Symbol: twhz(2)  
  - Min.: 0 ns  
  - Max.: 5 ns  
  - 71V124SA12: 5 ns

**NOTES:**  
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
Timing Waveform of Read Cycle No. 1\(^{(1)}\)

Timing Waveform of Read Cycle No. 2\(^{(1, 2, 4)}\)

NOTES:
1. WE is HIGH for Read Cycle.
2. Device is continuously selected, \(\overline{CS}\) is LOW.
3. Address must be valid prior to or coincident with the later of \(\overline{CS}\) transition LOW; otherwise \(t_{AA}\) is the limiting parameter.
4. \(\overline{OE}\) is LOW.
5. Transition is measured ±200mV from steady state.
Timing Waveform of Write Cycle No. 1 (\textbf{WE} Controlled Timing)\(^{(1,2,4)}\)

NOTES:
1. A write occurs during the overlap of a LOW \(\text{CS}\) and a LOW \(\text{WE}\).
2. OE is continuously HIGH. During a WE controlled write cycle with OE LOW, \(t_{WP}\) must be greater than or equal to \(t_{WHZ} + t_{DW}\) to allow the I/O drivers to turn off and data to be placed on the bus for the required \(t_{OW}\). If OE is HIGH during a WE controlled write cycle, this requirement does not apply and the minimum write pulse is the specified \(t_{WP}\).
3. During this period, I/O pins are in the output state, and input signals must not be applied.
4. If the CS LOW transition occurs simultaneously with or after the WE LOW transition, the outputs remain in a high impedance state. CS must be active during the \(t_{CW}\) write period.
5. Transition is measured ±200mV from steady state.

Timing Waveform of Write Cycle No. 2 (\(\overline{\text{CS}}\) Controlled Timing)\(^{(1, 4)}\)
Ordering Information

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Power</th>
<th>Speed</th>
<th>Package</th>
<th>Process/ Temperature Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>71V124</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

- Blank
- 8: Tube or Tray
- 10: Commercial Only
- 12: Commercial and Industrial
- 15: Commercial and Industrial

- Blank
- I: Commercial (0°C to +70°C)
- Industrial (-40°C to +85°C)
- G: Green

- TY: 300-mil SOJ (SO32-2)
- Y: 400-mil SOJ (SO32-3)
- PH: TSOP Type II (SO32-4)

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Datasheet Document History

11/22/99   Updated to new format
            Pg. 1–4, 7  Added Industrial Temperature range offerings
            Pg. 2  Added Recommended Operating Temperature and Supply Voltage table
            Pg. 6  Revised footnotes on Write Cycle No. 1 diagram
            Pg. 8  Added Datasheet Document History

08/30/00  Pg. 3  Tighten lcc and lsb
            Pg. 4  Tighten AC Characteristics toh, tow and twhz

08/22/01  Pg. 7  Removed footnote "400-mil SOJ package only offered in 10ns and 12ns speed grade"

11/30/03  Pg. 1,3,7  Added Industrial temperature offering 10ns speed grade

01/30/04  Pg. 7  Added "Restricted hazardous substance device" to ordering information

2/14/07   Pg. 7  Added H generation die step to data sheet ordering information

10/13/08  Pg. 7  Removed "IDT" from the orderable part number

11/15/10  Pg. 1,3,4,7  Removed 20ns commercial, 10ns & 20ns industrial and also removed HSA offering

03/29/12  Pg. 7  Removed die step indicator from the ordering information
            Added tape and reel and green to the ordering information

02/19/13: Pg. 1  Removed IDT reference to fabrication and changed fastest access address time from 9ns to 10ns
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