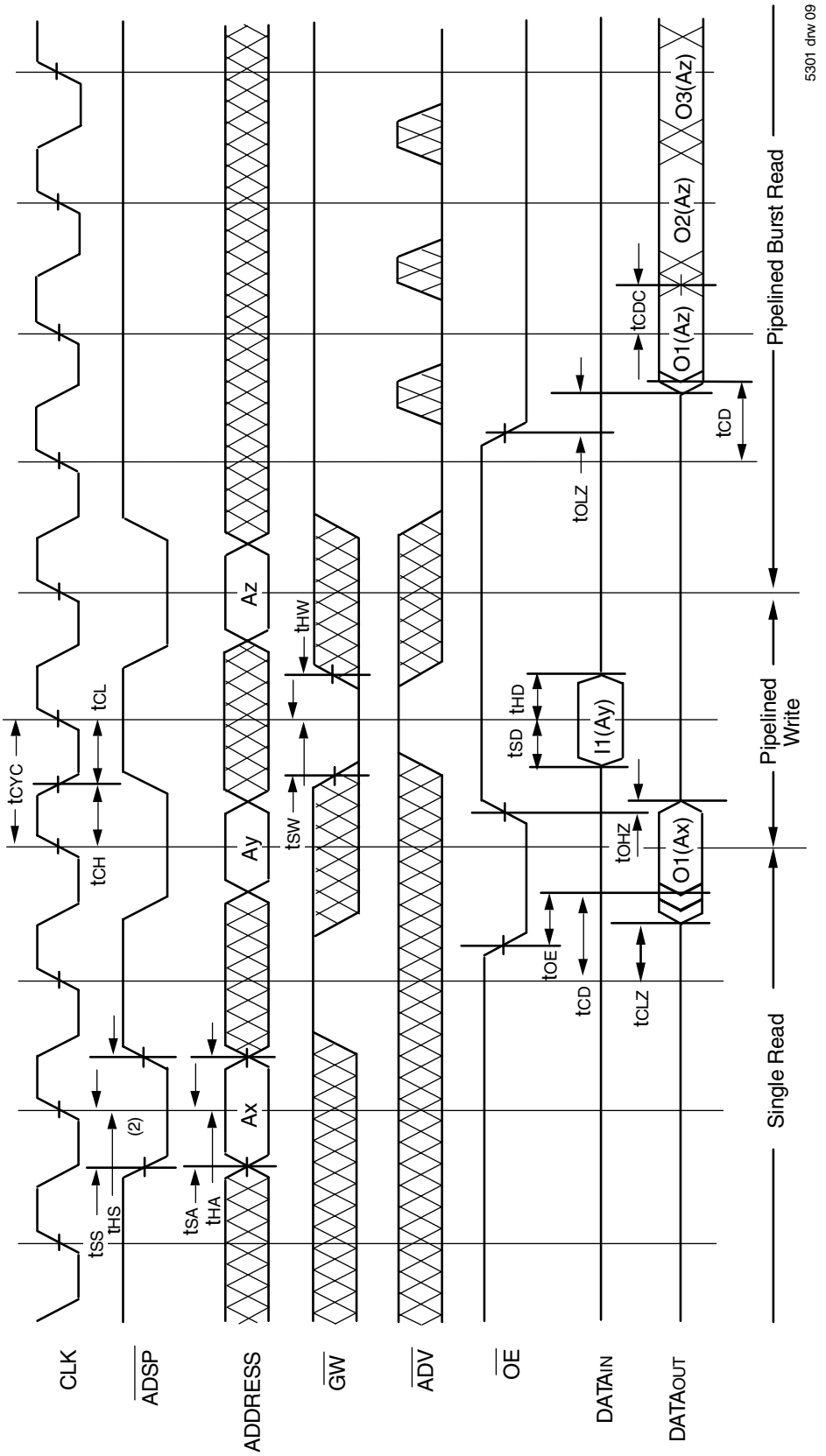
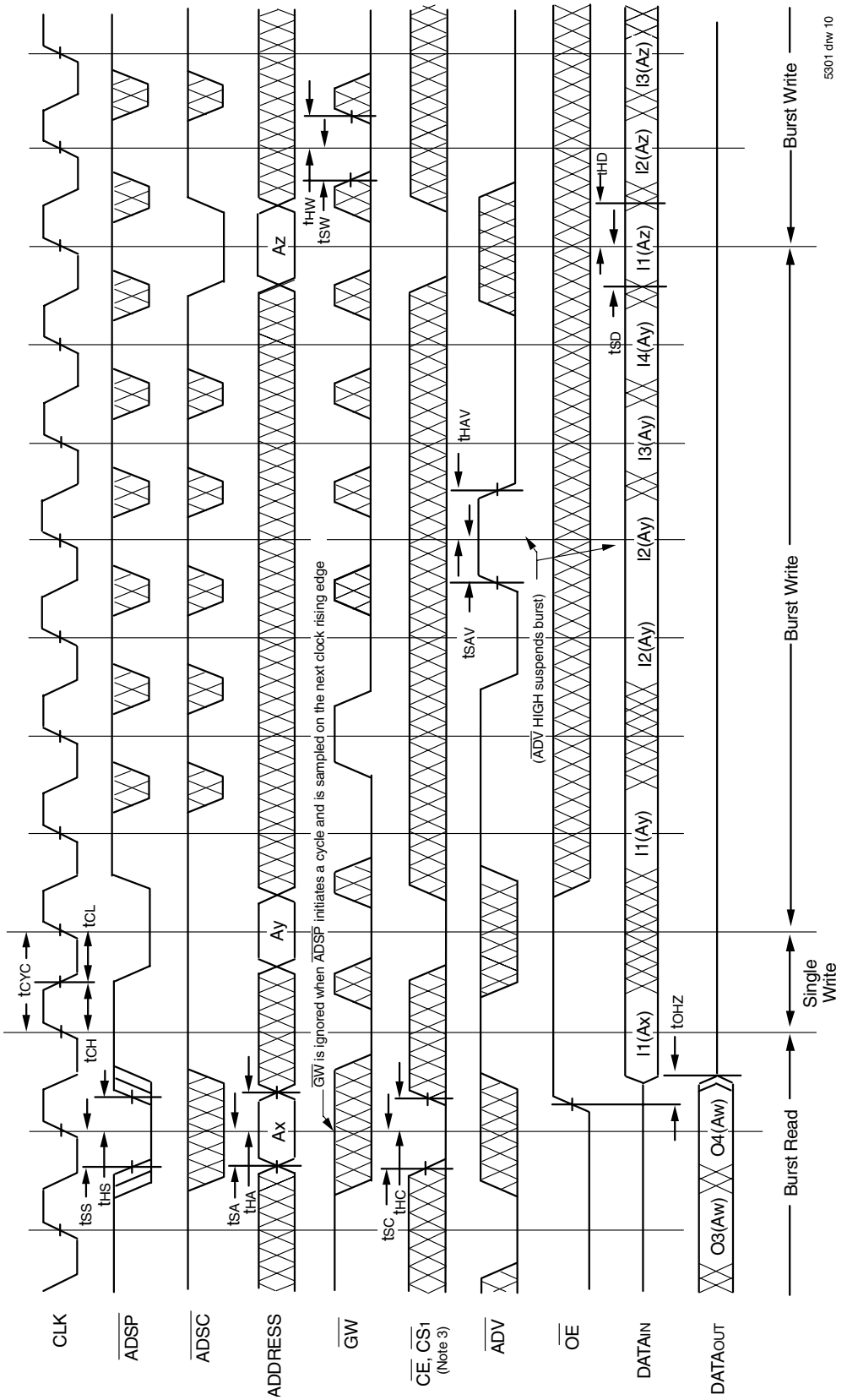
Timing Waveform of Combined Pipelined Read and Write Cycles(1,2,3)



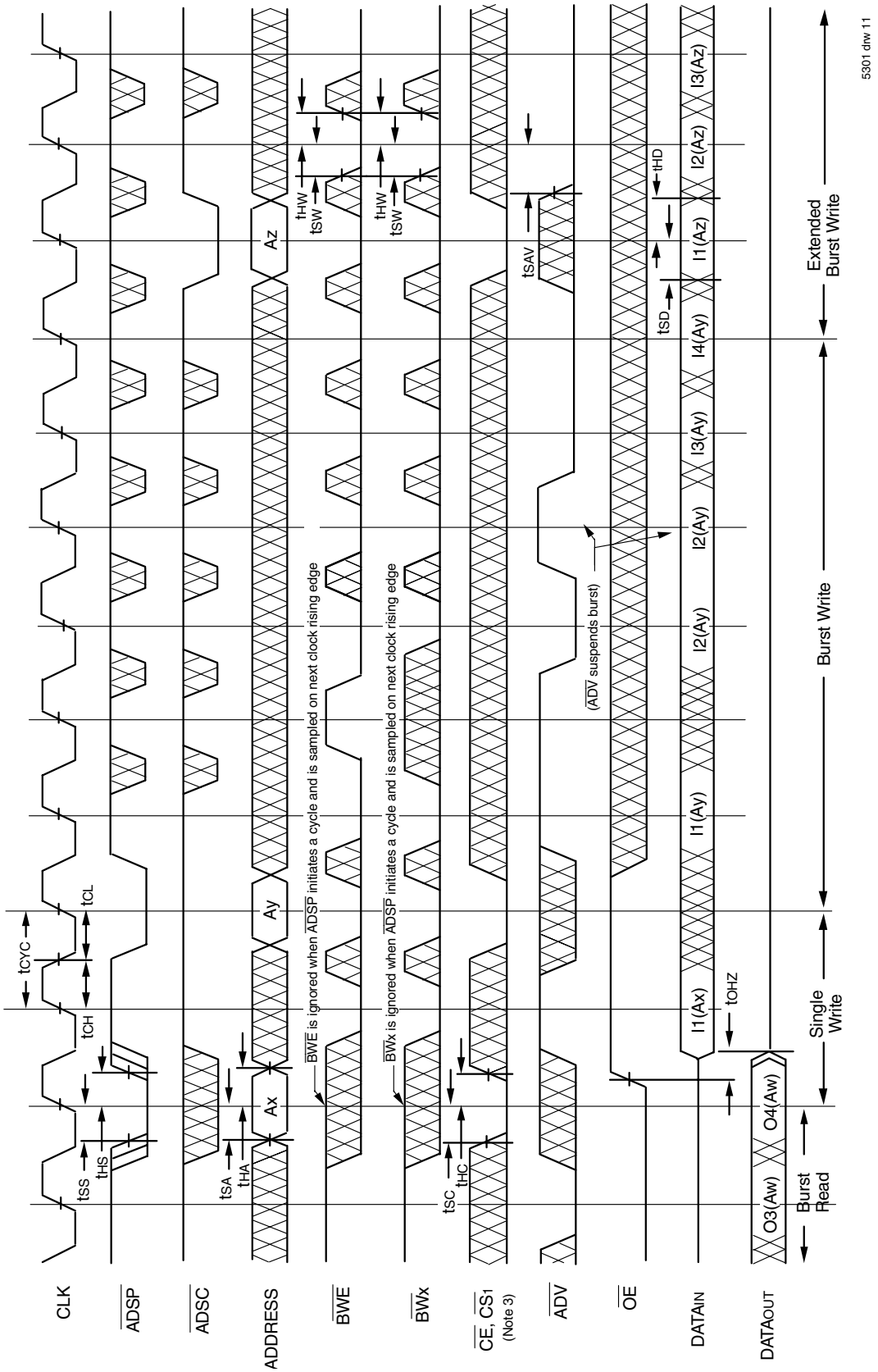
NOTES:
1. Device is selected through entire cycle; $\overline{CE}$ and $\overline{CS}1$ are LOW, CS0 is HIGH.
2. ZZ input is LOW and $\overline{LBO}$ is Don't Care for this cycle.
3. O1 (Ax) represents the first output from the external address Ax. I1 (Ay) represents the first input from the external address Ay; O1 (Az) represents the first output from the external address Az; O2 (Az) represents the next output data in the burst sequence of the base address Az, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input.

Timing Waveform of Write Cycle No. 1 - $\overline{GW}$ Controlled(1,2,3)



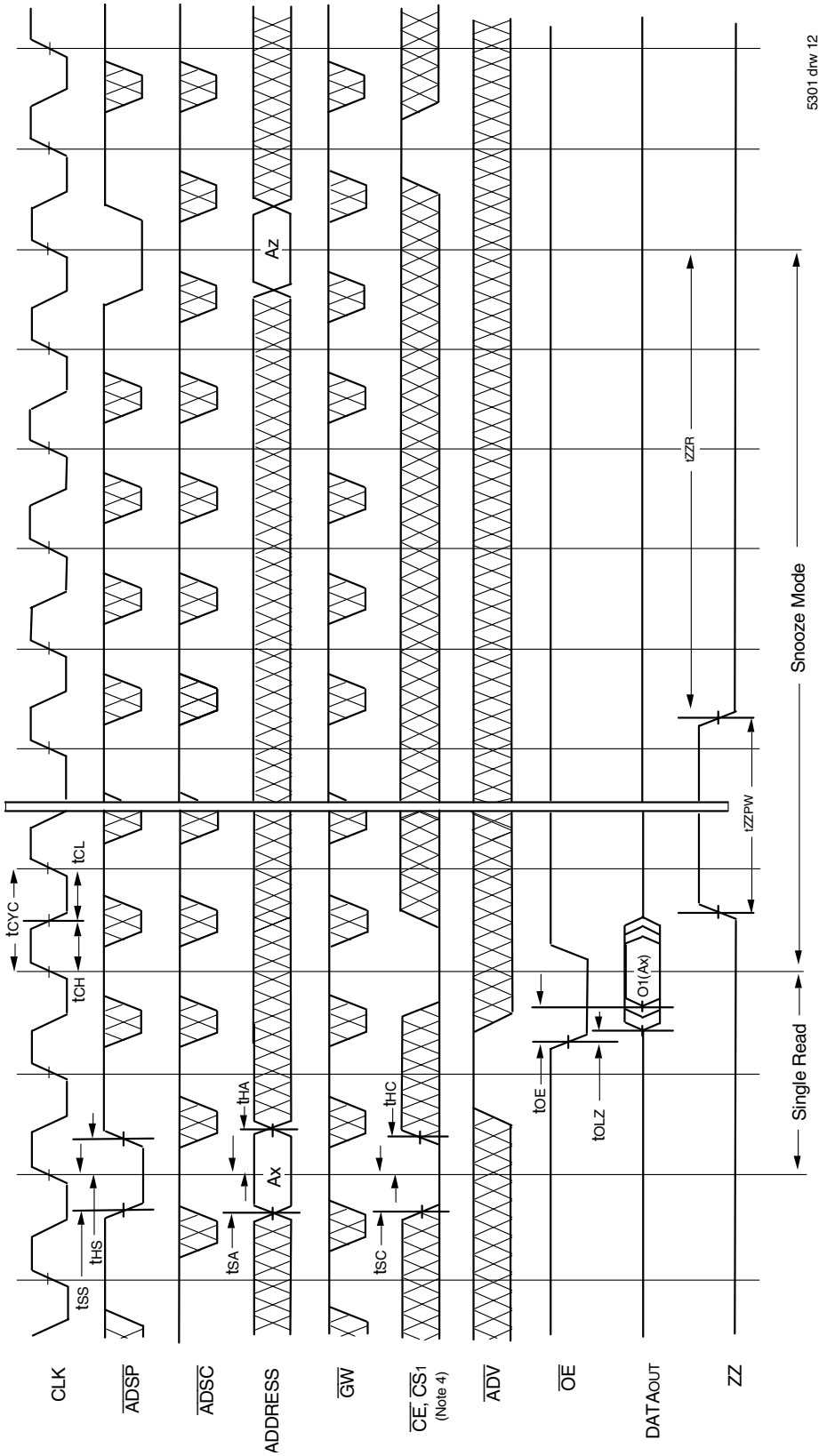
NOTES:
1. ZZ input is LOW, $\overline{BWE}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS1}$ signals. For example, when $\overline{CE}$ and $\overline{CS1}$ are LOW on this waveform, CS0 is HIGH.

Timing Waveform of Write Cycle No. 2 - Byte Controlled(1,2,3)



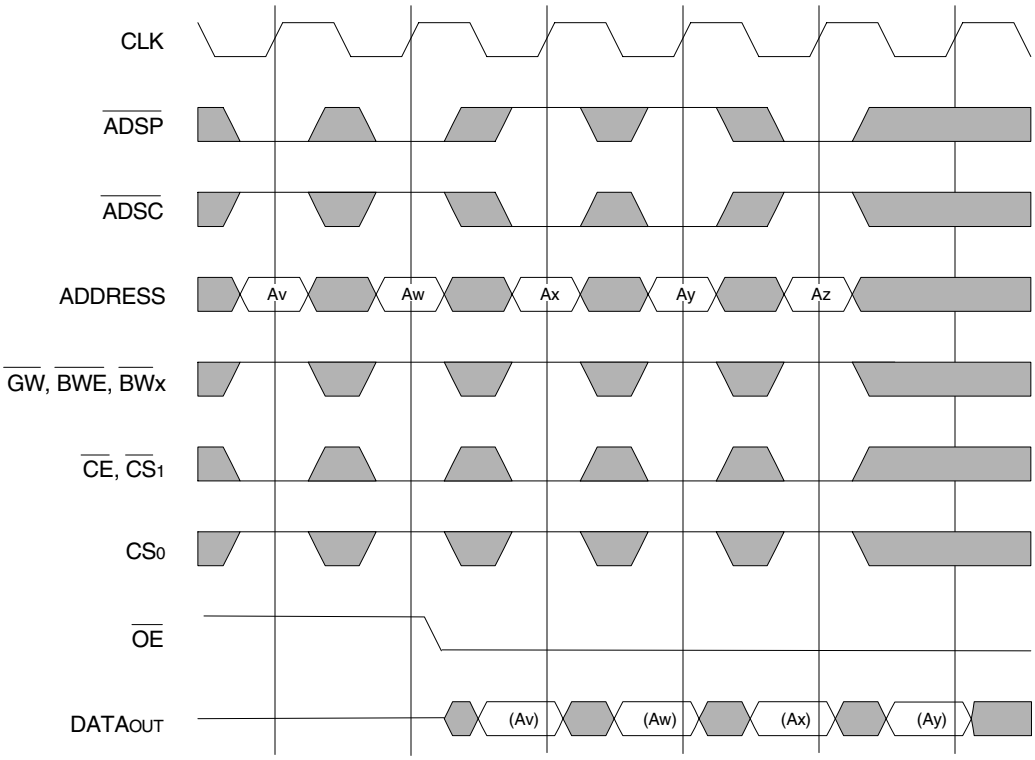
NOTES:
1. ZZ input is LOW, $\overline{GW}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. O4 (Aw) represents the final output data in the burst sequence of the base address Aw. I1 (Ax) represents the first input from the external address Ax. I1 (Ay) represents the first input from the external address Ay; I2 (Ay) represents the next input data in the burst sequence of the base address Ay, etc. where A0 and A1 are advancing for the four word burst in the sequence defined by the state of the $\overline{LBO}$ input. In the case of input I2 (Ay) this data is valid for two cycles because $\overline{ADV}$ is high and has suspended the burst.
3. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when $\overline{CE}$ and $\overline{CS}_1$ are LOW on this waveform, CS_0 is HIGH.

Timing Waveform of Sleep (ZZ) and Power-Down Modes(1,2,3)



NOTES:
1. Device must power up in deselected Mode
2. $\overline{LBO}$ is Don't Care for this cycle.
3. It is not necessary to retain the state of the input registers throughout the Power-down cycle.
4. CS_0 timing transitions are identical but inverted to the $\overline{CE}$ and $\overline{CS}_1$ signals. For example, when CE and CS1 are LOW on this waveform, CS_0 is HIGH.

Non-Burst Read Cycle Timing Waveform



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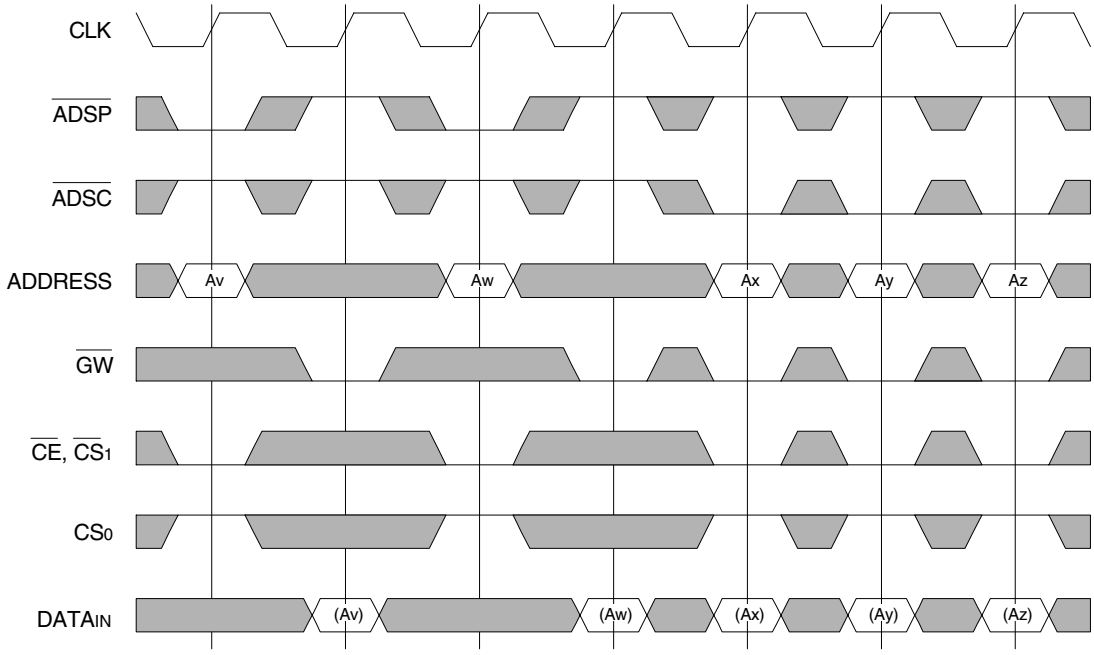
NOTES:
1. ZZ input is LOW, $\overline{ADV}$ is HIGH and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. For read cycles, $\overline{ADSP}$ and $\overline{ADSC}$ function identically and are therefore interchangable.

Non-Burst Write Cycle Timing Waveform



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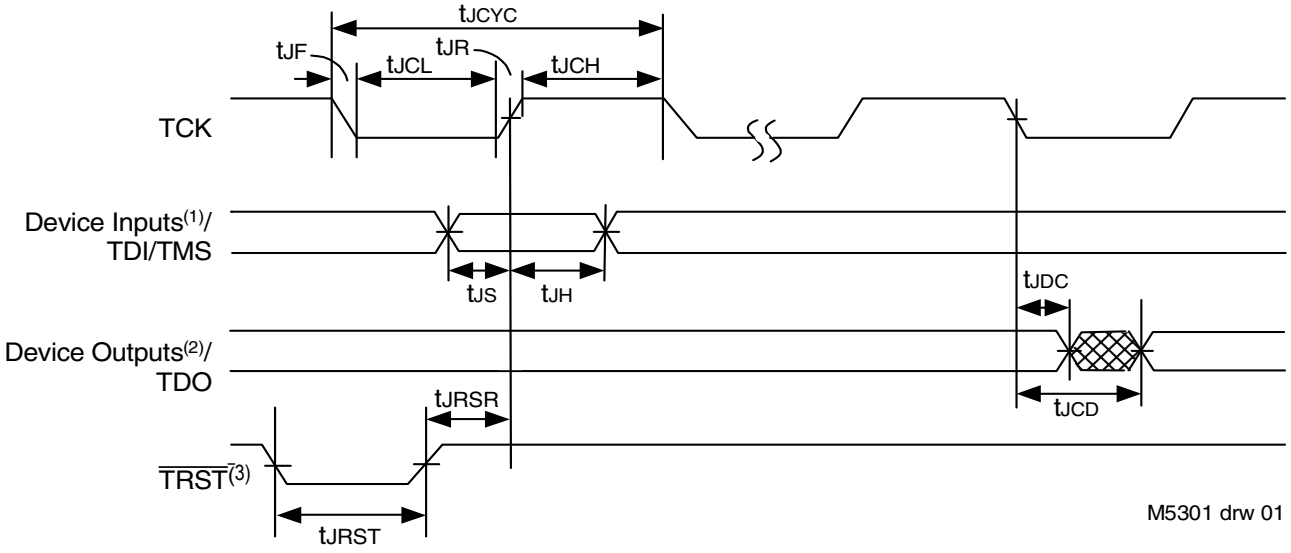
NOTES:
1. ZZ input is LOW, $\overline{ADV}$ and $\overline{OE}$ are HIGH, and $\overline{LBO}$ is Don't Care for this cycle.
2. (Ax) represents the data for address Ax, etc.
3. Although only $\overline{GW}$ writes are shown, the functionality of $\overline{BWE}$ and $\overline{BWx}$ together is the same as $\overline{GW}$.
4. For write cycles, $\overline{ADSP}$ and $\overline{ADSC}$ have different limitations.

JTAG Interface Specification (SA Version only)



NOTES:
1. Device inputs = All device inputs except TDI, TMS and $\overline{\text{TRST}}$.
2. Device outputs = All device outputs except TDO.
3. During power up, $\overline{\text{TRST}}$ could be driven low or not be used since the JTAG circuit resets automatically. $\overline{\text{TRST}}$ is an optional JTAG reset.

JTAG AC Electrical Characteristics(1,2,3,4)

Symbol	Parameter	Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	5(1)	ns
t_{JF}	JTAG Clock Fall Time	—	5(1)	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	20	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	25	—	ns
t_{JH}	JTAG Hold	25	—	ns

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NOTES:
1. Guaranteed by design.
2. AC Test Load (Fig. 1) on external output signals.
3. Refer to AC Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
JTAG Identification (JIDR)	32
Boundary Scan (BSR)	Note (1)

I5301 tbl 03

NOTE:
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available by contacting your local IDT sales representative.

JTAG Identification Register Definitions (SA Version only)

Instruction Field	Value	Description
Revision Number (31:28)	0x2	Reserved for version number.
IDT Device ID (27:12)	0x23C, 0x23E	Defines IDT part number 71V35761SA.
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT.
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register.

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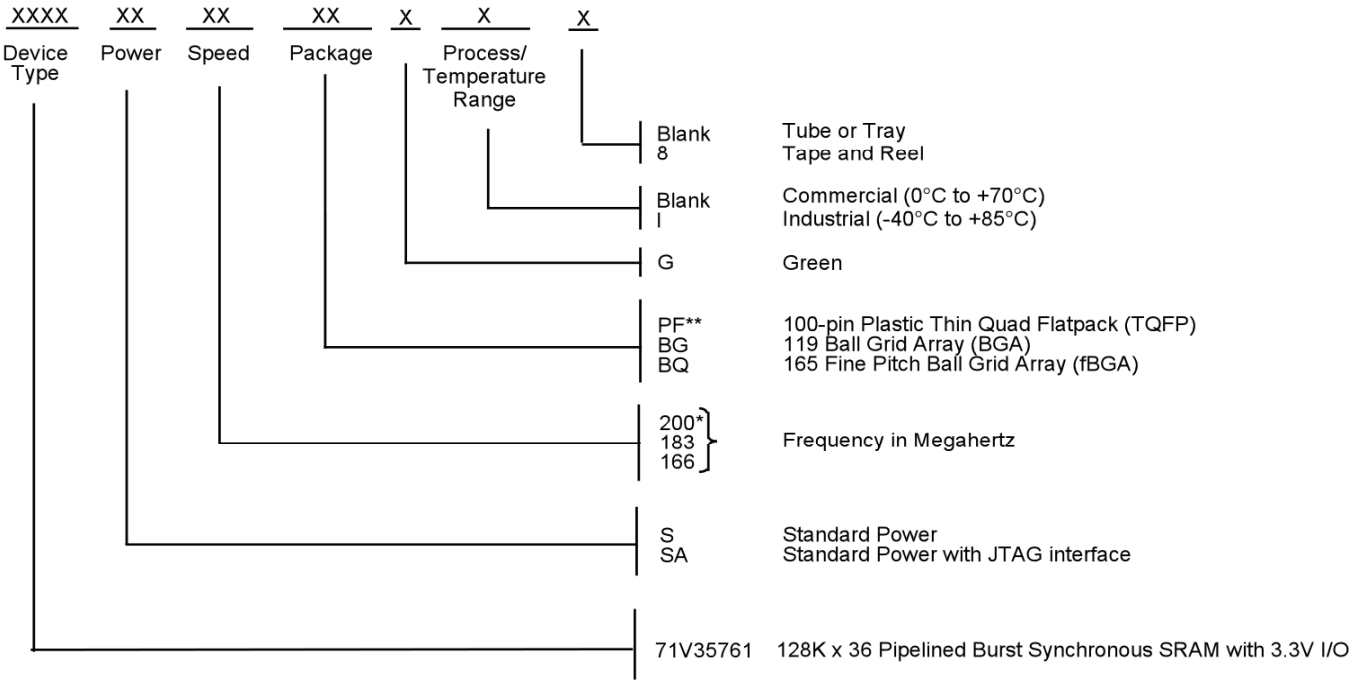
Available JTAG Instructions

Instruction	Description	OPCODE
EXTEST	Forces contents of the boundary scan cells onto the device outputs[1]. Places the boundary scan register (BSR) between TDI and TDO.	0000
SAMPLE/PRELOAD	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs[2] and outputs[1] to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.	0001
DEVICE_ID	Loads the JTAG ID register (JIDR) with the vendor ID code and places the register between TDI and TDO.	0010
HIGHZ	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state.	0011
RESERVED	Several combinations are reserved. Do not use codes other than those identified for EXTEST, SAMPLE/PRELOAD, DEVICE_ID, HIGHZ, CLAMP, VALIDATE and BYPASS instructions.	0100
RESERVED		0101
RESERVED		0110
RESERVED		0111
CLAMP	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.	1000
RESERVED	Same as above.	1001
RESERVED		1010
RESERVED		1011
RESERVED		1100
VALIDATE	Automatically loaded into the instruction register whenever the TAP controller passes through the CAPTURE-IR state. The lower two bits '01' are mandated by the IEEE std. 1149.1 specification.	1101
RESERVED	Same as above.	1110
BYPASS	The BYPASS instruction is used to truncate the boundary scan register as a single bit in length.	1111

I5301 tbl 04

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{\text{TRST}}$.

Ordering Information



*Commercial temperature range only
** JTAG (SA version) is not available with 100 pin TQFP package.

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Package Information

100-Pin Thin Quad Plastic Flatpack (TQFP)
119 Ball Grid Array (BGA)
165 Fine Pitch Ball Grid Array (fBGA)
Information available on the IDT website

Datasheet Document History

12/31/99		Created new datasheet from 71v3576 and 71v3578 datasheet.
	Pg. 1, 4, 8, 11, 19	Added industrial temperature range offering from 166MHz and 183MHz
04/04/00	Pg. 18	Added 100 pin TQFP package Diagram Outline
	Pg. 4	Add BGA capacitance table; Add industrial temperature to table; Insert note to Absolute Max Rating and Recommended Operating Temperature tables
06/01/00		Add new package diagram outline, 13 x 15mm 165fBGA
	Pg. 20	Correct BG119 Package Diagram Outline
07/15/00	Pg. 7	Add note reference to BG119 pinout
	Pg. 8	Add DNU reference note to BQ165 pinout
	Pg. 20	Update BG119 Package Diagram Outline Dimensions
10/25/00		Remove Preliminary status
	Pg. 8	Add reference note to N5 on the BQ165 pinout, reserved for JTAG $\overline{\text{TRST}}$
04/22/03	Pg.4	Updated 165 BGA table information from TBD to 7
06/30/03	Pg. 1,2,3,5-9	Updated datasheet with JTAG information
	Pg. 5-8	Removed note for NC pins (38,39(PF package); L4, U4 (BG package) H2, N7 (BQ package)) requiring NC or connection to Vss.
	Pg. 19,20	Added two pages of JTAG Specification, AC Electrical, Definitions and Instructions
	Pg. 21-23	Removed old package information from the datasheet
	Pg. 24	Updated ordering information with JTAG and Y stepping information. Added information regarding packages available IDT website.
03/02/09	Pg. 21	Removed "IDT" from orderable part number
06/01/10	Pg. 1-21	Added "Restricted hazardous substance device" to the ordering information. Removed IDT71V35781S/SA from datasheet.
08/01/14	Pg. 1-3	Moved the FBD, the pin description and pin definition tables to pages 1 - 3 respectively to align the datasheet reading flow to that of our other established datasheets
	Pg. 20	In the Ordering Information, Tape & Reel added & RoHS designation changed to Green
11/06/14	Pg. 1	Removed "Y" stepping from the datasheet part number. Changed DS Device to IDT71V35761S/SA
	Pg. 1	In Features: Added text: "Green parts available, see ordering information"
	Pg. 2	In Description: Clarified text in last paragraph
	Pg. 3	Removed device 71V35781 in the Pin Definitions Table
	Pg. 21	Removed stepping from Ordering Information
	Pg. 22	Updated sramhelp contact information