

FEATURES

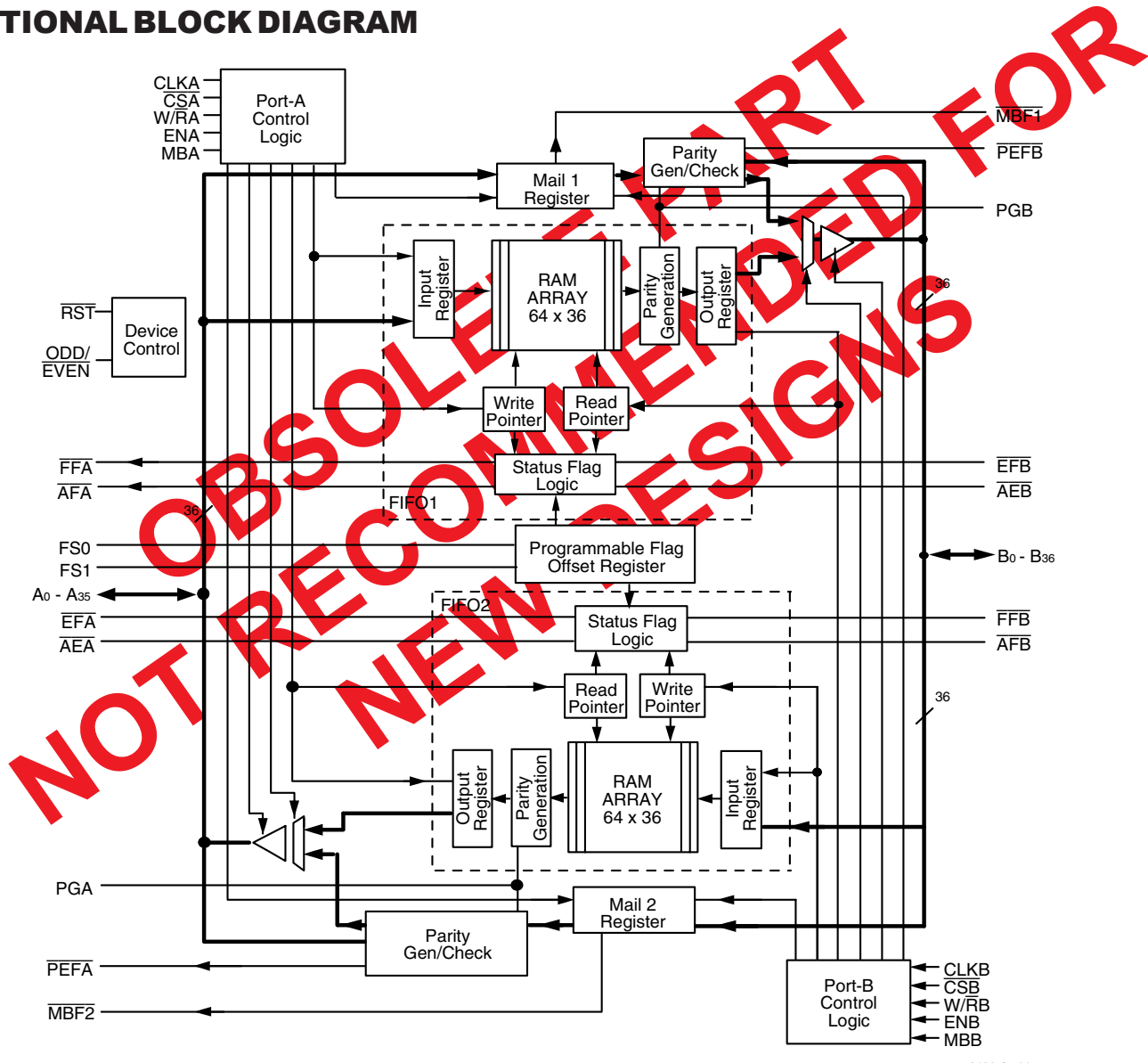
- Free-running CLKA and CLKB can be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
- Two independent clocked FIFOs (64 x 36 storage capacity each) buffering data in opposite directions
- Mailbox bypass Register for each FIFO
- Programmable Almost-Full and Almost-Empty Flags
- Microprocessor interface control logic
- \overline{EFA} , \overline{FFA} , \overline{AEA} , and \overline{AFA} flags synchronized by CLKA
- \overline{EFB} , \overline{FFB} , \overline{AEB} , and \overline{AFB} flags synchronized by CLKB
- Passive parity checking on each port
- Parity generation can be selected for each port

- Supports clock frequencies up to 67 MHz
- Fast access times of 10ns
- Available in 132-pin plastic quad flat package (PQF) or space-saving 120-pin thin quad flat package (TQFP)
- Industrial temperature range (-40°C to +85°C) is available
- Green parts available, see ordering information

DESCRIPTION

The IDT723612 is a monolithic high-speed, low-power CMOS bi-directional clocked FIFO memory. It supports clock frequencies up to 67 MHz and has read access times as fast as 10ns. Two independent 64 x 36 dual-port SRAM FIFOs on board the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions and two programmable flags (Almost-Full and

FUNCTIONAL BLOCK DIAGRAM



3136 drw01

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Almost-Empty) to indicate when a selected number of words is stored in memory. Communication between each port can bypass the FIFOs via two 36-bit mailbox registers. Each mailbox register has a flag to signal when new mail has been stored. Parity is checked passively on each port and may be ignored if not desired. Parity generation can be selected for data read from each port. Two or more devices can be used in parallel to create wider data paths.

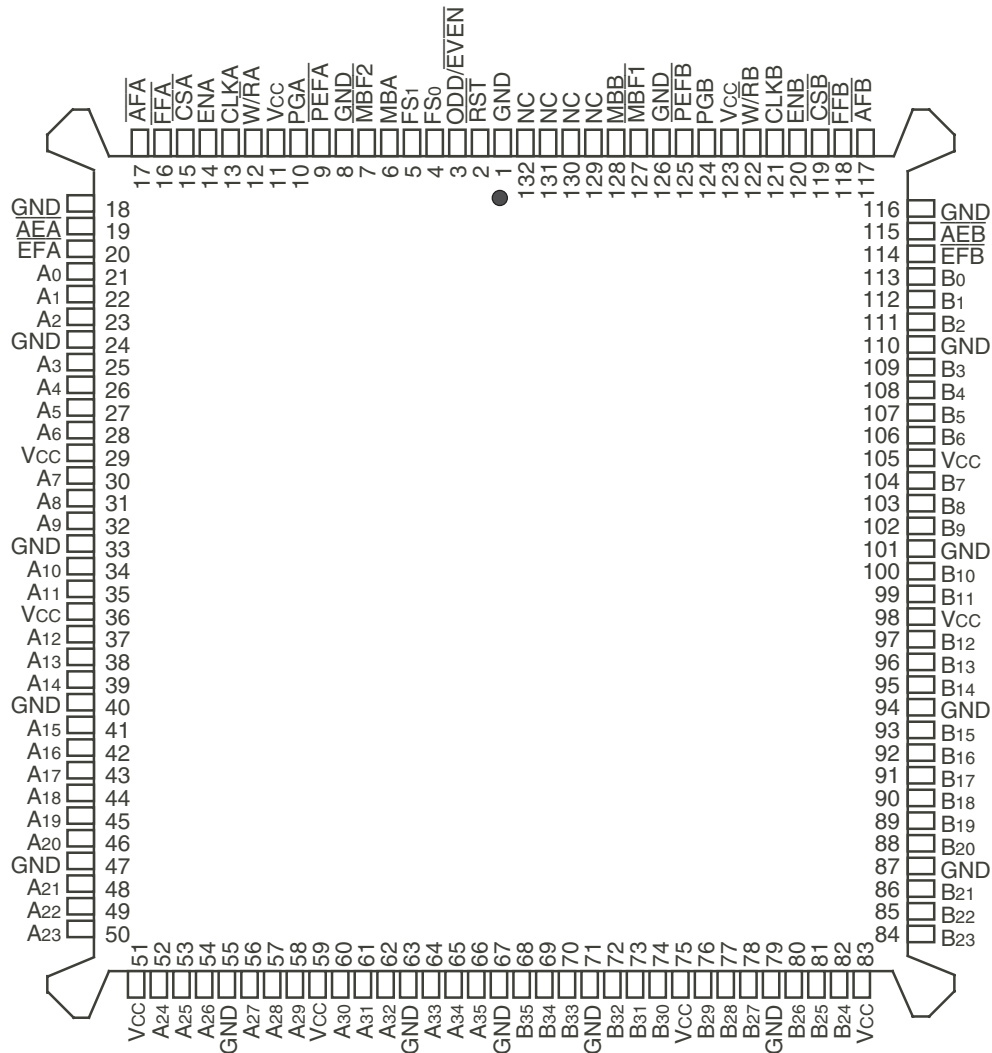
This device is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH

transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bi-directional interface between microprocessors and/or buses with synchronous control.

The Full Flag (FFA, FFB) and Almost-Full (AFA, AFB) flag of a FIFO are two-stage synchronized to the port clock that writes data to its array. The Empty Flag (EFA, EFB) and Almost-Empty (AEA, AEB) flag of a FIFO are two stage synchronized to the port clock that reads data from its array.

The IDT723612 is characterized for operation from 0°C to 70°C.

PIN CONFIGURATIONS



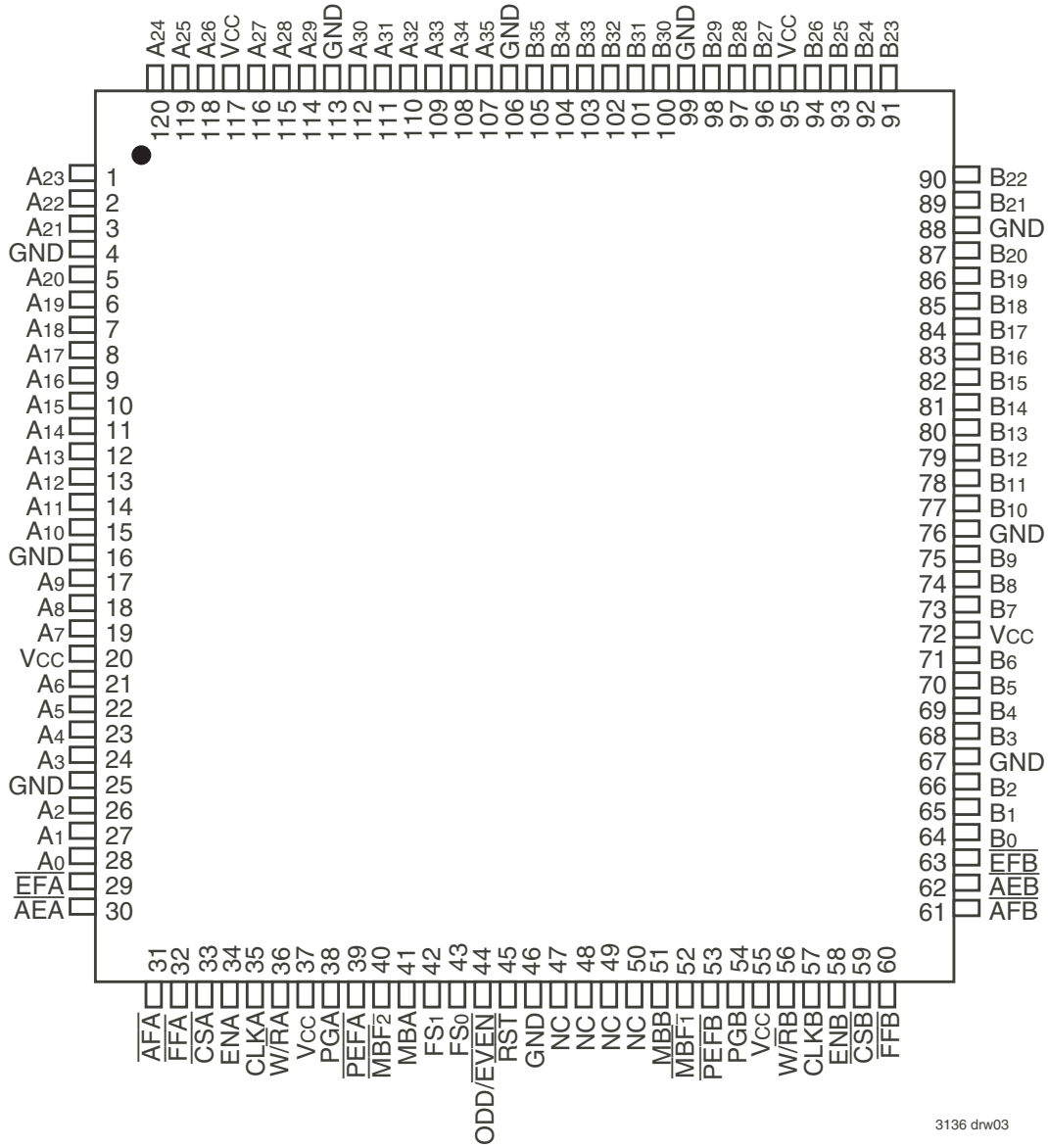
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NOTES:

1. Electrical pin 1 in center of beveled edge.
2. NC - No internal connection
3. Uses Yamaichi socket IC51-1324-828

PQFP⁽²⁾ (PQ132-1, ORDER CODE: PQF)
TOP VIEW

PIN CONFIGURATIONS (CONTINUED)



3136 drw03

NOTES:

1. Pin 1 identifier in corner.
2. NC - No internal connection

TQFP (PN120-1, ORDER CODE: PF)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
A0-A35	Port-A Data	I/O	36-bit bidirectional data port for side A.
\overline{AEA}	Almost-Empty Flag	O (Port A)	Programmable Almost-Empty flag synchronized to CLKA. It is LOW when the number of words in the FIFO2 is less than or equal to the value in the offset register, X.
AEB	Port-B Almost-Empty Flag	O (Port B)	Programmable Almost-Full flag synchronized to CLKB. It is LOW when the number of words in FIFO1 is less than or equal to the value in the offset register, X.
\overline{AFA}	Port-A Almost-Full Flag	O (Port A)	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the offset register, X.
\overline{AFB}	Port-B Almost-Empty Flag	O (Port B)	Programmable Almost-Full flag synchronized to CLKB. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the offset register, X.
B0-B35	Port-B Data.	I/O	36-bit bidirectional data port for side B.
CLKA	Port-A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through port-A and can be asynchronous or coincident to CLKB. \overline{EFA} , \overline{FFA} , \overline{AFA} , and \overline{AEA} are synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port-B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through port-B and can be asynchronous or coincident to CLKA. \overline{EFB} , \overline{FFB} , \overline{AFB} , and \overline{AEB} are synchronized to the LOW-to-HIGH transition of CLKB.
\overline{CSA}	Port-A Chip Select	I	\overline{CSA} must be LOW to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A. The A0-A35 outputs are in the high-impedance state when \overline{CSA} is HIGH.
\overline{CSB}	Port-B Chip Select	I	\overline{CSB} must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B. The B0-B35 outputs are in the high-impedance state when \overline{CSB} is HIGH.
\overline{EFA}	Port-A Empty Flag	O (Port A)	\overline{EFA} is synchronized to the LOW-to-HIGH transition of CLKA. When \overline{EFA} is LOW, FIFO2 is empty, and reads from its memory are disabled. Data can be read from FIFO2 to the output register when \overline{EFA} is HIGH. \overline{EFA} is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after data is loaded into empty FIFO2 memory.
\overline{EFB}	Port-B Empty Flag	O (Port B)	\overline{EFB} is synchronized to the LOW-to-HIGH transition of CLKB. When \overline{EFB} is LOW, the FIFO1 is empty, and reads from its memory are disabled. Data can be read from FIFO1 to the output register when \overline{EFB} is HIGH. \overline{EFB} is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after data is loaded into empty FIFO1 memory.
ENA	Port-A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on port-A.
ENB	Port-B Enable	I	ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on port-B.
\overline{FFA}	Port-A Full Flag	O (Port A)	\overline{FFA} is synchronized to the LOW-to-HIGH transition of CLKA. When \overline{FFA} is LOW, FIFO1 is full, and writes to its memory are disabled. \overline{FFA} is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKA after reset.
\overline{FFB}	Port-B Full Flag	O (Port B)	\overline{FFB} is synchronized to the LOW-to-HIGH transition of CLKB. When \overline{FFB} is LOW, FIFO2 is full, and writes to its memory are disabled. \overline{FFB} is forced LOW when the device is reset and is set HIGH by the second LOW-to-HIGH transition of CLKB after reset.
FS1, FS0	Flag-Offset Selects	I	The LOW-to-HIGH transition of \overline{RST} latches the values of FS0 and FS1, which selects one of four preset values for the Almost-Full flag and almost-Empty flag.
MBA	Port-A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a port-A read or write operation. When the A0-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output, and a LOW level selects FIFO2 output register data for output.
MBB	Port-B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a port-B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output, and a LOW level selects FIFO1 output register data for output.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is set LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a port-B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH when the device is reset.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is set LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a port-A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH when the device is reset.

PIN DESCRIPTION (CONTINUED)

Symbol	Name	I/O	Description
ODD/ EVEN	Odd/Even Parity Select	I	Odd parity is checked on each port when ODD/ <u>EVEN</u> is HIGH, and even parity is checked when ODD/ <u>EVEN</u> is LOW. ODD/ <u>EVEN</u> also selects the type of parity generated for each port if parity generation is enabled for a read operation.
<u>PEFA</u>	Port-A Parity Error Flag	O (Port A)	When any byte applied to terminals A0-A35 fails parity, <u>PEFA</u> is LOW. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35, with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/ <u>EVEN</u> input. The parity trees used to check the A0-A35 inputs are shared by the mail2 register to generate parity if parity generation is selected by PGA. Therefore, if a mail2 read with parity generation is setup by having W/ <u>RA</u> LOW, MBA HIGH, and PGA HIGH, the <u>PEFA</u> flag is forced HIGH regardless of the A0-A35 inputs.
<u>PEFB</u>	Port-B Parity Error Flag	O (Port B)	When any byte applied to terminals B0-B35 fails parity, <u>PEFB</u> is LOW. Bytes are organized as B0-B8, B9-B17, B18-B26, B27-B35 with the most significant bit of each byte serving as the parity bit. The type of parity checked is determined by the state of the ODD/ <u>EVEN</u> input. The parity trees used to check the B0-B35 inputs are shared by the mail1 register to generate parity if parity generation is selected by PGB. Therefore, if a mail1 read with parity generation is setup by having W/ <u>RB</u> LOW, MBB HIGH, and PGB HIGH, the <u>PEFB</u> flag is forced HIGH regardless of the state of the B0-B35 inputs.
PGA	Port-A Parity	I	Parity is generated for data reads from port A when PGA is HIGH. Generation The type of parity generated is selected by the state of the ODD/ <u>EVEN</u> input. Bytes are organized as A0-A8, A9-A17, A18-A26, and A27-A35. The generated parity bits are output in the most significant bit of each byte.
PGB	Port-B Parity	I	Parity is generated for data reads from port B when PGB is HIGH. The type of parity generated is selected by the state of the ODD/ <u>EVEN</u> input. Bytes are organized as B0-B8, B9-B17, B18-B26, and B27-B35. The generated parity bits are output in the most significant bit of each byte.
<u>RST</u>	Reset	I	To reset the device, four LOW-to-HIGH transitions of <u>CLKA</u> and four LOW-to-HIGH transitions of <u>CLKB</u> must occur while <u>RST</u> is LOW. This sets the <u>AFA</u> , <u>AFB</u> , <u>MBF1</u> , and <u>MBF2</u> flags HIGH and the <u>EFA</u> , <u>EFB</u> , <u>AEA</u> , <u>AEB</u> , <u>FFA</u> , and <u>FFB</u> flags LOW. The LOW-to-HIGH transition of <u>RST</u> latches the status of the <u>FS1</u> and <u>FS0</u> inputs to select Almost-Full and Almost-Empty flag offset.
W/ <u>RA</u>	Port-A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port A for a LOW-to-HIGH transition of <u>CLKA</u> . The A0-A35 outputs are in the high-impedance state when W/ <u>RA</u> is HIGH.
W/ <u>RB</u>	Port-B Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on port B for a LOW-to-HIGH transition of <u>CLKB</u> . The B0-B35 outputs are in the high-impedance state when W/ <u>RB</u> is HIGH.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)⁽²⁾

Symbol	Rating	Commercial	Unit
V _{CC}	Supply Voltage Range	-0.5 to 7	V
V _I ⁽²⁾	Input Voltage Range	-0.5 to V _{CC} +0.5	V
V _O ⁽²⁾	Output Voltage Range	-0.5 to V _{CC} +0.5	V
I _{IK}	Input Clamp Current, (V _I < 0 or V _I > V _{CC})	±20	mA
I _{OK}	Output Clamp Current, (V _O < 0 or V _O > V _{CC})	±50	mA
I _{OUT}	Continuous Output Current, (V _O = 0 to V _{CC})	±50	mA
I _{CC}	Continuous Current Through V _{CC} or GND	±500	mA
T _{STG}	Storage Temperature Range	-65 to 150	°C

NOTES:

- Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.5	V
V _{IH}	HIGH Level Input Voltage	2	—	V
V _{IL}	LOW-Level Input Voltage	—	0.8	V
I _{OH}	HIGH-Level Output Current	—	-4	mA
I _{OL}	LOW-Level Output Current	—	8	mA
T _A	Operating Free-air Temperature	0	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

Parameter	Test Conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
V _{OH}	V _{CC} = 4.5V, I _{OH} = -4 mA	2.4	—	—	V
V _{OL}	V _{CC} = 4.5V, I _{OL} = 8 mA	—	—	0.5	V
I _{LI}	V _{CC} = 5.5V, V _I = V _{CC} or 0	—	—	±50	μA
I _{LO}	V _{CC} = 5.5V, V _O = V _{CC} or 0	—	—	±50	μA
I _{CC} ⁽²⁾	V _{CC} 5.5V, I _O = 0 mA, V _I = V _{CC} or GND	—	—	1	mA
C _{IN}	V _I = 0, f = 1 MHz	—	4	—	pF
C _{OUT}	V _O = 0, f = 1 MHz	—	8	—	pF

NOTES:

- All typical values are at V_{CC} = 5V, T_A = 25°C.
- For additional I_{CC} information, see following page.

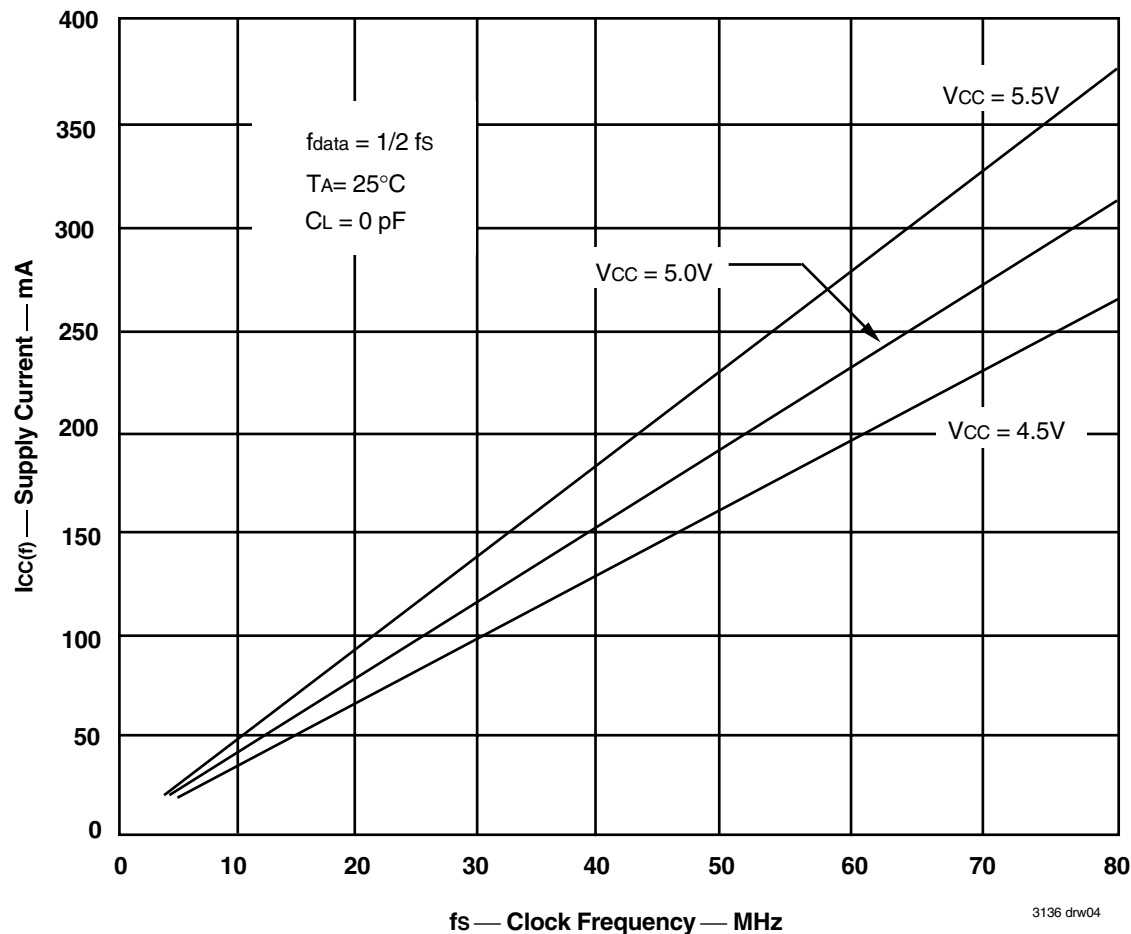


Figure 1. Typical Characteristics: Supply Current vs Clock Frequency

CALCULATING POWER DISSIPATION

The $I_{CC}(f)$ current for the graph in Figure 1 was taken while simultaneously reading and writing the FIFO on the IDT723612 with CLKA and CLKB set to f_s . All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero-capacitance load. Once the capacitance load per data-output channel is known, the power dissipation can be calculated with the equation below.

With $I_{CC}(f)$ taken from Figure 1, the maximum power dissipation (P_D) of the IDT723612 may be calculated by:

$$P_D = V_{CC} \times I_{CC}(f) + \sum (C_L \times V_{CC} \times (V_{OH} - V_{OL}) \times f_o)$$

where:

- CL = output capacitance load
- f_o = switching frequency of an output
- V_{OH} = output HIGH level voltage
- V_{OL} = output LOW level voltage

When no reads or writes are occurring on the IDT723612, the power dissipated by a single clock (CLKA or CLKB) input running at frequency f_s is calculated by:

$$P_T = V_{CC} \times f_s \times 0.290 \text{ mA/MHz}$$

DC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

(Commercial: VCC = 5.0V ±10%, TA = 0°C to +70°C; Industrial; VCC = 5.0V ± 10%, TA = 40°C to +85°C)

Symbol	Parameter	Commercial		Com'l & Ind'l ⁽¹⁾		Unit
		IDT723612L15		IDT723612L20		
		Min.	Max.	Min.	Max.	
t _S	Clock Frequency, CLKA or CLKB	–	66.7	–	50	MHz
t _{CLK}	Clock Cycle Time, CLKA or CLKB	15	–	20	–	ns
t _{CLKH}	Pulse Duration, CLKA and CLKB HIGH	6	–	8	–	ns
t _{CLKL}	Pulse Duration, CLKA and CLKB LOW	6	–	8	–	ns
t _{DS}	Setup Time, A0-A35 before CLKA↑ and B0-B35 before CLKB↑	4	–	5	–	ns
t _{ENS1}	Setup Time, \overline{CSA} , $\overline{W/RA}$ before CLKA↑; \overline{CSB} , $\overline{W/RB}$ before CLKB↑	6	–	6	–	ns
t _{ENS2}	Setup Time, ENA, before CLKA↑; ENB before CLKB↑	4	–	5	–	ns
t _{ENS3}	Setup Time, MBA before CLKA↑; MBB before CLKB↑	4	–	5	–	ns
t _{PGS}	Setup Time, $\overline{ODD/EVEN}$ and PGA before CLKA↑; $\overline{ODD/EVEN}$ and PGB before CLKB↑ ⁽²⁾	4	–	5	–	ns
t _{RSTS}	Setup Time, \overline{RST} LOW before CLKA↑ or CLKB↑ ⁽³⁾	5	–	6	–	ns
t _{FSS}	Setup Time, FS0/FS1 before \overline{RST} HIGH	5	–	6	–	ns
t _{DH}	Hold Time, A0-A35 after CLKA↑ and B0-B35 after CLKB↑	2.5	–	2.5	–	ns
t _{ENH1}	Hold Time, \overline{CSA} , $\overline{W/RA}$ after CLKA↑; \overline{CSB} , $\overline{W/RB}$ after CLKB↑	2	–	2	–	ns
t _{ENH2}	Hold Time, ENA, after CLKA↑; ENB after CLKB↑	2.5	–	2.5	–	ns
t _{ENH3}	Hold Time, MBA after CLKA↑; MBB after CLKB↑	1	–	1	–	ns
t _{PGH}	Hold Time, $\overline{ODD/EVEN}$ and PGA after CLKA↑; $\overline{ODD/EVEN}$ and PGB after CLKB↑ ⁽²⁾	1	–	1	–	ns
t _{RSTH}	Hold Time, \overline{RST} LOW after CLKA↑ or CLKB↑ ⁽³⁾	5	–	6	–	ns
t _{FSH}	Hold Time, FS0 and FS1 after \overline{RST} HIGH	4	–	4	–	ns
t _{SKEW1} ⁽⁴⁾	Skew Time, between CLKA↑ and CLKB↑ for \overline{EFA} , \overline{EFB} , \overline{FFA} , and \overline{FFB}	8	–	8	–	ns
t _{SKEW2} ⁽⁴⁾	Skew Time, between CLKA↑ and CLKB↑ For \overline{AEA} , \overline{AEB} , \overline{AFA} , and \overline{AFB}	14	–	16	–	ns

NOTES:

1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Only applies for a clock edge that does a FIFO read.
3. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
4. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, CL = 30PF

(Commercial: VCC = 5.0V ±10%, TA = 0°C to +70°C; Industrial; VCC = 5.0V ± 10%, TA = 40°C to +85°C)

Symbol	Parameter	Commercial		Com'l & Ind'l ⁽¹⁾		Unit
		IDT723612L15		IDT723612L20		
		Min.	Max.	Min.	Max.	
tA	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B35	2	10	2	12	ns
tWFF	Propagation Delay Time, CLKA↑ to \overline{FFA} and CLKB↑ to \overline{FFB}	2	10	2	12	ns
tREF	Propagation Delay Time, CLKA↑ to \overline{EFA} and CLKB↑ to \overline{EFB}	2	10	2	12	ns
tPAE	Propagation Delay Time, CLKA↑ to \overline{AEA} and CLKB↑ to \overline{AEB}	2	10	2	12	ns
tPAF	Propagation Delay Time, CLKA↑ to \overline{AFA} and CLKB↑ to \overline{AFB}	2	10	2	12	ns
tPMF	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH and CLKB↑ to $\overline{MBF2}$ LOW or $\overline{MBF1}$ HIGH	1	9	1	12	ns
tPMR	Propagation Delay Time, CLKA↑ to B0-B35 ⁽²⁾ and CLKB↑ to A0-A35 ⁽³⁾	3	11	3	13	ns
tMDV	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B35 valid	1	11	1	11.5	ns
tDPDE	Propagation Delay Time, A0-A35 valid to \overline{PEFA} valid; B0-B35 valid to \overline{PEFB} valid	3	10	3	11	ns
tPOPE	Propagation Delay Time, ODD/ \overline{EVEN} to \overline{PEFA} and \overline{PEFB}	3	11	3	12	ns
tPOPB ⁽⁴⁾	Propagation Delay Time, ODD/ \overline{EVEN} to parity bits (A8, A17, A26, A35) and (B8, B17, B26, B35)	2	11	2	12	ns
tPEPE	Propagation Delay Time, $\overline{W/RA}$, \overline{CSA} , \overline{ENA} , MBA or PGA to \overline{PEFA} ; $\overline{W/RB}$, \overline{CSB} , ENB, MBB, PGB to \overline{PEFB}	1	11	1	12	ns
tPEPB ⁽⁴⁾	Propagation Delay Time, $\overline{W/RA}$, \overline{CSA} , ENA, MBA or PGA to parity bits (A8, A17, A26, A35); $\overline{W/RB}$, \overline{CSB} , bits (B8, B17, B26, B35) ENB, MBB or PGB to parity	3	12	3	13	ns
tRSF	Propagation Delay Time, \overline{RST} to (\overline{AEA} , \overline{AEB}) LOW and (\overline{AFA} , \overline{AFB} , $\overline{MBF1}$, $\overline{MBF2}$) HIGH	1	15	1	20	ns
tEN	Enable Time, \overline{CSA} and $\overline{W/RA}$ LOW to A0-A35 active and \overline{CSB} LOW and $\overline{W/RB}$ HIGH to B0-B35 active	2	10	2	12	ns
tDIS	Disable Time, \overline{CSA} or $\overline{W/RA}$ HIGH to A0-A35 at high impedance and \overline{CSB} HIGH or $\overline{W/RB}$ LOW to B0-B35 at high impedance.	1	8	1	9	ns

NOTES:

1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Writing data to the mail1 register when the B0-B35 outputs are active and MBB is HIGH.
3. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.
4. Only applies when reading data from a mail register.

SIGNAL DESCRIPTIONS

RESET

The IDT723612 is reset by taking the Reset (\overline{RST}) input LOW for at least four port-A clock (CLKA) and four port-B Clock (CLKB) LOW-to-HIGH transitions. The Reset input can switch asynchronously to the clocks. A device reset initializes the internal read and write pointers of each FIFO and forces the Full Flags (\overline{FFA} , \overline{FFB}) LOW, the Empty Flags (\overline{EFA} , \overline{EFB}) LOW, the Almost-Empty flags (\overline{AEA} , \overline{AEB}) LOW and the Almost-Full flags (\overline{AFA} , \overline{AFB}) HIGH. A reset also forces the Mailbox Flags ($\overline{MBF1}$, $\overline{MBF2}$) HIGH. After a reset, \overline{FFA} is set HIGH after two LOW-to-HIGH transitions of CLKA and \overline{FFB} is set HIGH after two LOW-to-HIGH transitions of CLKB. The device must be reset after power up before data is written to its memory.

TABLE 1 — FLAG PROGRAMMING

FS1	FS0	\overline{RST}	ALMOST-FULL AND ALMOST-EMPTY FLAG OFFSET REGISTER (X)
H	H	↑	16
H	L	↑	12
L	H	↑	8
L	L	↑	4

A LOW-to-HIGH transition on the \overline{RST} input loads the Almost-Full and Almost-Empty registers (X) with the values selected by the Flag Select (FS0, FS1) inputs. The values that can be loaded into the registers are shown in Table 1.

FIFO WRITE/READ OPERATION

The state of port-A data A0-A35 outputs is controlled by the port-A Chip Select (\overline{CSA}) and the port-A Write/Read select ($\overline{W/RA}$). The A0-A35 outputs are in the high-impedance state when either \overline{CSA} or $\overline{W/RA}$ is HIGH. The A0-A35 outputs are active when both \overline{CSA} and $\overline{W/RA}$ are LOW.

Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when \overline{CSA} is LOW, $\overline{W/RA}$ is HIGH, ENA is HIGH, MBA is LOW, and \overline{FFA} is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when \overline{CSA} is LOW, $\overline{W/RA}$ is LOW, ENA is HIGH, MBA is LOW, and \overline{EFA} is HIGH (see Table 2).

The port-B control signals are identical to those of port A. The state of the port-B data (B0-B35) outputs is controlled by the port-B Chip Select (\overline{CSB}) and the port-B Write/Read select ($\overline{W/RB}$). The B0-B35 outputs are in the high-impedance state when either \overline{CSB} or $\overline{W/RB}$ is HIGH. The B0-B35 outputs are active when both \overline{CSB} and $\overline{W/RB}$ are LOW.

Data is loaded into FIFO2 from the B0-B35 inputs on a LOW-to-HIGH transition of CLKB when \overline{CSB} is LOW, $\overline{W/RB}$ is HIGH, ENB is HIGH, MBB is LOW, and \overline{FFB} is HIGH. Data is read from FIFO1 to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when \overline{CSB} is LOW, $\overline{W/RB}$ is LOW, ENB is HIGH, MBB is LOW, and \overline{EFB} is HIGH (see Table 3).

TABLE 2 — PORT-A ENABLE FUNCTION TABLE

\overline{CSA}	$\overline{W/RA}$	ENA	MBA	CLKA	A0-A35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO1 Write
L	H	H	H	↑	In High-Impedance State	Mail1 Write
L	L	L	L	X	Active, FIFO2 Output Register	None
L	L	H	L	↑	Active, FIFO2 Output Register	FIFO2 Read
L	L	L	H	X	Active, Mail2 Register	None
L	L	H	H	↑	Active, Mail2 Register	Mail2 Read (Set $\overline{MBF2}$ HIGH)

TABLE 3 — PORT-B ENABLE FUNCTION TABLE

\overline{CSB}	$\overline{W/RB}$	ENB	MBB	CLKB	B0-B35 Outputs	Port Functions
H	X	X	X	X	In High-Impedance State	None
L	H	L	X	X	In High-Impedance State	None
L	H	H	L	↑	In High-Impedance State	FIFO2 Write
L	H	H	H	↑	In High-Impedance State	Mail2 Write
L	L	L	L	X	Active, FIFO1 Output Register	None
L	L	H	L	↑	Active, FIFO1 Output Register	FIFO1 read
L	L	L	H	X	Active, Mail1 Register	None
L	L	H	H	↑	Active, Mail1 Register	Mail1 Read (Set $\overline{MBF1}$ HIGH)

The setup and hold time constraints to the port clocks for the port Chip Selects (CSA, CSB) and Write/Read selects (W/RA, W/RB) are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port chip select and write/read select may change states during the setup and hold time window of the cycle.

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through two flip-flop stages. This is done to improve flag reliability by reducing the probability of metastable events on the output when CLKA and CLKB operate asynchronously to one another. EFA, AEA, FFA, and AFA are synchronized by CLKA. EFB, AEB, FFB, and AFB are synchronized to CLKB. Tables 4 and 5 show the relationship of each port flag to FIFO1 and FIFO2.

EMPTY FLAGS (EFA, EFB)

The Empty Flag of a FIFO is synchronized to the port clock that reads data from its array. When the Empty Flag is HIGH, new data can be read to the FIFO output register. When the Empty Flag is LOW, the FIFO is empty and attempted FIFO reads are ignored.

The read pointer of a FIFO is incremented each time a new word is clocked to the output register. The state machine that controls an Empty Flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO SRAM status is empty, empty+1, or empty+2. A word written to a FIFO can be read to the FIFO output register in a minimum of three cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The Empty Flag of the FIFO is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock, and the new data word can be read to the FIFO output register in the following cycle.

A LOW-to-HIGH transition on an Empty Flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

FULL FLAG (FFA, FFB)

The Full Flag of a FIFO is synchronized to the port clock that writes data to its array. When the Full Flag is HIGH, a memory location is free in the SRAM to receive new data. No memory locations are free when the Full Flag is LOW and attempted writes to the FIFO are ignored.

Each time a word is written to a FIFO, the write pointer is incremented. The state machine that controls a Full Flag monitors a write-pointer and read pointer comparator that indicates when the FIFO SRAM status is full, full-1, or full-2. From the time a word is read from a FIFO, the previous memory location is ready to be written in a minimum of three cycles of the Full Flag synchronizing clock. Therefore, a Full Flag is LOW if less than two cycles of the Full Flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full Flag synchronization clock after the read sets the Full Flag HIGH and the data can be written in the following clock cycle.

A LOW-to-HIGH transition on a Full Flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle.

ALMOST EMPTY FLAGS (AEA, AEB)

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an Almost-Empty flag monitors a write-pointer comparator that indicates when the FIFO SRAM status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see Reset above). An Almost-Empty flag is LOW when the FIFO contains X or less words in memory and is HIGH when the FIFO contains (X+1) or more words.

Two LOW-to-HIGH transitions of the Almost-Empty flag synchronizing clocks are required after a FIFO write for the Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing (X+1) or more words remains LOW if two cycles of the synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 7 and 8).

ALMOST FULL FLAGS (AFA, AFB)

The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write-pointer and read-pointer comparator that indicates when the FIFO

TABLE 4 — FIFO1 FLAG OPERATION

Number of Words in the FIFO1 ⁽¹⁾	Synchronized to CLKB		Synchronized to CLKA	
	EFB	AEB	AFA	FFA
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

NOTE:

1. X is the value in the Almost-Empty flag and Almost-Full flag offset register.

TABLE 5 — FIFO2 FLAG OPERATION

Number of Words in the FIFO1 ⁽¹⁾	Synchronized to CLKB		Synchronized to CLKA	
	EFA	AEA	AFB	FFB
0	L	L	H	H
1 to X	H	L	H	H
(X+1) to [64-(X+1)]	H	H	H	H
(64-X) to 63	H	H	L	H
64	H	H	L	L

SRAM status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the value of the Almost-Full and Almost-Empty Offset register (X). This register is loaded with one of four preset values during a device reset (see Reset above). An Almost-Full flag is LOW when the FIFO contains (64-X) or more words in memory and is HIGH when the FIFO contains [64-(X+1)] or less words.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for the Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing [64-(X+1)] or less words remains LOW if two cycles of the synchronizing clock have not elapsed since the read that reduced the number of words in memory to [64-(X+1)]. An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of the synchronizing clock after the FIFO read that reduces the number of words in memory to [64-(X+1)]. A second LOW-to-HIGH transition of an Almost-Full flag synchronizing clock begins the first synchronization cycle if it occurs at time tSKEW2 or greater after the read that reduces the number of words in memory to [64-(X+1)]. Otherwise, the subsequent synchronizing clock cycle can be the first synchronization cycle (see Figure 14 and 15).

MAILBOX REGISTERS

Each FIFO has a 36-bit bypass register to pass command and control information between port A and port B without putting it in queue. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. A LOW-to-HIGH transition on CLK_A writes A0-A35 data to the mail1 register when a port-A write is selected by \overline{CSA} , \overline{WRA} , and ENA and MBA HIGH. A LOW-to-HIGH transition on CLK_B writes B0-B35 data to the mail2 register when a port-B write is selected by \overline{CSB} , \overline{WRB} , and ENB and MBB is HIGH. Writing data to a mail register sets the corresponding flag (MBF1 or MBF2) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When a port's data outputs are active, the data on the bus comes from the FIFO output register when the port Mailbox-select input (MBA, MBB) is LOW and from the mail register when the port mailbox-select input is HIGH. The Mail1 register Flag (MBF1) is set HIGH by a LOW-to-HIGH transition on CLK_B when a port-B read is selected by \overline{CSB} , \overline{WRB} , and ENB and MBB is HIGH. The Mail2 register Flag (MBF2) is set HIGH by a LOW-to-HIGH transition on CLK_A when port-A read is selected by \overline{CSA} , \overline{WRA} , and ENA and MBA is HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register.

PARITY CHECKING

The port-A inputs (A0-A35) and port-B inputs (B0-B35) each have four parity trees to check the parity of incoming (or outgoing) data. A parity failure on one or more bytes of the input bus is reported by a LOW level on the port Parity Error Flag (PEFA, PEFB). Odd or even parity checking can be selected, and the Parity Error Fags can be ignored if this feature is not desired.

Parity status is checked on each input bus according to the level of the Odd/Even parity (ODD/EVEN) select input. A parity error on one or more bytes of a port is reported by a LOW level on the corresponding port Parity Error Flag

(\overline{PEFA} , \overline{PEFB}) output. Port-A bytes are arranged as A0-A8, A9-A17, A18-A26, and A27-A35 with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. When odd/even parity is selected, a port parity error flag (\overline{PEFA} , \overline{PEFB}) is LOW if any byte on the port has an odd/even number of LOW levels applied to the bits.

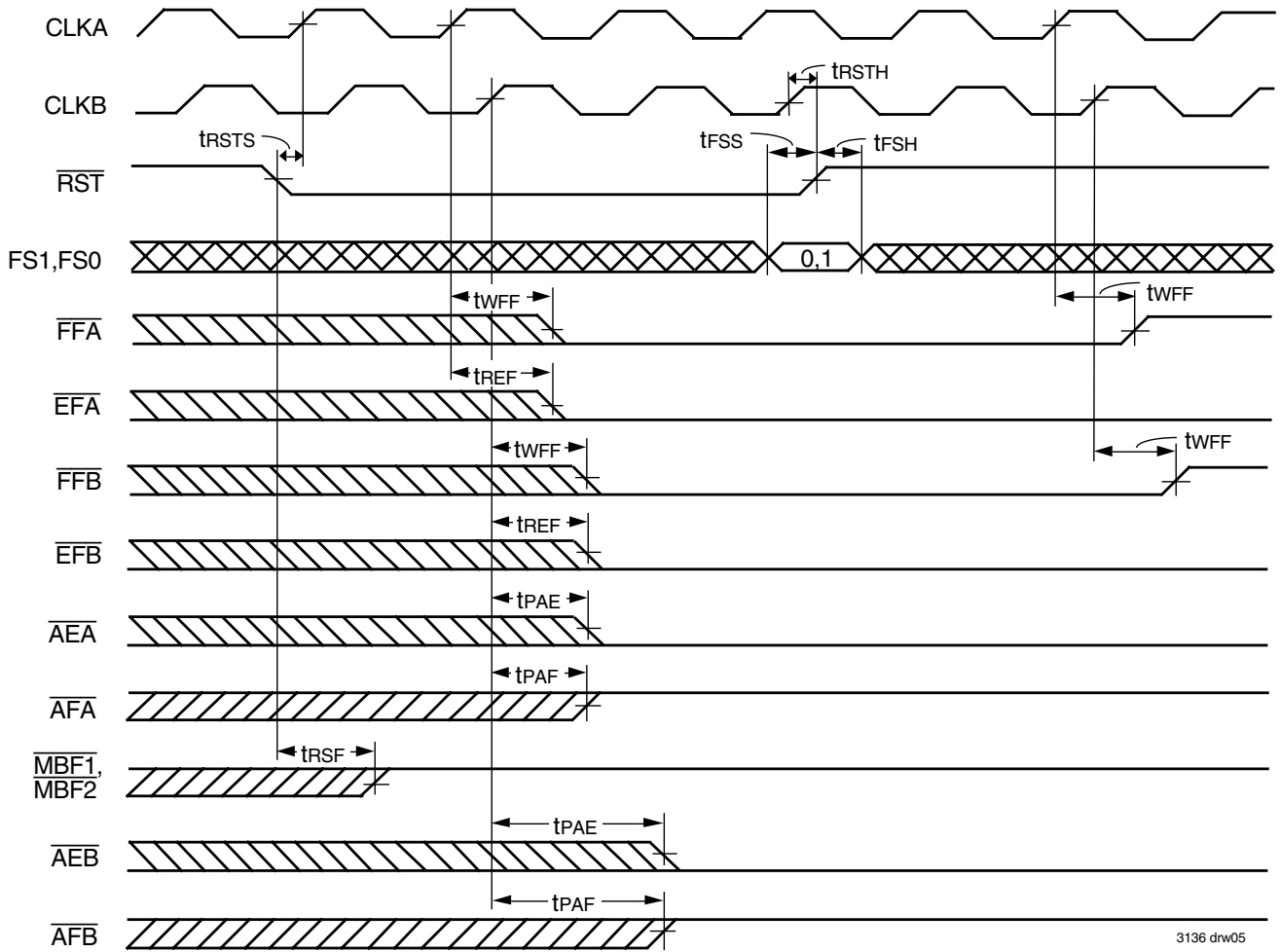
The four parity trees used to check the A0-A35 inputs are shared by the mail2 register when parity generation is selected for port-A reads (PGA = HIGH). When a port-A read from the mail2 register with parity generation is selected with \overline{WRA} LOW, \overline{CSA} LOW, ENA HIGH, MBA HIGH, and PGA HIGH, the port-A Parity Error Flag (\overline{PEFA}) is held HIGH regardless of the levels applied to the A0-A35 inputs. Likewise, the parity trees used to check the B0-B35 inputs are shared by the mail1 register when parity generation is selected for port-B reads (PGB = HIGH). When a port-B read from the mail1 register with parity generation is selected with \overline{WRB} LOW, \overline{CSB} LOW, ENB HIGH, MBB HIGH, and PGB HIGH, the port-B parity error flag (\overline{PEFB}) is held HIGH regardless of the levels applied to the B0-B35 inputs.

PARITY GENERATION

A HIGH level on the port-A Parity Generate select (PGA) or port-B Parity Generate select (PGB) enables the IDT723612 to generate parity bits for port reads from a FIFO or mailbox register. Port-A bytes are arranged as A0-A8, A9-A17, A18-26, and A27-A35, with the most significant bit of each byte used as the parity bit. Port-B bytes are arranged as B0-B8, B9-B17, B18-B26, and B27-B35, with the most significant bit of each byte used as the parity bit. A write to a FIFO or mail register stores the levels applied to all thirty-six inputs regardless of the state of the Parity Generate select (PGA, PGB) inputs. When data is read from a port with parity generation selected, the lower eight bits of each byte are used to generate a parity bit according to the level on the ODD/EVEN select. The generated parity bits are substituted for the levels originally written to the most significant bits of each byte as the word is read to the data outputs.

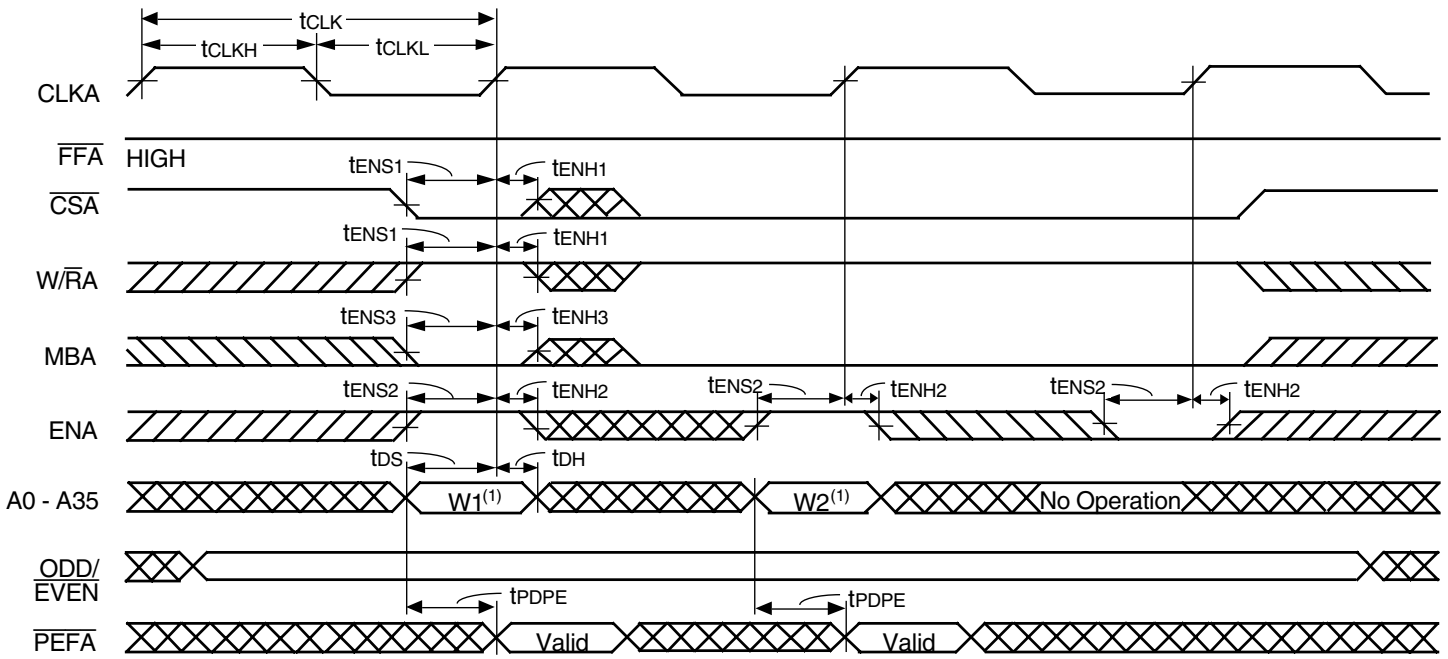
Parity bits for FIFO data are generated after the data is read from SRAM and before the data is written to the output register. Therefore, the port-A parity generate select (PGA) and Odd/Even parity select (ODD/EVEN) have setup and hold time constraints to the port-A Clock (CLK_A) and the port-B Parity Generate select (PGB) and ODD/EVEN have setup and hold-time constraints to the port-B Clock (CLK_B). These timing constraints only apply for a rising clock edge used to read a new word to the FIFO output register.

The circuit used to generate parity for the mail1 data is shared by the port-B bus (B0-B35) to check parity and the circuit used to generate parity for the mail2 data is shared by the port-A bus (A0-A35) to check parity. The shared parity trees of a port are used to generate parity bits for the data in a mail register when the port Write/Read select (\overline{WRA} , \overline{WRB}) input is LOW, the port mail select (MBA, MBB) input is HIGH, Chip Select (\overline{CSA} , \overline{CSB}) is LOW, Enable (ENA, ENB) is HIGH, and port Parity Generate select (PGA, PGB) is HIGH. Generating parity for mail register data does not change the contents of the register.



3136 drw05

Figure 2. Device Reset Loading the X Register with the Value of Eight

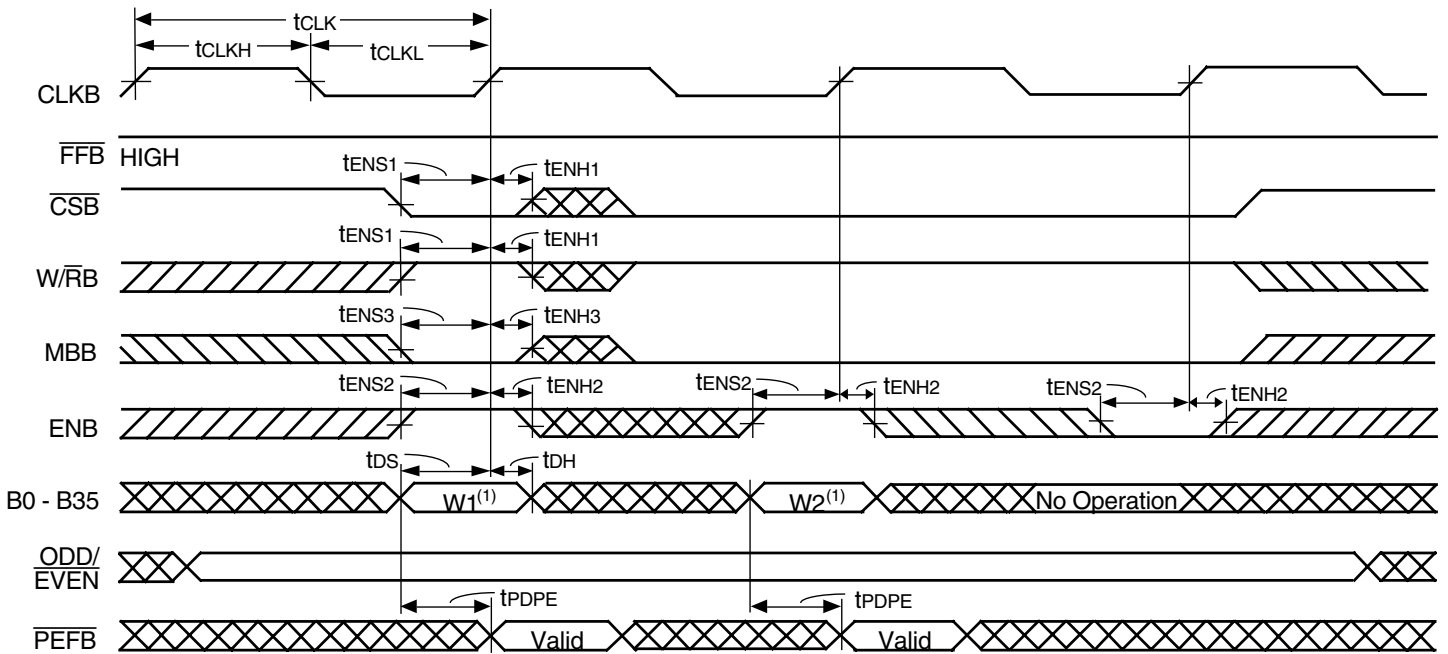


3136 drw06

NOTE:

1. Written to FIFO1.

Figure 3. Port-A Write Cycle Timing for FIFO1

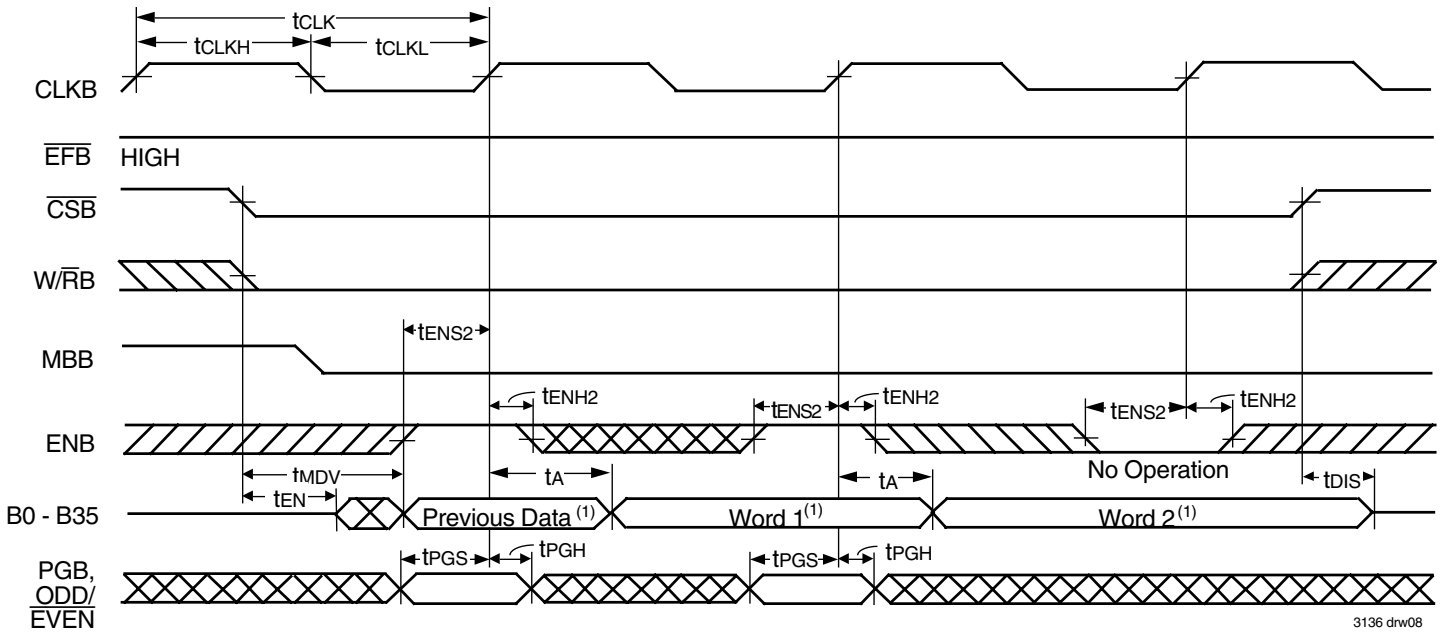


3136 drw07

NOTE:

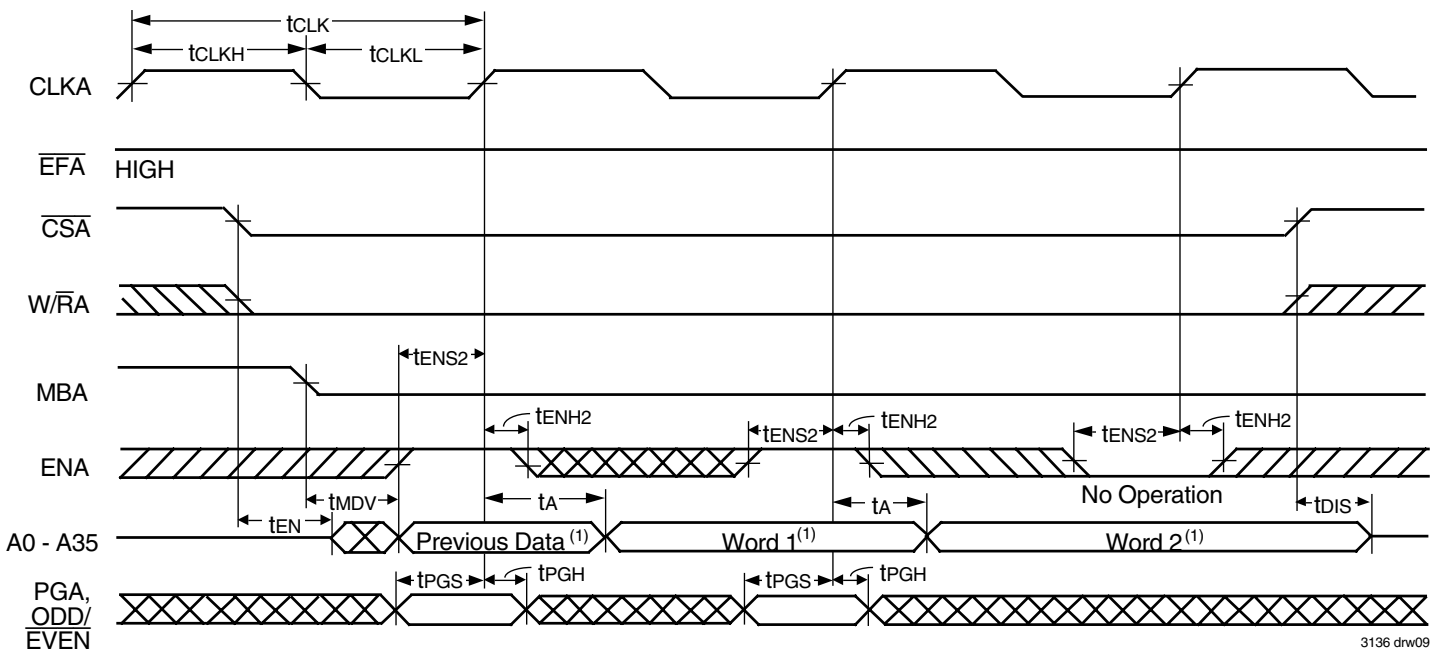
1. Written to FIFO2.

Figure 4. Port-B Write Cycle Timing for FIFO2



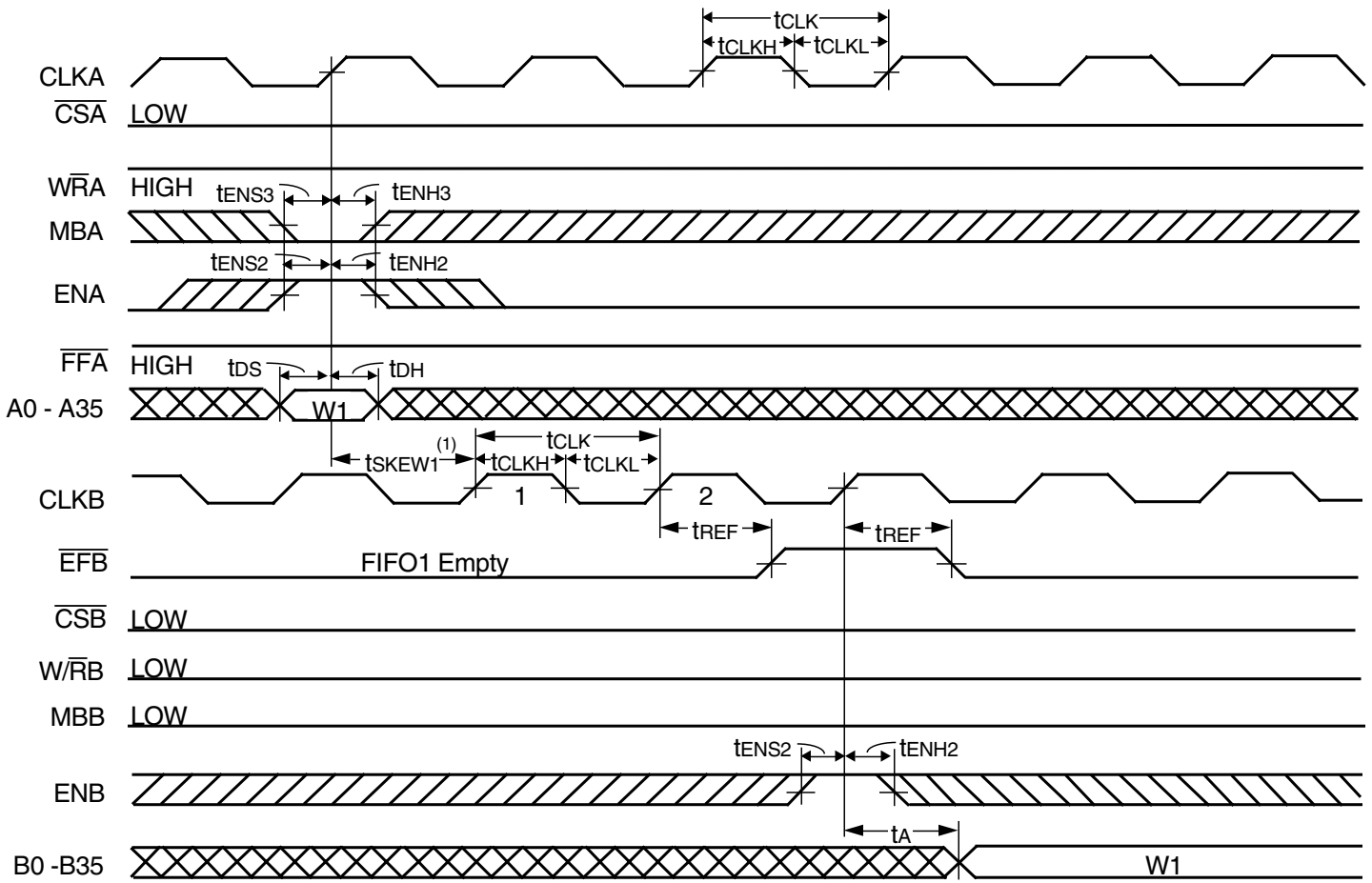
NOTE:
1. Read from FIFO1.

Figure 5. Port-B Read Cycle Timing for FIFO1



NOTE:
1. Read from FIFO2.

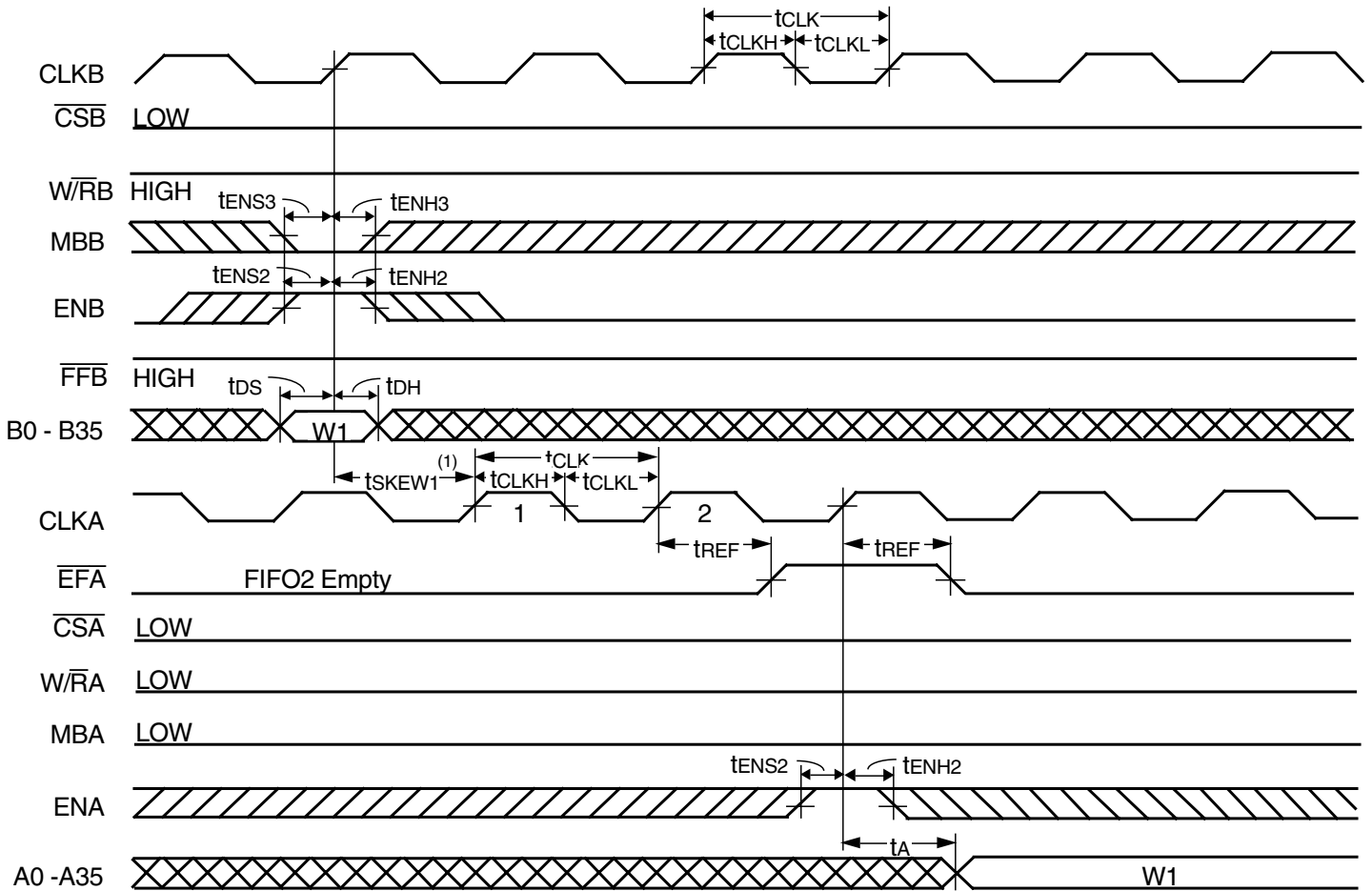
Figure 6. Port-A Read Cycle Timing for FIFO2



3136 drw10

NOTE:
1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for \overline{EFB} to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1} , then the transition of \overline{EFB} HIGH may occur one CLKB cycle later than shown.

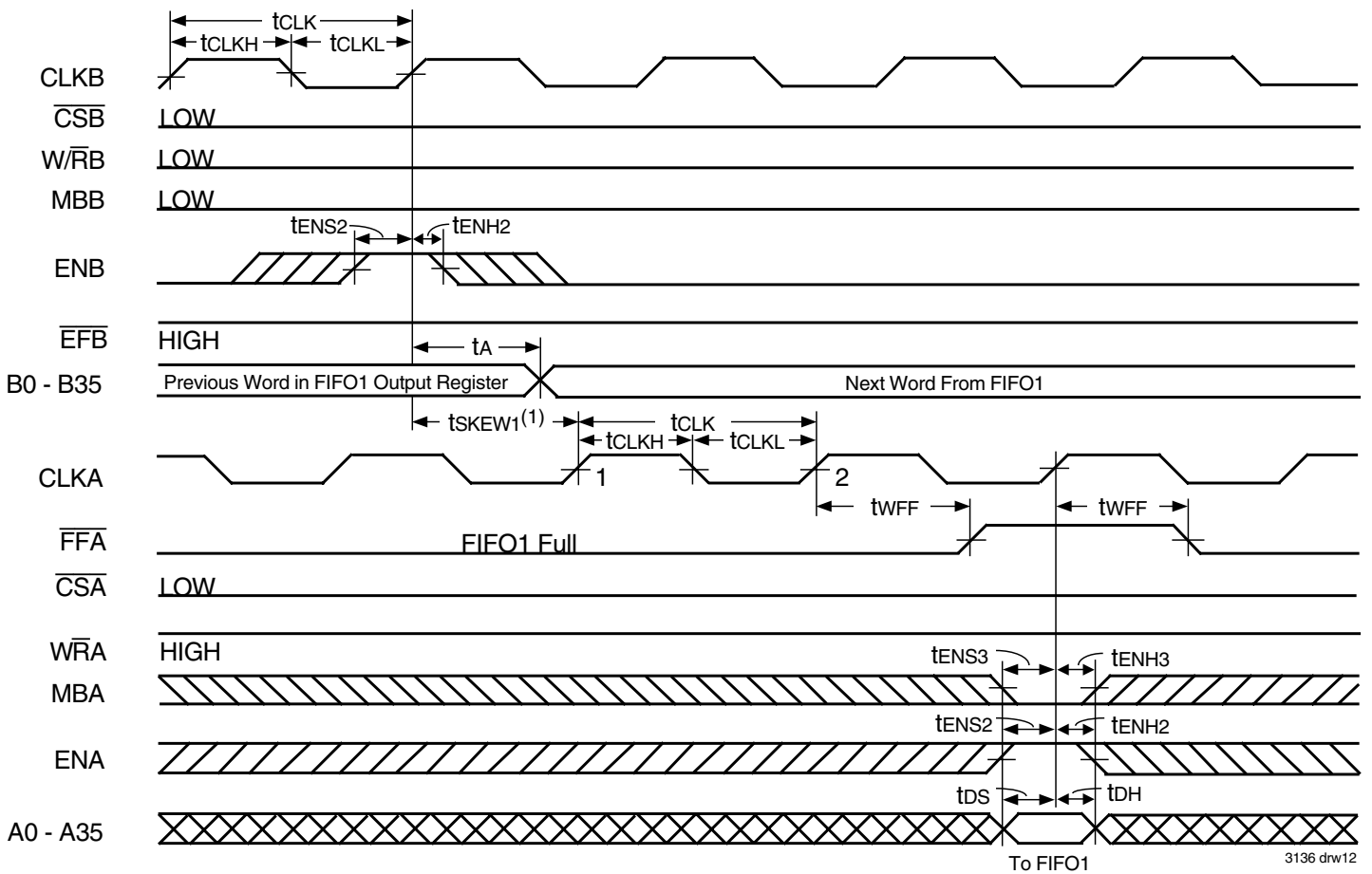
Figure 7. \overline{EFB} Flag Timing and First Data Read when FIFO1 is Empty



3136 drw11

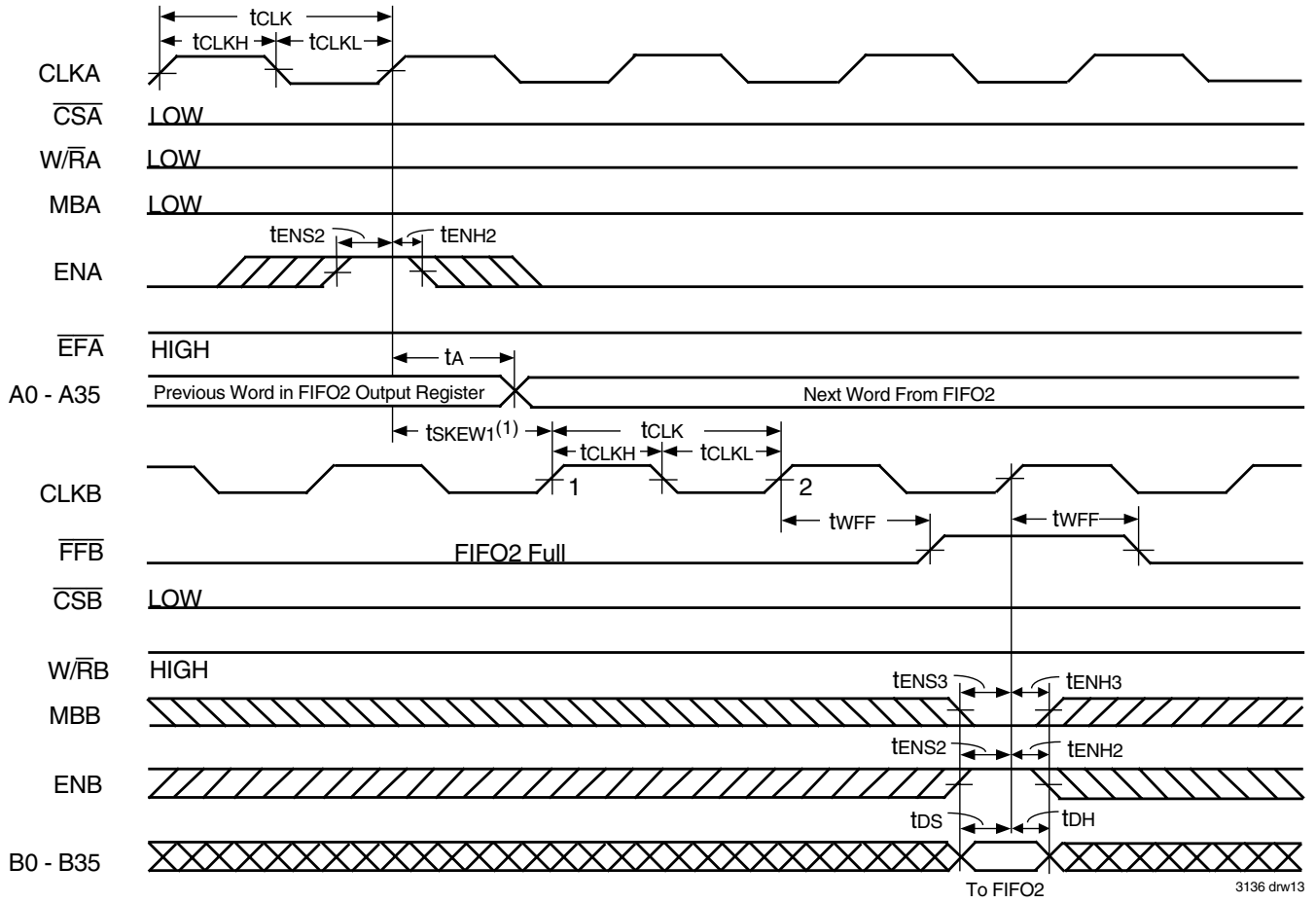
NOTE:
1. t_{SKWEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for \overline{EFA} to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKWEW1} , then the transition of \overline{EFA} HIGH may occur one CLKA cycle later than shown.

Figure 8. \overline{EFA} Flag Timing and First Data Read when FIFO2 is Empty



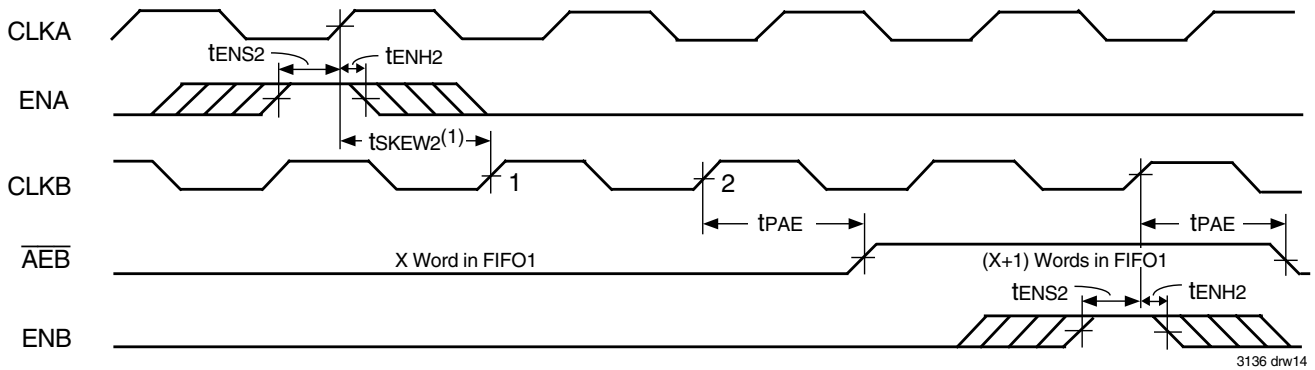
NOTE:
1. t_{SKEW1} is the minimum time between a rising $CLKB$ edge and a rising $CLKA$ edge for \overline{FFA} to transition HIGH in the next $CLKA$ cycle. If the time between the rising $CLKB$ edge and rising $CLKA$ edge is less than t_{SKEW1} , then \overline{FFA} may transition HIGH one $CLKA$ cycle later than shown.

Figure 9. \overline{FFA} Flag Timing and First Available Write when FIFO1 is Full



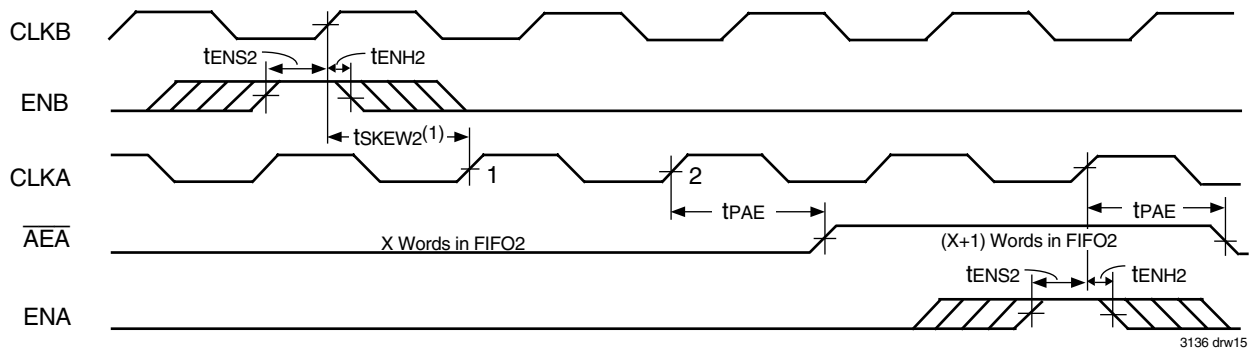
NOTE:
1. tsKEW1 is the minimum time between a rising CLKA edge and a rising CLKB edge for FFB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tsKEW1, then FFB may transition HIGH one CLKB cycle later than shown.

Figure 10. FFB Flag Timing and First Available Write when FIFO2 is Full



NOTES:
1. tsKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for AEB to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tsKEW2, then AEB may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write (CSA = LOW, W/RA = HIGH, MBA = LOW), FIFO1 read (CSB = LOW, W/RB = LOW, MBB = LOW).

Figure 11. Timing for AEB when FIFO1 is Almost Empty

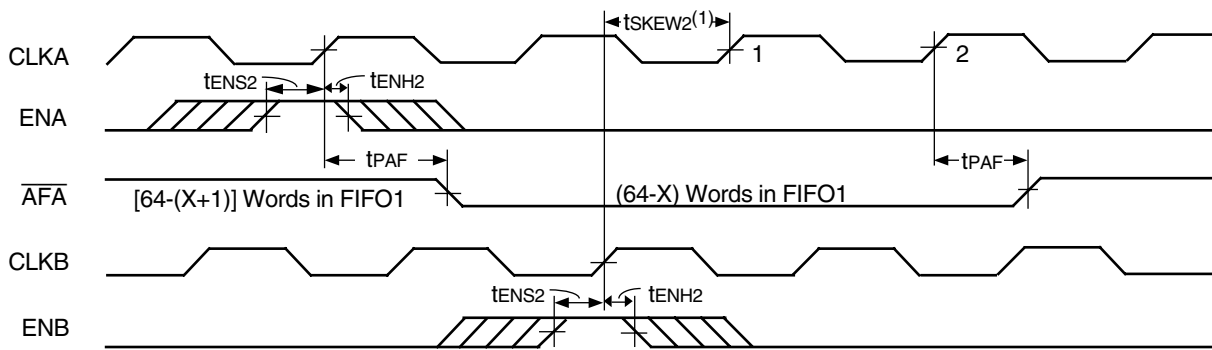


3136 drw15

NOTES:

1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for \overline{AEA} to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then \overline{AEA} may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB} = \text{LOW}$, $W/\overline{RB} = \text{HIGH}$, $MBB = \text{LOW}$), FIFO2 read ($\overline{CSA} = \text{LOW}$, $W/\overline{RA} = \text{LOW}$, $MBA = \text{LOW}$).

Figure 12. Timing for \overline{AEA} when FIFO2 is Almost Empty

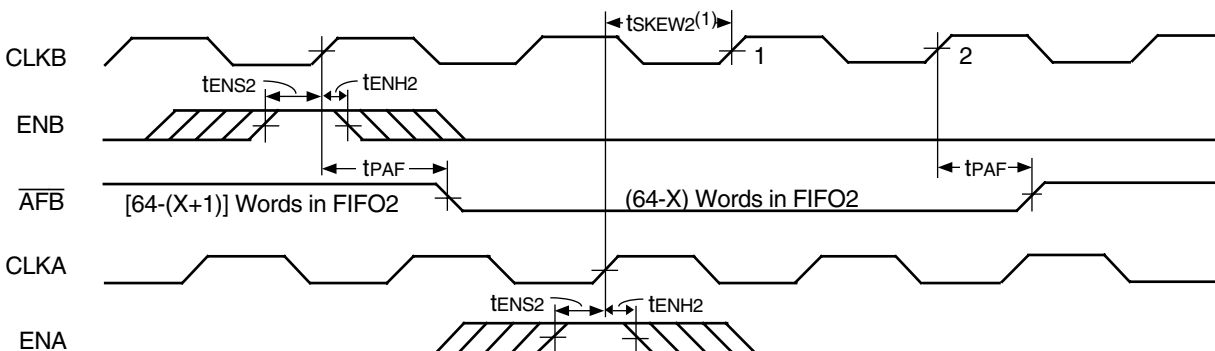


3136 drw16

NOTES:

1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for \overline{AFA} to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then \overline{AFA} may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA} = \text{LOW}$, $W/\overline{RA} = \text{HIGH}$, $MBA = \text{LOW}$), FIFO1 read ($\overline{CSB} = \text{LOW}$, $W/\overline{RB} = \text{LOW}$, $MBB = \text{LOW}$).

Figure 13. Timing for \overline{AFA} when FIFO1 is Almost Full

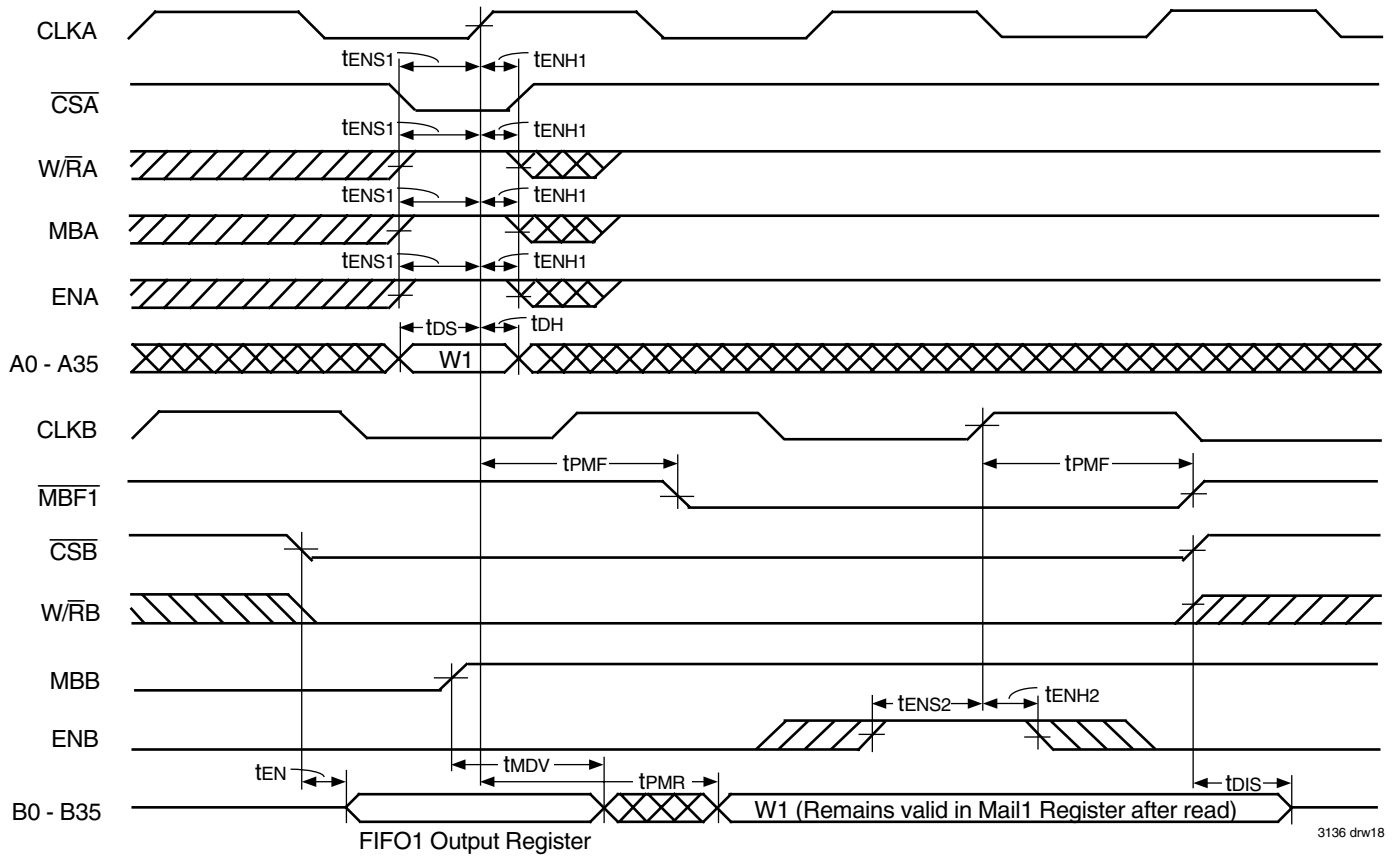


3136 drw17

NOTES:

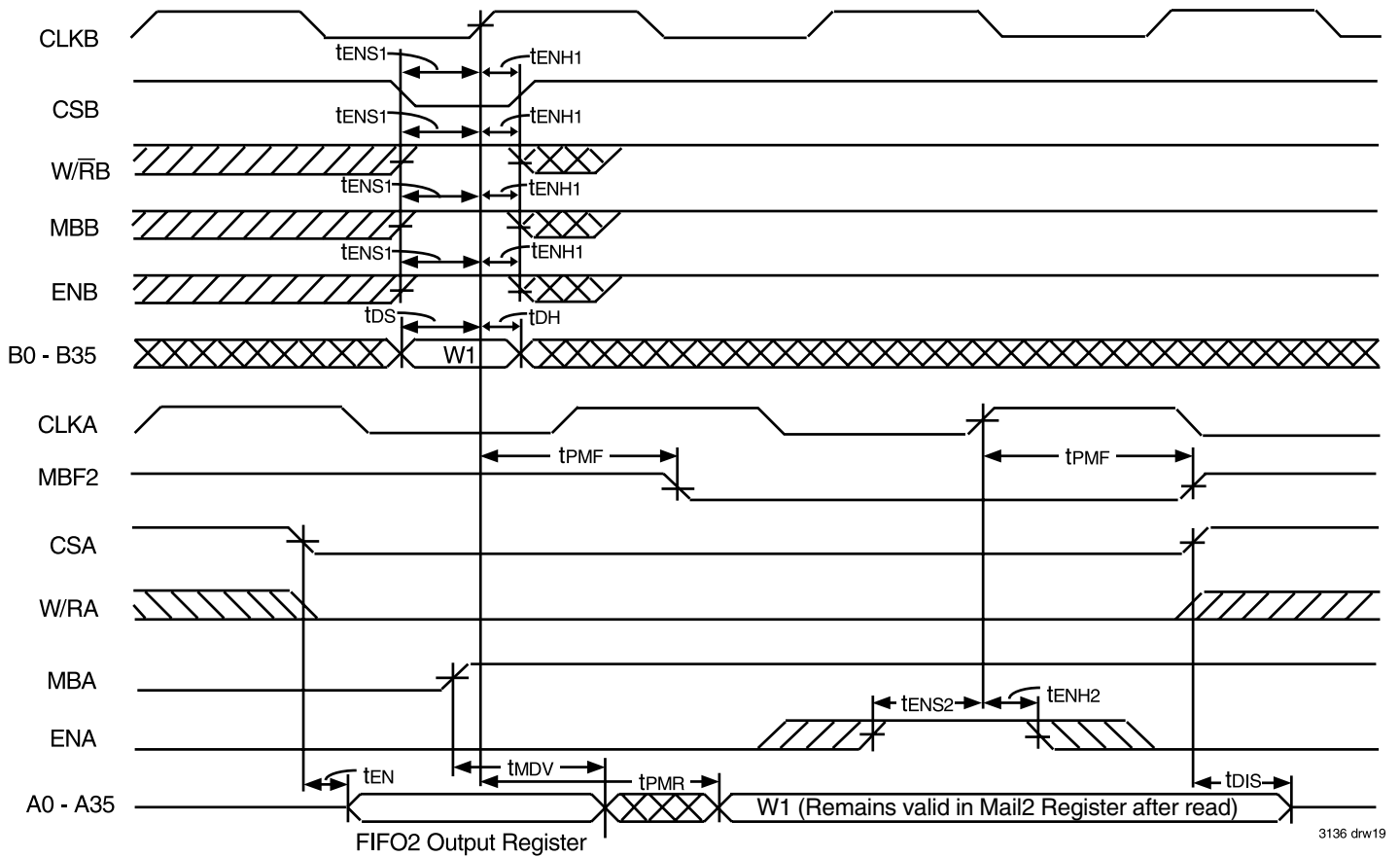
1. tSKEW2 is the minimum time between a rising CLKB edge and a rising CLKA edge for \overline{AFB} to transition HIGH in the next CLKB cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW2, then \overline{AFB} may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write ($\overline{CSB} = \text{LOW}$, $W/\overline{RB} = \text{HIGH}$, $MBB = \text{LOW}$), FIFO2 read ($\overline{CSA} = \text{LOW}$, $W/\overline{RA} = \text{LOW}$, $MBA = \text{LOW}$).

Figure 14. Timing for \overline{AFB} when FIFO2 is Almost Full



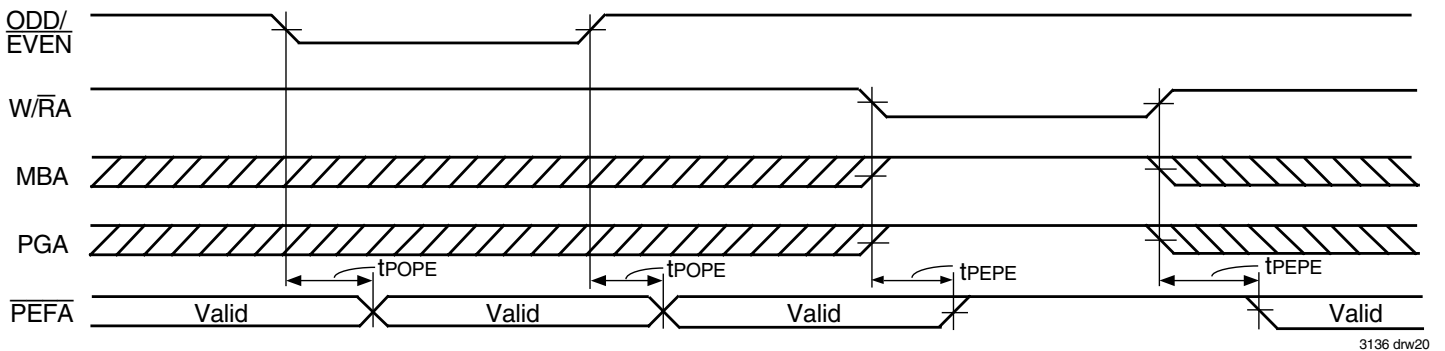
NOTE:
1. Port-B parity generation off (PGB = LOW).

Figure 15. Timing for Mail1 Register and **MBF1** Flag



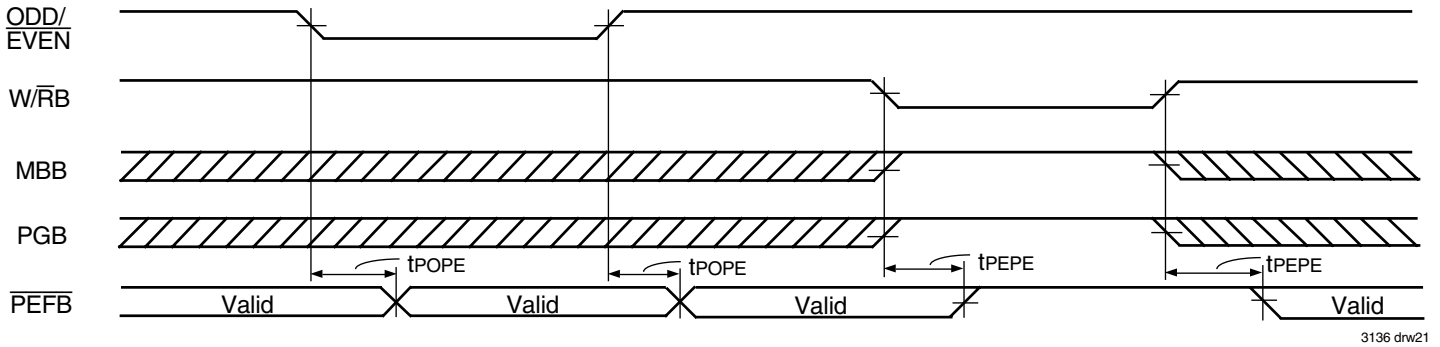
NOTE:
1. Port-A parity generation off (PGA = LOW).

Figure 16. Timing for Mail2 Register and $\overline{MBF2}$ Flag



NOTE:
1. ENA is HIGH, and \overline{CSA} is LOW.

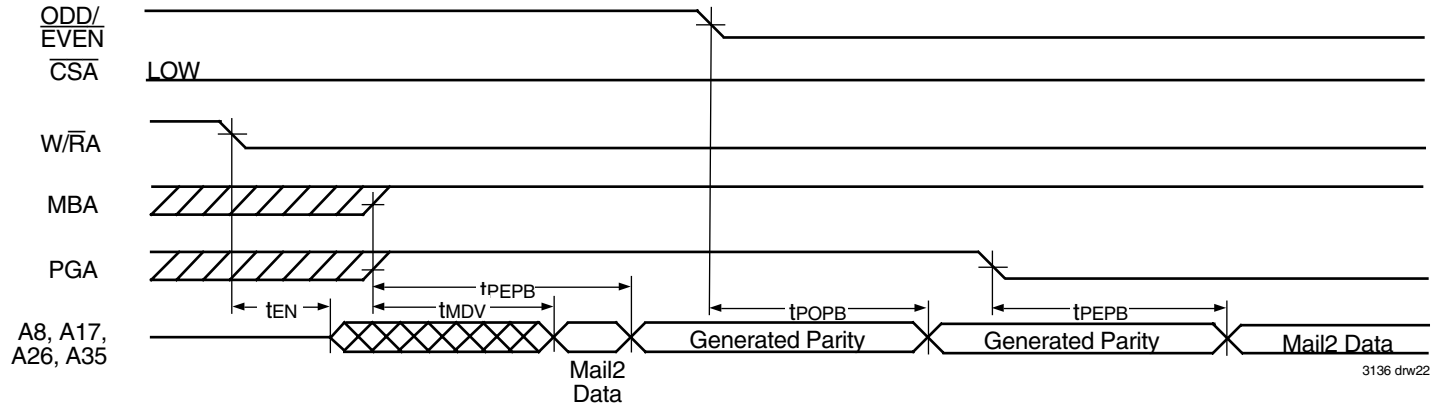
Figure 17. ODD/ \overline{EVEN} $\overline{W/RA}$, MBA, and PGA to \overline{PEFA} Timing



3136 drw21

NOTE:
1. ENB is HIGH, and CSB is LOW.

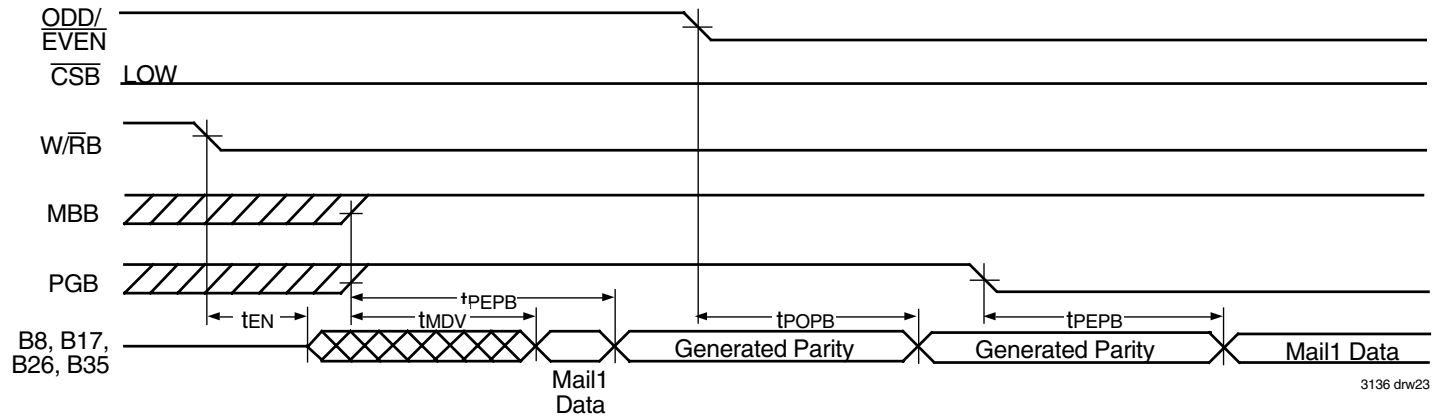
Figure 18. ODD/EVEN W/RB, MBB, and PGB to PEFB Timing



3136 drw22

NOTE:
1. ENA is HIGH.

Figure 19. Parity Generation Timing when Reading from Mail2 Register

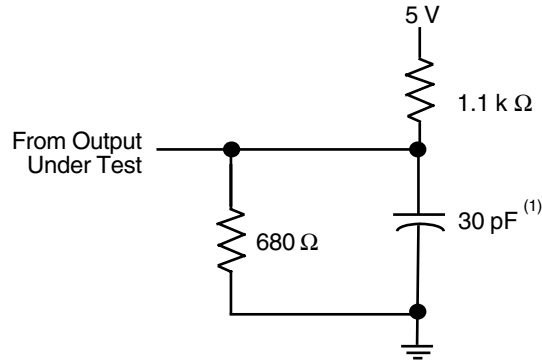


3136 drw23

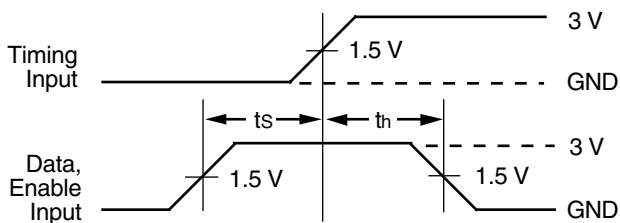
NOTE:
1. ENB is HIGH.

Figure 20. Parity Generation Timing when Reading from Mail1 Register

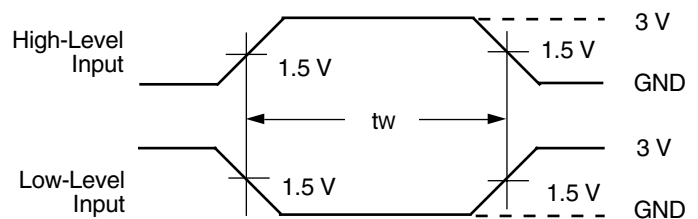
PARAMETER MEASUREMENT INFORMATION



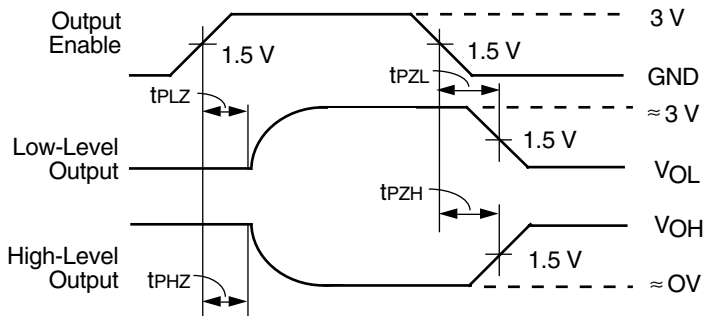
LOAD CIRCUIT



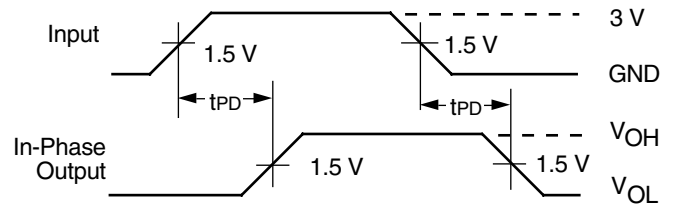
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**



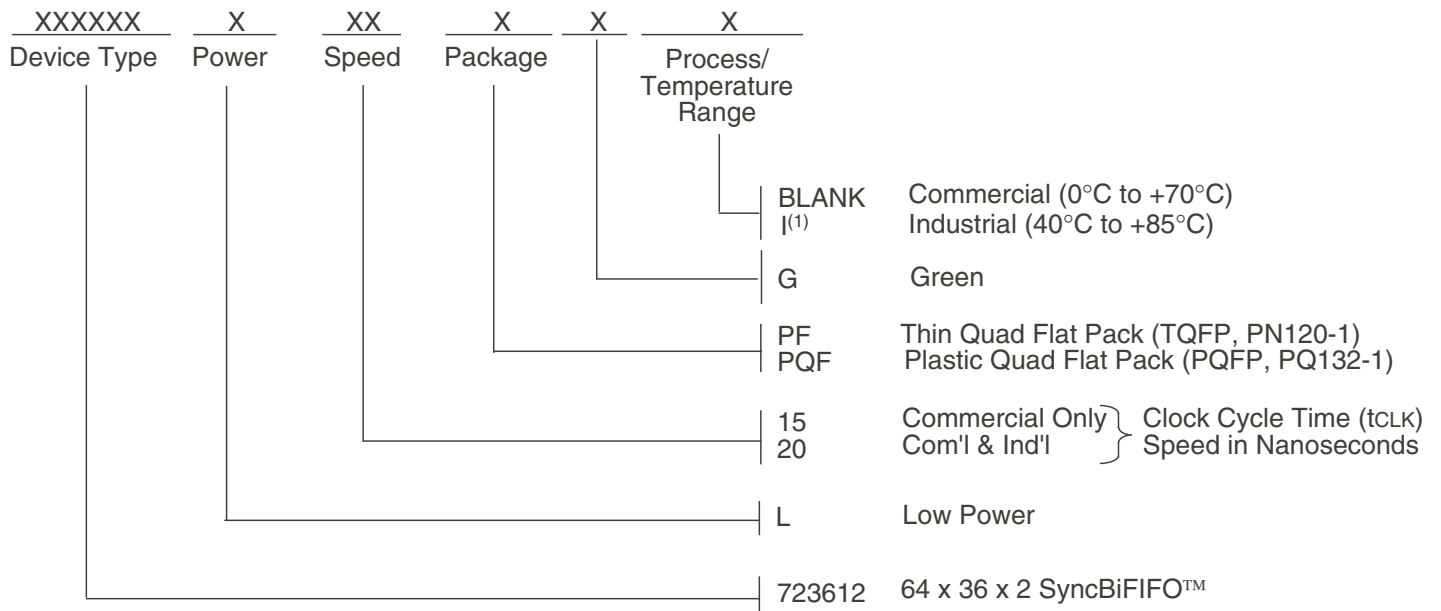
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

3136 drw24

NOTE:
1. Includes probe and jig capacitance.

Figure 21. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



3136 drw25

NOTES:

1. Industrial temperature range product for 20ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages contact your sales office.

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