CMOS TRIPLE BUS SyncFIFO™ WITH BUS-MATCHING 256 x 36 x 2, 512 x 36 x 2 1,024 x 36 x 2

IDT723626
IDT723636
IDT723646

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

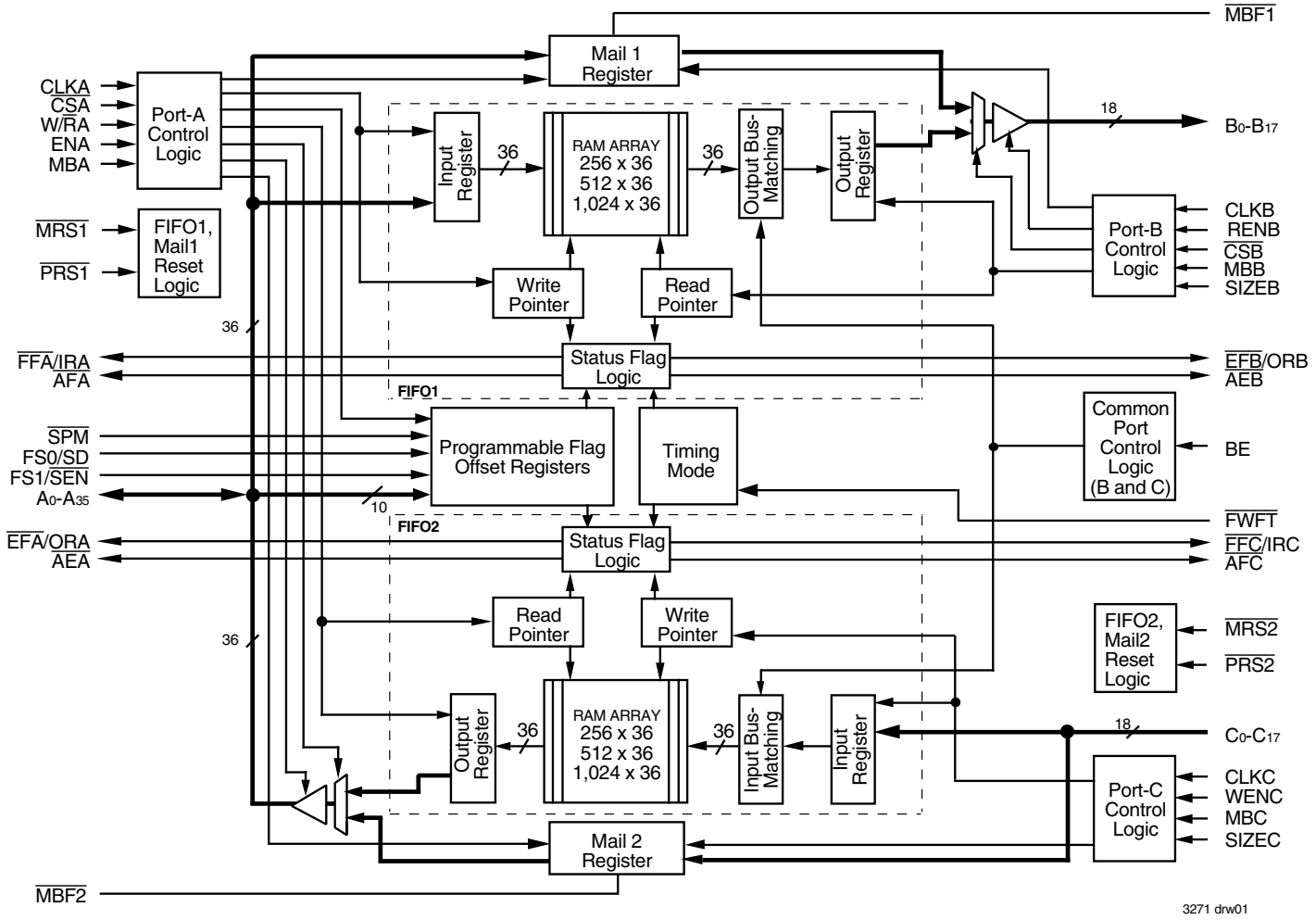
FEATURES:

- **Memory storage capacity:**
  - **IDT723626 – 256 x 36 x 2**
  - **IDT723636 – 512 x 36 x 2**
  - **IDT723646 – 1,024 x 36 x 2**
- **Clock frequencies up to 67 MHz (10ns access time)**
- **Two independent FIFOs buffer data between one bidirectional 36-bit port and two unidirectional 18-bit ports (Port C receives and Port B transmits)**
- **18-bit (word) and 9-bit (byte) bus sizing of 18 bits (word) on Ports B and C**
- **Select IDT Standard timing (using $\overline{EFA}$, $\overline{EFB}$, $\overline{FFA}$, and $\overline{FFC}$ flag functions) or First Word Fall Through Timing (using ORA, ORB, IRA, and IRC flag functions)**
- **Programmable Almost-Empty and Almost-Full flags; each has three default offsets (8, 16 and 64)**
- **Serial or parallel programming of partial flags**
- **Big- or Little-Endian format for word and byte bus sizes**
- **Master Reset clears data and configures FIFO, Partial Reset clears data but retains configuration settings**
- **Mailbox bypass registers for each FIFO**
- **Free-running CLKA, CLKB and CLKC may be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)**
- **Auto power down minimizes power dissipation**
- **Available in a space-saving 128-pin Thin Quad Flatpack (TQFP)**
- **Green parts available, see ordering information**

DESCRIPTION:

The IDT723626/723636/723646 is a monolithic, high-speed, low-power, CMOS Triple Bus synchronous (clocked) FIFO memory which supports clock frequencies up to 67 MHz and has read access times as fast as 10 ns. Two

FUNCTIONAL BLOCK DIAGRAM

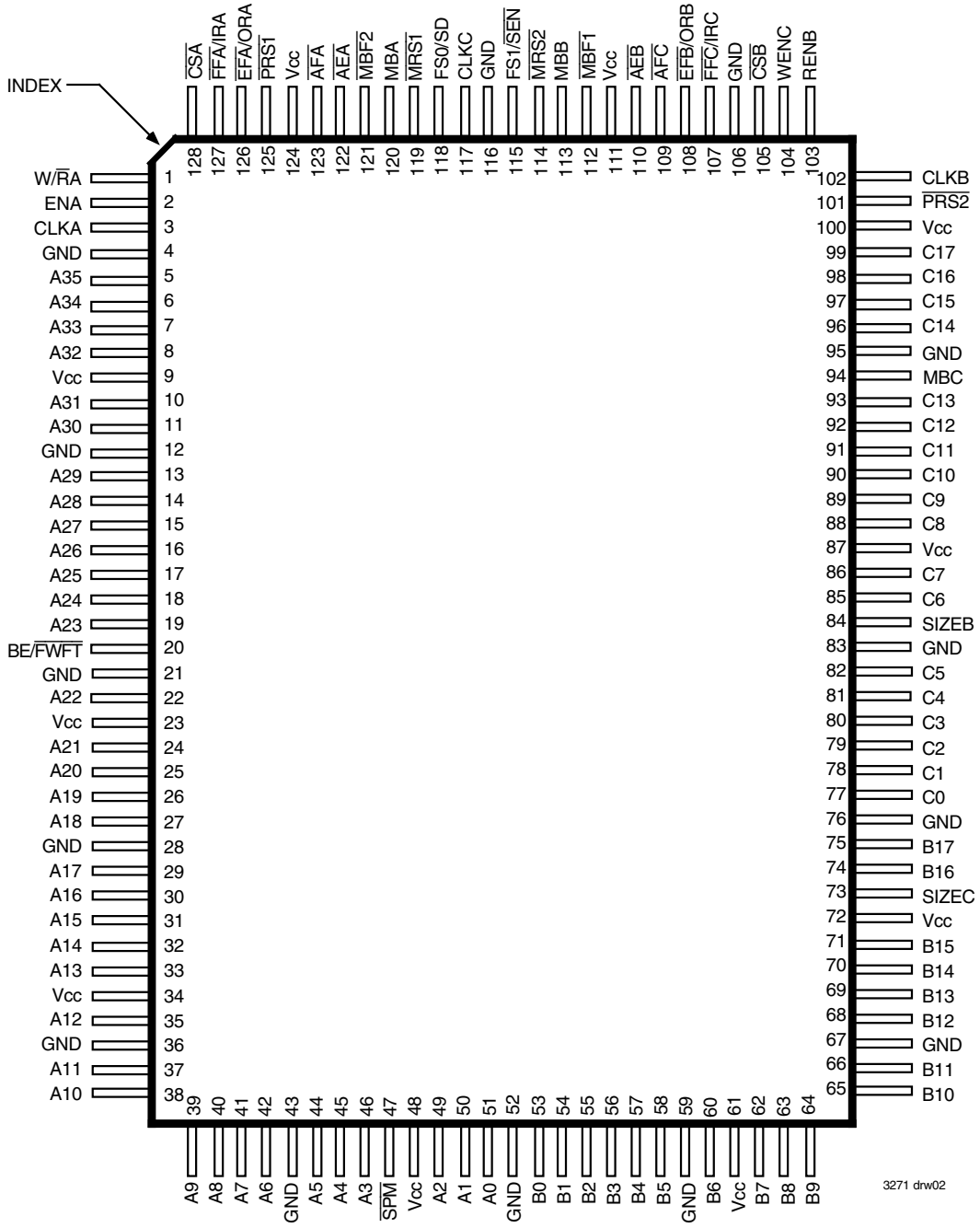


DESCRIPTION (CONTINUED)

independent 256/512/1,024 x 36 dual-port SRAM FIFOs on board each chip buffer data between a bidirectional 36-bit bus (Port A) and two unidirectional 18-bit buses (Port B transmits data, Port C receives data.) FIFO data can be read out of Port B and written into Port C using either 18-bit or 9-bit formats with a choice of Big- or Little-Endian configurations.

These devices are a synchronous (clocked) FIFO, meaning each port employs a synchronous interface. All data transfers through a port are gated to the LOW-to-HIGH transition of a port clock by enable signals. The clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple

PIN CONFIGURATION



TQFP (PK128-1, order code: PF)
TOP VIEW

bidirectional interface between microprocessors and/or buses with synchronous control.

Communication between each port may bypass the FIFOs via two mailbox registers. The mailbox registers' width matches the selected bus width of ports B and C. Each mailbox register has a flag ($\overline{MBF1}$ and $\overline{MBF2}$) to signal when new mail has been stored.

Two kinds of reset are available on these FIFOs: Master Reset and Partial Reset. Master Reset initializes the read and write pointers to the first location of the memory array and selects serial flag programming, parallel flag programming, or one of three possible default flag offset settings, 8, 16 or 64. Each FIFO has its own, independent Master Reset pin, $\overline{MRS1}$ and $\overline{MRS2}$.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Master Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings. Each FIFO has its own, independent Partial Reset pin, $\overline{PRS1}$ and $\overline{PRS2}$.

These devices have two modes of operation: In the *IDT Standard mode*, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the *First Word Fall Through mode* (FWFT), the first word written to an empty FIFO appears automatically on the outputs, no read operation required (Nevertheless, accessing subsequent words does necessitate a formal read request). The state of the BE/$\overline{FWFT}$ pin during Master Reset determines the mode in use.

Each FIFO has a combined Empty/Output Ready Flag ($\overline{EFA}$/ORA and $\overline{EFB}$/ORB) and a combined Full/Input Ready Flag ($\overline{FFA}$/IRA and $\overline{FFC}$/IRC). The $\overline{EF}$ and $\overline{FF}$ functions are selected in the IDT Standard mode. $\overline{EF}$ indicates whether or not the FIFO memory is empty. $\overline{FF}$ shows whether the memory is full or not. The IR and OR functions are selected in the First Word Fall Through mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

Each FIFO has a programmable Almost-Empty flag ($\overline{AEA}$ and $\overline{AEB}$) and a programmable Almost-Full flag ($\overline{AFA}$ and $\overline{AFC}$). $\overline{AEA}$ and $\overline{AEB}$ indicate when a selected number of words remain in the FIFO memory. $\overline{AFA}$ and $\overline{AFC}$ indicate when the FIFO contains more than a selected number of words.

$\overline{FFA}$/IRA, $\overline{FFC}$/IRC, $\overline{AFA}$ and $\overline{AFC}$ are two-stage synchronized to the Port Clock that writes data into its array. $\overline{EFA}$/ORA, $\overline{EFB}$/ORB, $\overline{AEA}$, and $\overline{AEB}$ are two-stage synchronized to the Port Clock that reads data from its array. Programmable offsets for $\overline{AEA}$, $\overline{AEB}$, $\overline{AFA}$, $\overline{AFC}$ are loaded in parallel using Port A or in serial via the SD input. The Serial Programming Mode pin ($\overline{SPM}$) makes this selection. Three default offset settings are also provided. The $\overline{AEA}$ and $\overline{AEB}$ threshold can be set at 8, 16 or 64 locations from the empty boundary and the $\overline{AFA}$ and $\overline{AFC}$ threshold can be set at 8, 16 or 64 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Master Reset.

Two or more FIFOs may be used in parallel to create wider data paths. Such a width expansion requires no additional, external components. Furthermore, two IDT723626/723636/723646 FIFOs can be combined with unidirectional FIFOs capable of First Word Fall Through timing (i.e. the SuperSync FIFO family) to form a depth expansion.

If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the power down state, supply current consumption (I_{CC}) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the power down state.

The IDT723626/723636/723646s are characterized for operation from 0°C to 70°C. They are fabricated using high speed, submicron CMOS technology.

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
A0-A35	Port A Data	I/O	36-bit bidirectional data port for side A.
$\overline{AEA}$	Port A Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKA. It is LOW when the number of words in FIFO2 is less than or equal to the value in the Almost-Empty A Offset register, X2.
$\overline{AEB}$	Port B Almost-Empty Flag	O	Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in FIFO1 is less than or equal to the value in the Almost-Empty B Offset register, X1.
$\overline{AFA}$	Port A Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in FIFO1 is less than or equal to the value in the Almost-Full A Offset register, Y1.
$\overline{AFC}$	Port C Almost-Full Flag	O	Programmable Almost-Full flag synchronized to CLKC. It is LOW when the number of empty locations in FIFO2 is less than or equal to the value in the Almost-Full C Offset register, Y2.
B0-B17	Port B Data	O	18-bit output data port for side B.
BE/$\overline{FWFT}$	Big-Endian/ First Word Fall Through Select	I	This is a dual purpose pin. During Master Reset, a HIGH on BE will select Big-Endian operation. In this case, depending on the bus size, the *most* significant byte or word on Port A is read from Port B first (A-to-B data flow) or is written to Port C first (C-to-A data flow). A LOW on BE will select Little-Endian operation. In this case, the *least* significant byte or word on Port A is read from Port B first (A-to-B data flow) or is written to Port C first (C-to-A data flow). After Master Reset, this pin selects the timing mode. A HIGH on $\overline{FWFT}$ selects IDT Standard mode, a LOW selects First Word Fall Through mode. Once the timing mode has been selected, the level on $\overline{FWFT}$ must be static throughout device operation.
C0-C17	Port C Data	I	18-bit input data port for side C.
CLKA	Port A Clock	I	CLKA is a continuous clock that synchronizes all data transfers through Port A and can be asynchronous or coincident to CLKB. $\overline{FFA}$/IRA, $\overline{EFA}$/ORA, $\overline{AFA}$, and $\overline{AEA}$ are all synchronized to the LOW-to-HIGH transition of CLKA.
CLKB	Port B Clock	I	CLKB is a continuous clock that synchronizes all data transfers through Port B and can be asynchronous or coincident to CLKA. $\overline{EFB}$/ORB and $\overline{AEB}$ are synchronized to the LOW-to-HIGH transition of CLKB.
CLKC	Port C Clock	I	CLKC is a continuous clock that synchronizes all data transfers through Port C and can be asynchronous or coincident to CLKA. $\overline{FFC}$/IRC and $\overline{AFC}$ are synchronized to the LOW-to-HIGH transition of CLKC.
$\overline{CSA}$	Port A Chip Select	I	$\overline{CSA}$ must be LOW to enable to LOW-to-HIGH transition of CLKA to read or write on Port A. The A0-A35 outputs are in the high-impedance state when $\overline{CSA}$ is HIGH.
$\overline{CSB}$	Port B Chip Select	I	$\overline{CSB}$ must be LOW to enable a LOW-to-HIGH transition of CLKB to read data on Port B. The B0-B17 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH.
$\overline{EFA}$/ORA	Port A Empty/ Output Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{EFA}$ function is selected. $\overline{EFA}$ indicates whether or not the FIFO2 memory is empty. In the FWFT mode, the ORA function is selected. ORA indicates the presence of valid data on the A0-A35 outputs, available for reading. $\overline{EFA}$/ORA is synchronized to the LOW-to-HIGH transition of CLKA.
$\overline{EFB}$/ORB	Port B Empty/ Output Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{EFB}$ function is selected. $\overline{EFB}$ indicates whether or not the FIFO1 memory is empty. In the FWFT mode, the ORB function is selected. ORB indicates the presence of valid data on the B0-B17 outputs, available for reading. $\overline{EFB}$/ORB is synchronized to the LOW-to-HIGH transition of CLKB.
ENA	Port A Enable	I	ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on Port A.
$\overline{FFA}$/IRA	Port A Full/ Input Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{FFA}$ function is selected. $\overline{FFA}$ indicates whether or not the FIFO1 memory is full. In the FWFT mode, the IRA function is selected. IRA indicates whether or not there is space available for writing to the FIFO1 memory. $\overline{FFA}$/IRA is synchronized to the LOW-to-HIGH transition of CLKA.
$\overline{FFC}$/IRC	Port C Full/ Input Ready Flag	O	This is a dual function pin. In the IDT Standard mode, the $\overline{FFC}$ function is selected. $\overline{FFC}$ indicates whether or not the FIFO2 memory is full. In the FWFT mode, the IRC function is selected. IRC indicates whether or not there is space available for writing to the FIFO2 memory. $\overline{FFC}$/IRC is synchronized to the LOW-to-HIGH transition of CLKC.

PIN DESCRIPTIONS (CONTINUED)

Symbol	Name	I/O	Description
FS1/$\overline{SEN}$	Flag Offset Select 1/ Serial Enable,	I	FS1/$\overline{SEN}$ and FS0/SD are dual-purpose inputs used for flag Offset register programming. During Master Reset, FS1/$\overline{SEN}$ and FS0/SD, together with $\overline{SPM}$, select the flag offset programming method. Three Offset register programming methods are available: automatically load one of three preset values (8, 16, or 64), parallel load from Port A, and serial load.
FS0/SD	Flag Offset Select 0/ Serial Data	I	When serial load is selected for flag Offset register programming, FS1/$\overline{SEN}$ is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/$\overline{SEN}$ is LOW, a rising edge on CLKA load the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the Offset registers is 32 for the IDT723626, 36 for the IDT723636, and 40 for the IDT723646. The first bit write stores the Y-register (Y1) MSB and the last bit write stores the X-register (X2) LSB.
MBA	Port A Mailbox Select	I	A HIGH level on MBA chooses a mailbox register for a Port A read or write operation. When the A0-A35 outputs are active, a HIGH level on MBA selects data from the mail2 register for output and a LOW level selects FIFO2 output-register data for output.
MBB	Port B Mailbox Select	I	A HIGH level on MBB chooses a mailbox register for a Port B read operation. When the B0-B17 outputs are active, a HIGH level on MBB selects data from the mail1 register for output and a LOW level selects FIFO1 output register data for output.
MBC	Port C Mailbox Select	I	A HIGH level on MBC chooses the mail2 register for a Port C write operation. This pin must be HIGH during Master Reset.
$\overline{MBF1}$	Mail1 Register Flag	O	$\overline{MBF1}$ is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while $\overline{MBF1}$ is LOW. $\overline{MBF1}$ is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B read is selected and MBB is HIGH. $\overline{MBF1}$ is set HIGH following either a Master or Partial Reset of FIFO1.
$\overline{MBF2}$	Mail2 Register Flag	O	$\overline{MBF2}$ is set LOW by a LOW-to-HIGH transition of CLKC that writes data to the mail2 register. Writes to the mail2 register are inhibited while $\overline{MBF2}$ is LOW. $\overline{MBF2}$ is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A read is selected and MBA is HIGH. $\overline{MBF2}$ is set HIGH following either a Master or Partial Reset of FIFO2.
$\overline{MRS1}$	Master Reset	I	A LOW on this pin initializes the FIFO1 read and write pointers to the first location of memory and sets the Port B output register to all zeroes. A LOW-to-HIGH transition on $\overline{MRS1}$ selects the programming method (serial or parallel) and one of three programmable flag default offsets for FIFO1 and FIFO2. It also configures ports B and C for bus size and endian arrangement. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while $\overline{MRS1}$ is LOW.
$\overline{MRS2}$	Master Reset	I	A LOW on this pin initializes the FIFO2 read and write pointers to the first location of memory and sets the Port A output register to all zeroes. A LOW-to-HIGH transition on $\overline{MRS2}$ toggled simultaneously with $\overline{MRS1}$, selects the programming method (serial or parallel) and one of the three flag default offsets for FIFO2. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKC must occur while $\overline{MRS2}$ is LOW.
$\overline{PRS1}$	Partial Reset	I	A LOW on this pin initializes the FIFO1 read and write pointers to the first location of memory and sets the Port B output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained.
$\overline{PRS2}$	Partial Reset	I	A LOW on this pin initializes the FIFO2 read and write pointers to the first location of memory and sets the Port A output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained.
RENB	Port B Read Enable	I	RENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read data on Port B.
SIZEB[1]	Port B Bus Size Select	I	SIZEB determines the bus width of Port B. A HIGH on this pin selects byte (9-bit) bus size. A LOW on this pin selects word (18-bit) bus size. SIZEB works with SIZEC and BE to select the bus size and endian arrangement for ports B and C. The level of SIZEB must be static throughout device operation.
SIZEC[1]	Port C Bus Size Select	I	SIZEC determines the bus width of Port C. A HIGH on this pin selects byte (9-bit) bus size. A LOW on this pin selects word (18-bit) bus size. SIZEC works with SIZEB and BE to select the bus size and endian arrangement for ports B and C. The level of SIZEC must be static throughout device operation.
$\overline{SPM}$[1]	Serial Programming Mode	I	A LOW on this pin selects serial programming of partial flag offsets. A HIGH on this pin selects parallel programming or default offsets (8, 16, or 64).
WENC	Port C Write Enable	I	WENC must be HIGH to enable a LOW-to-HIGH transition of CLKC to write data on Port C.
W/$\overline{R}$A	Port A Write/Read Select	I	A HIGH selects a write operation and a LOW selects a read operation on Port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the HIGH impedance state when W/$\overline{R}$A is HIGH.

NOTE:
1. SIZEB, SIZEC and $\overline{SPM}$ are not TTL compatible. These inputs should be tied to GND or VCC.

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)(1)

Symbol	Rating	Commercial	Unit
V_{CC}	Supply Voltage Range	–0.5 to 7	V
V_I(2)	Input Voltage Range	–0.5 to V_{CC}+0.5	V
V_O(2)	Output Voltage Range	–0.5 to V_{CC}+0.5	V
I_{IK}	Input Clamp Current (V_I < 0 or V_I > V_{CC})	±20	mA
I_{OK}	Output Clamp Current (V_O = < 0 or V_O > V_{CC})	±50	mA
I_{OUT}	Continuous Output Current (V_O = 0 to V_{CC})	±50	mA
I_{CC}	Continuous Current Through V_{CC} or GND	±400	mA
T_{STG}	Storage Temperature Range	–65 to 150	°C

NOTES:
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage (Commercial)	4.5	5.0	5.5	V
V_{IH}	High-Level Input Voltage (Commercial)	2	—		V
V_{IL}	Low-Level Input Voltage (Commercial)	—	—	0.8	V
I_{OH}	High-Level Output Current (Commercial)	—	—	–4	mA
I_{OL}	Low-Level Output Current (Commercial)	—	—	8	mA
T_A	Operating Free-Air Temperature (Commercial)	0	—	70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)

Symbol	Parameter	Test Conditions		IDT723626 IDT723636 IDT723646 Commercial t_{CLK} = 15 ns			Unit
				Min.	Typ.(1)	Max.	
V_{OH}	Output Logic "1" Voltage	V_{CC} = 4.5V,	I_{OH} = –4 mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage	V_{CC} = 4.5V,	I_{OL} = 8 mA	—	—	0.5	V
I_{LI}	Input Leakage Current (Any Input)	V_{CC} = 5.5V,	V_I = V_{CC} or 0	—	—	±10	µA
I_{LO}	Output Leakage Current	V_{CC} = 5.5V,	V_O = V_{CC} or 0	—	—	±10	µA
I_{CC2}(2)	Standby Current (with CLKA, CLKB and CLKC running)	V_{CC} = 5.5V,	V_I = V_{CC} - 0.2V or 0	—	—	8	mA
I_{CC3}(2)	Standby Current (no clocks running)	V_{CC} = 5.5V,	V_I = V_{CC} - 0.2V or 0	—	—	1	mA
C_{IN}(3)	Input Capacitance	V_I = 0,	f = 1 MHz	—	4	—	pF
C_{OUT}(3)	Output Capacitance	V_O = 0,	f = 1 MHZ	—	8	—	pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_A = 25°C.
2. For additional I_{CC} information, *see Figure 1, Typical Characteristics: Supply Current (I_{CC}) vs. Clock Frequency (fs).*
3. Characterized values, not currently tested.

DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC(f)}$ current for the graph in Figure 1 was taken while simultaneously reading and writing a FIFO on the IDT723626/723636/723646 with CLKA, CLKB and CLKC set to fs. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero capacitance load. Once the capacitance load per data-output channel and the number of IDT723626/723636/723646 inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC(f)}$ taken from Figure 1, the maximum power dissipation (P_T) of these FIFOs may be calculated by:

$$P_T = V_{CC} \times [I_{CC(f)} + (N \times \Delta I_{CC} \times dc)] + \sum_{N} (C_L \times V_{CC}^2 \times f_o)$$

where:

N	=	number of inputs driven by TTL levels
ΔI_{CC}	=	increase in power supply current for each input at a TTL HIGH level
dc	=	duty cycle of inputs at a TTL HIGH level of 3.4V
C_L	=	output capacitance load
f_o	=	switching frequency of an output

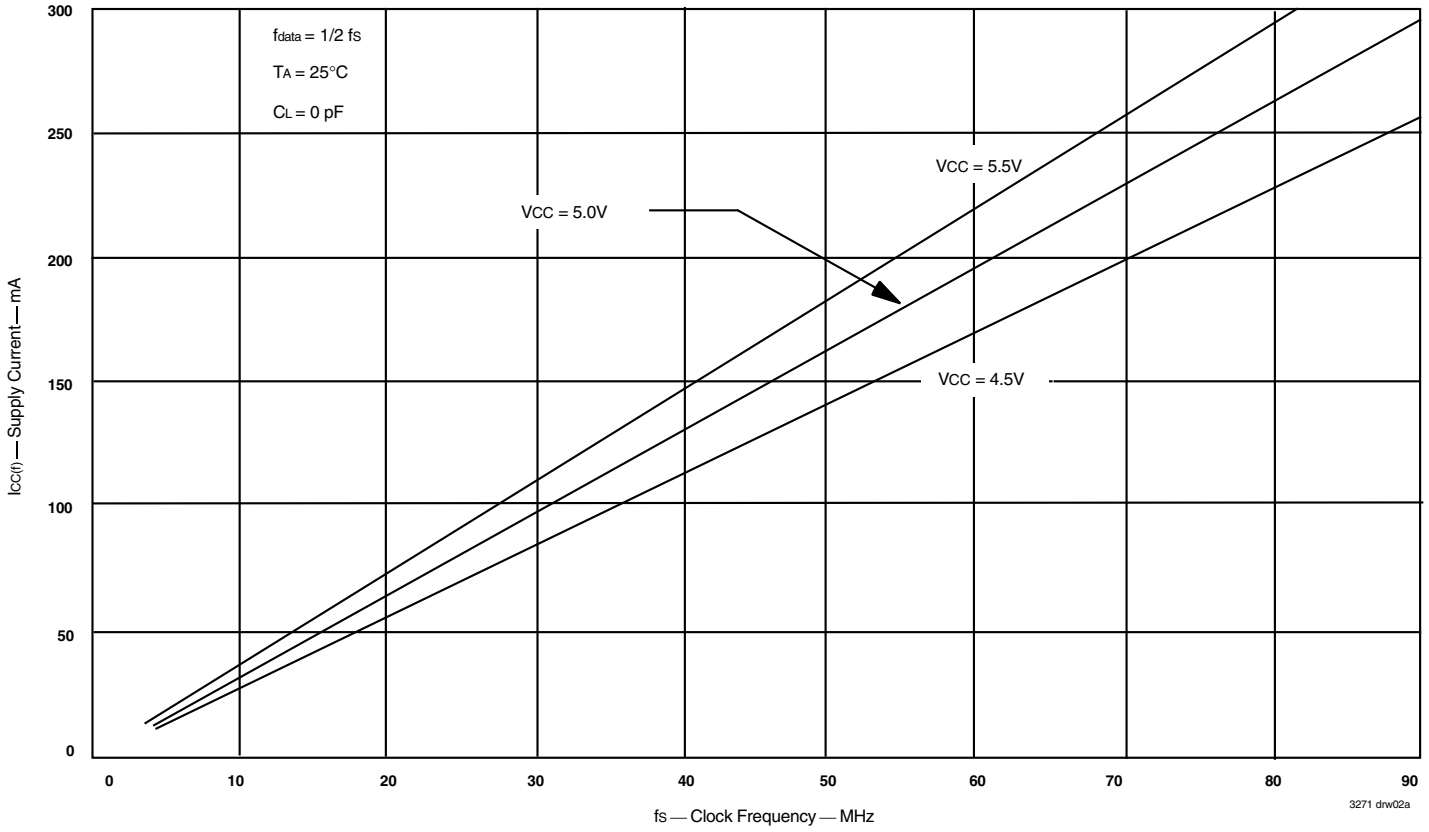


Figure 1. Typical Characteristics: Supply Current (Icc) vs. Clock Frequency (fs)

TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial IDT723626L15 IDT723636L15 IDT723646L15 Min.	Commercial IDT723626L15 IDT723636L15 IDT723646L15 Max.	Unit
f_S	Clock Frequency, CLKA, CLKB, or CLKC	—	66.7	MHz
t_{CLK}	Clock Cycle Time, CLKA, CLKB, or CLKC	15	—	ns
t_{CLKH}	Pulse Duration, CLKA, CLKB, or CLKC HIGH	6	—	ns
t_{CLKL}	Pulse Duration, CLKA, CLKB, OR CLKC LOW	6	—	ns
t_{DS}	Setup Time, A0-A35 before CLKA↑ and C0-C17 before CLKC↑	4	—	ns
t_{ENS1}	Setup Time, $\overline{CSA}$ and W/$\overline{R}$A before CLKA↑; $\overline{CSB}$ before CLKB↑	4.5	—	ns
t_{ENS2}	Setup Time, ENA and MBA before CLKA↑; RENB and MBB before CLKB↑ ; WENC and MBC before CLKC↑	4.5	—	ns
t_{RSTS}	Setup Time, $\overline{MRS1}$, $\overline{MRS2}$, $\overline{PRS1}$, or $\overline{PRS2}$ LOW before CLKA↑ or CLKB↑(1)	5	—	ns
t_{FSS}	Setup Time, FS0 and FS1 before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	7.5	—	ns
t_{BES}	Setup Time, BE/$\overline{FWFT}$ before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	7.5	—	ns
t_{SPMS}	Setup Time, $\overline{SPM}$ before $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	7.5	—	ns
t_{SDS}	Setup Time, FS0/SD before CLKA↑	4	—	ns
t_{SENS}	Setup Time, FS1/$\overline{SEN}$ before CLKA↑	4	—	ns
t_{FWS}	Setup Time, BE/$\overline{FWFT}$ before CLKA↑	0	—	ns
t_{DH}	Hold Time, A0-A35 after CLKA↑ and C0-C17 after CLKC↑	1	—	ns
t_{ENH}	Hold Time, $\overline{CSA}$, W/$\overline{R}$A, ENA, and MBA after CLKA↑; $\overline{CSB}$, RENB, and MBB after CLKB↑; WENC and MBC after CLKC↑	1	—	ns
t_{RSTH}	Hold Time, $\overline{MRS1}$, $\overline{MRS2}$, $\overline{PRS1}$ or $\overline{PRS2}$ LOW after CLKA↑ or CLKB↑(1)	4	—	ns
t_{FSH}	Hold Time, FS0 and FS1 after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	2	—	ns
t_{BEH}	Hold Time, BE/$\overline{FWFT}$ after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	2	—	ns
t_{SPMH}	Hold Time, $\overline{SPM}$ after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	2	—	ns
t_{SDH}	Hold Time, FS0/SD after CLKA↑	1	—	ns
t_{SENH}	Hold Time, FS1/$\overline{SEN}$ HIGH after CLKA↑	1	—	ns
t_{SPH}	Hold Time, FS1/$\overline{SEN}$ HIGH after $\overline{MRS1}$ and $\overline{MRS2}$ HIGH	2	—	ns
t_{SKEW1}(2)	Skew Time, between CLKA↑and CLKB↑ for $\overline{EFB}$/ORB and $\overline{FFA}$/IRA; between CLKA↑ and CLKC↑ for $\overline{EFA}$/ORA and $\overline{FFC}$/IRC	7.5	—	ns
t_{SKEW2}(2,3)	Skew Time, between CLKA↑ and CLKB↑ for $\overline{AEB}$ and AFA; between CLKA↑ and CLKC↑ for $\overline{AEA}$ and $\overline{AFC}$	12	—	ns

NOTES:
1. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
2. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship among CLKA cycle, CLKB cycle, and CLKC cycle.
3. Design simulated, not tested (typical values).

SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, CL = 30pF

(Commercial: V_{CC} = 5.0V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial IDT723626L15 IDT723636L15 IDT723646L15 Min.	Commercial IDT723626L15 IDT723636L15 IDT723646L15 Max.	Unit
t_A	Access Time, CLKA↑ to A0-A35 and CLKB↑ to B0-B17	2	10	ns
t_{WFF}	Propagation Delay Time, CLKA↑ to $\overline{FFA}$/IRA and CLKC↑ to $\overline{FFC}$/IRC	2	8	ns
t_{REF}	Propagation Delay Time, CLKA↑ to $\overline{EFA}$/ORA and CLKB↑ to $\overline{EFB}$/ORB	1	8	ns
t_{PAE}	Propagation Delay Time, CLKA↑ to $\overline{AEA}$ and CLKB↑ to $\overline{AEB}$	1	8	ns
t_{PAF}	Propagation Delay Time, CLKA↑ to $\overline{AFA}$ and CLKC↑ to $\overline{AFC}$	1	8	ns
t_{PMF}	Propagation Delay Time, CLKA↑ to $\overline{MBF1}$ LOW or $\overline{MBF2}$ HIGH, CLKB↑ to $\overline{MBF1}$ HIGH, and CLKC↑ to $\overline{MBF2}$ LOW	0	8	ns
t_{PMR}	Propagation Delay Time, CLKA↑ to B0-B17[1] and CLKC↑ to A0-A35[2]	2	10	ns
t_{MDV}	Propagation Delay Time, MBA to A0-A35 valid and MBB to B0-B17 valid	2	10	ns
t_{RSF}	Propagation Delay Time, $\overline{MRS1}$ or $\overline{PRS1}$ LOW to $\overline{AEB}$ LOW, $\overline{AFA}$ HIGH, and $\overline{MBF1}$ HIGH and $\overline{MRS2}$ or $\overline{PRS2}$ LOW to $\overline{AEA}$ LOW, $\overline{AFC}$ HIGH, and $\overline{MBF2}$ HIGH	1	15	ns
t_{EN}	Enable Time, $\overline{CSA}$ or W/$\overline{R}$A LOW to A0-A35 Active and $\overline{CSB}$ LOW to B0-B17 Active	2	10	ns
t_{DIS}	Disable Time, $\overline{CSA}$ or W/$\overline{R}$A HIGH to A0-A35 at HIGH impedance and $\overline{CSB}$ HIGH to B0-B17 at HIGH impedance	1	8	ns

NOTES:
1. Writing data to the mail1 register when the B0-B17 outputs are active and MBB is HIGH.
2. Writing data to the mail2 register when the A0-A35 outputs are active and MBA is HIGH.

SIGNAL DESCRIPTION

MASTER RESET ($\overline{MRS1}$, $\overline{MRS2}$)

After power up, a Master Reset operation must be performed by providing a LOW pulse to $\overline{MRS1}$ and $\overline{MRS2}$ simultaneously. Afterwards, the FIFO1 memory of the IDT723626/723636/723646 undergoes a complete reset by taking its associated Master Reset ($\overline{MRS1}$) input LOW for at least four Port A Clock (CLKA) and four Port B Clock (CLKB) LOW-to-HIGH transitions. The FIFO2 memory undergoes a complete reset by taking its associated Master Reset ($\overline{MRS2}$) input LOW for at least four Port A Clock (CLKA) and four Port C Clock (CLKC) LOW-to-HIGH transitions. The Master Reset inputs can switch asynchronously to the clocks. A Master Reset initializes the associated read and write pointers to the first location of the memory and forces the Full/Input Ready flag ($\overline{FFA}$/IRA, $\overline{FFC}$/IRC) LOW, the Empty/Output Ready flag ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB) LOW, the Almost-Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the Almost-Full flag ($\overline{AFA}$, $\overline{AFC}$) HIGH. A Master Reset also forces the associated Mailbox Flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Master Reset, the FIFO's Full/Input Ready flag is set HIGH after two Write clock cycles. Then the FIFO is ready to be written to.

A LOW-to-HIGH transition on a FIFO1 Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input latches the value of the Big-Endian (BE) input for determining the order by which bytes are transferred through ports B and C. It also latches the values of the Flag Select (FS0, FS1) and Serial Programming Mode ($\overline{SPM}$) inputs for choosing the Almost-Full and Almost-Empty offset programming mode.

A LOW-to-HIGH transition on the FIFO2 Master Reset ($\overline{MRS2}$) clears the flag offset registers of FIFO2 (X2, Y2). A LOW-to-HIGH transition on the FIFO2 Master Reset input ($\overline{MRS2}$) latches the value of the Big-Endian (BE) input for Ports B and C and also latches the values of the Flag Select (FS0, FS1) and Serial Programming Mode ($\overline{SPM}$) inputs for choosing the Almost-Full and Almost-Empty offset programming method (for details see Table 1, *Flag Programming*, and *Almost-Empty and Almost-Full Flag Offset Programming* section). The relevant Master Reset timing diagrams can be found in Figure 4 and 5.

Note that MBC must be HIGH during Master Reset (until $\overline{FFA}$/IRA and $\overline{FFC}$/IRC go HIGH). MBA and MBB are "don't care" inputs[1] during Master Reset.

PARTIAL RESET ($\overline{PRS1}$, $\overline{PRS2}$)

The FIFO1 memory of these devices undergoes a limited reset by taking its associated Partial Reset ($\overline{PRS1}$) input LOW for at least four Port A Clock (CLKA) and four Port B Clock (CLKB) LOW-to-HIGH transitions. The FIFO2 memory undergoes a limited reset by taking its associated Partial Reset ($\overline{PRS2}$) input LOW for at least four Port A Clock (CLKA) and four Port C Clock (CLKC) LOW-to-HIGH transitions. The Partial Reset inputs can switch asynchronously to the clocks. A Partial Reset initializes the internal read and write pointers and forces the Full/Input Ready flag ($\overline{FFA}$/IRA, $\overline{FFC}$/IRC) LOW, the Empty/Output Ready flag ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB) LOW, the Almost-Empty flag ($\overline{AEA}$, $\overline{AEB}$) LOW, and the Almost-Full flag ($\overline{AFA}$, $\overline{AFC}$) HIGH. A Partial Reset also forces the Mailbox Flag ($\overline{MBF1}$, $\overline{MBF2}$) of the parallel mailbox register HIGH. After a Partial Reset, the FIFO's Full/Input Ready flag is set HIGH after two Write clock cycles.

Whatever flag offsets, programming method (parallel or serial), and timing mode (FWFT or IDT Standard mode) are currently selected at the time a Partial Reset is initiated, those settings will remain unchanged upon completion of the reset operation. A Partial Reset may be useful in the case where reprogramming a FIFO following a Master Reset would be inconvenient. See Figure 6 and 7 for Partial Reset timing diagrams.

BIG-ENDIAN/FIRST WORD FALL THROUGH (BE/$\overline{FWFT}$)

— ENDIAN SELECTION

This is a dual purpose pin. At the time of Master Reset, the BE select function is active, permitting a choice of Big- or Little-Endian byte arrangement for data written to Port C or read from Port B. This selection determines the order by which bytes (or words) of data are transferred through those ports. For the following illustrations, note that both ports B and C are configured to have a byte (or a word) bus size.

A HIGH on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) inputs go from LOW to HIGH will select a Big-Endian arrangement. When data is moving in the direction from Port A to Port B, the most significant byte (word) of the long word written to Port A will be read from Port B first; the least significant byte (word) of the long word written to Port A will be read from Port B last. When data is moving in the direction from Port C to Port A, the byte (word) written to Port C first will be read from Port A as the most significant byte (word) of the long word; the byte (word) written to Port C last will be read from Port A as the least significant byte (word) of the long word.

A LOW on the BE/$\overline{FWFT}$ input when the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) inputs go from LOW to HIGH will select a Little-Endian arrangement. When data is moving in the direction from Port A to Port B, the least significant byte (word) of the long word written to Port A will be read from Port B first; the most significant byte (word) of the long word written to Port A will be read from Port B last. When data is moving in the direction from Port C to Port A, the byte (word) written to Port C first will be read from Port A as the least significant byte (word) of the long word; the byte (word) written to Port C last will be read from Port A as the most significant byte (word) of the long word. Refer to Figures 2 and 3 for illustrations of the BE function. See Figure 4 (FIFO1 Master Reset) and 5 (FIFO2 Master Reset) for Endian Select timing diagrams.

— TIMING MODE SELECTION

After Master Reset, the FWFT select function is available, permitting a choice between two possible timing modes: IDT Standard mode or First Word Fall Through (FWFT) mode. Once the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input is HIGH, a HIGH on the BE/$\overline{FWFT}$ input during the next LOW-to-HIGH transition of CLKA (for FIFO1) and CLKC (for FIFO2) will select IDT Standard mode. This mode uses the Empty Flag function ($\overline{EFA}$, $\overline{EFB}$) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function ($\overline{FFA}$, $\overline{FFC}$) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using a formal read operation.

Once the Master Reset ($\overline{MRS1}$, $\overline{MRS2}$) input is HIGH, a LOW on the BE/$\overline{FWFT}$ input during the next LOW-to-HIGH transition of CLKA (for FIFO1) and CLKC (for FIFO2) will select FWFT mode. This mode uses the Output Ready function (ORA, ORB) to indicate whether or not there is valid data at the data outputs (A0-A35 or B0-B17). It also uses the Input Ready function (IRA, IRC) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to the data

NOTE:
1. Either a HIGH or LOW can be applied to a "don't care" input with no change to the logical operation of the FIFO. Nevertheless, inputs that are temporarily "don't care" (along with unused inputs) must not be left open, rather they must be either HIGH or LOW.

outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation. Refer to Figure 4 (FIFO1 Master Reset) and Figure 5 (FIFO2 Master Reset) for First Word Fall Through select timing diagrams.

Following Master Reset, the level applied to the BE/$\overline{FWFT}$ input to choose the desired timing mode must remain static throughout FIFO operation.

PROGRAMMING THE ALMOST-EMPTY AND ALMOST-FULL FLAGS

Four registers in these FIFOs are used to hold the offset values for the Almost-Empty and Almost-Full flags. The Port B Almost-Empty flag ($\overline{AEB}$) Offset register is labeled X1 and the Port A Almost-Empty flag ($\overline{AEA}$) Offset register is labeled X2. The Port A Almost-Full flag ($\overline{AFA}$) Offset register is labeled Y1 and the Port C Almost-Full flag ($\overline{AFC}$) Offset register is labeled Y2. The index of each register name corresponds to its FIFO number. The Offset registers can be loaded with preset values during the reset of a FIFO, programmed in parallel using the FIFO's Port A data inputs, or programmed in serial using the Serial Data (SD) input (see Table 1).

$\overline{SPM}$, FS0/SD, and FS1/$\overline{SEN}$ function the same way in both IDT Standard and FWFT modes.

— PRESET VALUES

To load a FIFO's Almost-Empty flag and Almost-Full flag Offset registers with one of the three preset values listed in Table 1, the Serial Program Mode ($\overline{SPM}$) and at least one of the flag-select inputs must be HIGH during the LOW-to-HIGH transition of its Master Reset ($\overline{MRS1}$ and $\overline{MRS2}$) input. For example, to load the preset value of 64 into X1 and Y1, $\overline{SPM}$, FS0 and FS1 must be HIGH when FIFO1 reset ($\overline{MRS1}$) returns HIGH. Flag Offset registers associated with FIFO2 are loaded with one of the preset values in the same way with FIFO2 Master Reset ($\overline{MRS2}$) toggled simultaneously with FIFO1 Master Reset ($\overline{MRS1}$). For relevant Preset value loading timing diagrams, see Figure 4 and 5.

— PARALLEL LOAD FROM PORT A

To program the X1, X2, Y1, and Y2 registers from Port A, perform a Master Reset on both FIFOs simultaneously with $\overline{SPM}$ HIGH and FS0 and FS1 LOW during the LOW-to-HIGH transition of $\overline{MRS1}$ and $\overline{MRS2}$. After this reset is complete, the first four writes to FIFO1 do not store data in RAM but load the Offset registers in the order Y1, X1, Y2, X2. The Port A data inputs used by the Offset registers are (A7-A0), (A8-A0), or (A9-A0) for the IDT723626, IDT723636, or IDT723646, respectively. The highest numbered input is used as the most significant bit of the binary number in each case. Valid programming values for the registers range from 1 to 252 for the IDT723626; 1 to 508 for the IDT723636; and 1 to 1,020 for the IDT723646. After all the Offset registers are programmed from Port A, the Port C Full/Input Ready flag ($\overline{FFC}$/IRC) is set HIGH, and both FIFOs begin normal operation.

Refer to Figure 8 for a timing diagram illustration for parallel programming of the flag offset values.

— SERIAL LOAD

To program the X1, X2, Y1, and Y2 registers serially, initiate a Master Reset with $\overline{SPM}$ LOW, FS0/SD LOW and FS1/$\overline{SEN}$ HIGH during the LOW-to-HIGH transition of $\overline{MRS1}$ and $\overline{MRS2}$. After this reset is complete, the X and Y register values are loaded bit-wise through the FS0/SD input on each LOW-to-HIGH transition of CLKA that the FS1/$\overline{SEN}$ input is LOW. There are 32-, 36-, or 40-bit writes needed to complete the programming for the IDT723626, IDT723636, or IDT723646, respectively. The four registers are written in the order Y1, X1, Y2 and finally, X2. The first-bit write stores the most significant bit of the Y1 register and the last-bit write stores the least significant bit of the X2 register. Each register value can be programmed from 1 to 252 (IDT723626), 1 to 508 (IDT723636), or 1 to 1,020 (IDT723646).

When the option to program the Offset registers serially is chosen, the Port A Full/Input Ready ($\overline{FFA}$/IRA) flag remains LOW until all register bits are written. $\overline{FFA}$/IRA is set HIGH by the LOW-to-HIGH transition of CLKA after the last bit is loaded to allow normal FIFO1 operation. The Port B Full/Input Ready ($\overline{FFC}$/IRC) flag also remains LOW throughout the serial programming process, until all register bits are written. $\overline{FFC}$/IRC is set HIGH by the LOW-to-HIGH transition of CLKC after the last bit is loaded to allow normal FIFO2 operation.

See Figure 9 timing diagram, *Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)*.

TABLE 1 — FLAG PROGRAMMING

$\overline{SPM}$	FS1/$\overline{SEN}$	FS0/SD	$\overline{MRS1}$	$\overline{MRS2}$	X1 AND Y1 REGISTERS[1]	X2 AND Y2 REGISTERS[2]
H	H	H	↑	X	64	X
H	H	H	↑	↑	64	64
H	H	L	↑	X	16	X
H	H	L	↑	↑	16	16
H	L	H	↑	X	8	X
H	L	H	↑	↑	8	8
H	L	L	↑	↑	Parallel programming via Port A	Parallel programming via Port A
L	H	L	↑	↑	Serial programming via SD	Serial programming via SD
L	H	H	↑	↑	Reserved	Reserved
L	L	H	↑	↑	Reserved	Reserved
L	L	L	↑	↑	Reserved	Reserved

NOTES:
1. X1 register holds the offset for $\overline{AEB}$; Y1 register holds the offset for $\overline{AFA}$.
2. X2 register holds the offset for $\overline{AEA}$; Y2 register holds the offset for $\overline{AFC}$.

FIFO WRITE/READ OPERATION

The state of the Port A data (A0-A35) outputs is controlled by Port A Chip Select ($\overline{CSA}$) and Port A Write/Read Select (W/$\overline{RA}$). The A0-A35 outputs are in the High-impedance state when either $\overline{CSA}$ or W/$\overline{RA}$ is HIGH. The A0-A35 outputs are active when both $\overline{CSA}$ and W/$\overline{RA}$ are LOW.

Data is loaded into FIFO1 from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is HIGH, ENA is HIGH, MBA is LOW, and $\overline{FFA}$/IRA is HIGH. Data is read from FIFO2 to the A0-A35 outputs by a LOW-to-HIGH transition of CLKA when $\overline{CSA}$ is LOW, W/$\overline{RA}$ is LOW, ENA is HIGH, MBA is LOW, and $\overline{EFA}$/ORA is HIGH (see Table 2). FIFO reads and writes on Port A are independent of any concurrent Port B and Port C operation.

The state of the Port B data (B0-B17) outputs is controlled by the Port B Chip Select ($\overline{CSB}$). The B0-B17 outputs are in the high-impedance state when $\overline{CSB}$ is HIGH. The B0-B17 outputs are active when $\overline{CSB}$ is LOW.

Data is read from FIFO1 to the B0-B17 outputs by a LOW-to-HIGH transition of CLKB when $\overline{CSB}$ is LOW, RENB is HIGH, MBB is LOW and $\overline{EFB}$/ORB is HIGH (see Table 3). FIFO reads on Port B are independent of any concurrent Port A and Port C operations.

Data is loaded into FIFO2 from the C0-C17 inputs on a LOW-to-HIGH transition of CLKC when WENB is HIGH, MBC is LOW, and $\overline{FFC}$/IRC is HIGH (see Table 4). FIFO writes on Port C are independent of any concurrent Port A and Port B operation.

The setup and hold time constraints for $\overline{CSA}$ and W/$\overline{RA}$ with regard to CLKA as well as $\overline{CSB}$ with regard to CLKB are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If ENA is LOW during a clock cycle, either $\overline{CSA}$ or W/$\overline{RA}$ may change states during the setup and hold time window of the cycle. This is also true for $\overline{CSB}$ when RENB is LOW.

When operating the FIFO in FWFT mode and the Output Ready flag is LOW, the next word written is automatically sent to the FIFO's output register by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH. When the Output Ready flag is HIGH, subsequent data is clocked to the output registers only when a read is selected using $\overline{CSA}$, W/$\overline{RA}$, ENA and MBA at Port A or using $\overline{CSB}$, RENB and MBB at Port B.

When operating the FIFO in IDT Standard mode, the first word will cause the Empty Flag to change state on the second LOW-to-HIGH transition of the read clock. The data word will not be automatically sent to the output register. Instead, data residing in the FIFO's memory array is clocked to the output register only when a read is selected using $\overline{CSA}$ W/$\overline{RA}$ ENA and MBA at Port A or using $\overline{CSB}$, RENB and MBB at Port B. Relevant write and read timing diagrams for Port A can be found in Figure 10 and 15. Relevant read and write timing diagrams for Port B and Port C, together with Bus-Matching and Endian Select operations can be found in Figures 11 to 14.

TABLE 2 — PORT A ENABLE FUNCTION TABLE

$\overline{CSA}$	W/$\overline{RA}$	ENA	MBA	CLKA	DATA A (A0-A35) I/O	PORT FUNCTION
H	X	X	X	X	High-Impedance	None
L	H	L	X	X	Input	None
L	H	H	L	↑	Input	FIFO1 write
L	H	H	H	↑	Input	Mail1 write
L	L	L	L	X	Output	None
L	L	H	L	↑	Output	FIFO2 read
L	L	L	H	X	Output	None
L	L	H	H	↑	Output	Mail2 read (set $\overline{MBF2}$ HIGH)

TABLE 3 — PORT B ENABLE FUNCTION TABLE

$\overline{CSB}$	RENB	MBB	CLKB	DATA B (B0-B17) OUTPUTS	PORT FUNCTION
H	X	X	X	High-Impedance	None
L	L	L	X	Output	None
L	H	L	↑	Output	FIFO1 read
L	L	H	X	Output	None
L	H	H	↑	Output	Mail1 read (set $\overline{MBF1}$ HIGH)

TABLE 4 — PORT C ENABLE FUNCTION TABLE

WENC	MBC	CLKC	DATA C (C0-C17) INPUTS	PORT FUNCTION
H	L	↑	Input	FIFO2 write
H	H	↑	Input	Mail2 write
L	L	X	Input	None
L	H	X	Input	None

SYNCHRONIZED FIFO FLAGS

Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag signal reliability by reducing the probability of metastable events when CLKA operates asynchronously with respect to either CLKB or CLKC. $\overline{EFA}$/ORA, $\overline{AEA}$, $\overline{FFA}$/IRA, and $\overline{AFA}$ are synchronized to CLKA. $\overline{EFB}$/ORB and $\overline{AEB}$ are synchronized to CLKB. $\overline{FFC}$/IRC and $\overline{AFC}$ are synchronized to CLKC. Tables 5 and 6 show the relationship of each port flag to FIFO1 and FIFO2.

EMPTY/OUTPUT READY FLAGS ($\overline{EFA}$/ORA, $\overline{EFB}$/ORB)

These are dual purpose flags. In the FWFT mode, the Output Ready (ORA, ORB) function is selected. When the Output Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

In the IDT Standard mode, the Empty Flag ($\overline{EFA}$, $\overline{EFB}$) function is selected. When the Empty Flag is HIGH, data is available in the FIFO's RAM memory for reading to the output register. When the Empty Flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array. For both the FWFT and IDT Standard modes, the FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2.

In FWFT mode, from the time a word is written to a FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and three cycles of the port clock that reads data from the FIFO have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In IDT Standard mode, from the time a word is written to a FIFO, the Empty Flag will indicate the presence of data available for reading in a minimum of two cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Empty Flag of the FIFO remains LOW until the second LOW-to-HIGH transition of the synchronizing clock occurs, forcing the Empty Flag HIGH; only then can data be read.

A LOW-to-HIGH transition on an Empty/Output Ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time t_{SKEW1} or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 16, 17, 18 and 19).

TABLE 5 — FIFO1 FLAG OPERATION (IDT Standard and FWFT modes)

Number of Words in FIFO Memory[1,2]			Synchronized to CLKB		Synchronized to CLKA	
IDT723626[3]	IDT723636[3]	IDT723646[3]	$\overline{EFB}$/ORB	$\overline{AEB}$	$\overline{AFA}$	$\overline{FFA}$/IRA
0	0	0	L	L	H	H
1 to X1	1 to X1	1 to X1	H	L	H	H
(X1+1) to [256-(Y1+1)]	(X1+1) to [512-(Y1+1)]	(X1+1) to [1,024-(Y1+1)]	H	H	H	H
(256-Y1) to 255	(512-Y1) to 511	(1,024-Y1) to 1,023	H	H	L	H
256	512	1,024	H	H	L	L

NOTES:
1. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
2. Data in the output register does not count as a "word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. X1 is the almost-empty offset for FIFO1 used by $\overline{AEB}$. Y1 is the almost-full offset for FIFO1 used by $\overline{AFA}$. Both X1 and Y1 are selected during a FIFO1 reset or port A programming.
4. The ORB and IRA functions are active during FWFT mode; the $\overline{EFB}$ and $\overline{FFA}$ functions are active in IDT Standard mode.

TABLE 6 — FIFO2 FLAG OPERATION (IDT Standard and FWFT modes)

Number of Words in FIFO Memory[1,2]			Synchronized to CLKA		Synchronized to CLKC	
IDT723626[3]	IDT723636[3]	IDT723646[3]	$\overline{EFA}$/ORA	$\overline{AEA}$	$\overline{AFC}$	$\overline{FFC}$/IRC
0	0	0	L	L	H	H
1 to X2	1 to X2	1 to X2	H	L	H	H
(X2+1) to [256-(Y2+1)]	(X2+1) to [512-(Y2+1)]	(X2+1) to [1,024-(Y2+1)]	H	H	H	H
(256-Y2) to 255	(512-Y2) to 511	(1,024-Y2) to 1,023	H	H	L	H
256	512	1,024	H	H	L	L

NOTES:
1. When a word loaded to an empty FIFO is shifted to the output register, its previous FIFO memory location is free.
2. Data in the output register does not count as a "word in FIFO memory". Since in FWFT mode, the first word written to an empty FIFO goes unrequested to the output register (no read operation necessary), it is not included in the FIFO memory count.
3. X2 is the almost-empty offset for FIFO2 used by $\overline{AEA}$. Y2 is the almost-full offset for FIFO2 used by $\overline{AFC}$. Both X2 and Y2 are selected during a FIFO2 reset or port A programming.
4. The ORA and IRC functions are active during FWFT mode; the $\overline{EFA}$ and $\overline{FFC}$ functions are active in IDT Standard mode.

FULL/INPUT READY FLAGS ($\overline{FFA}$/IRA, $\overline{FFC}$/IRC)

These are dual purpose flags. In FWFT mode, the Input Ready (IRA and IRC) function is selected. In IDT Standard mode, the Full Flag ($\overline{FFA}$ and $\overline{FFC}$) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the FIFO to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and attempted writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array. For both FWFT and IDT Standard modes, each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls a Full/Input Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles of the Full/Input Ready flag synchronizing clock. Therefore, an Full/Input Ready flag is LOW if less than two cycles of the Full/Input Ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full/Input Ready flag synchronizing clock after the read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on a Full/Input Ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time t_{SKEW1} or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 20, 21, 22, and 23).

ALMOST-EMPTY FLAGS ($\overline{AEA}$, $\overline{AEB}$)

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array. The state machine that controls an Almost-Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The almost-empty state is defined by the contents of register X1 for $\overline{AEB}$ and register X2 for $\overline{AEA}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming section). An Almost-Empty flag is LOW when its FIFO contains X or less words and is HIGH when its FIFO contains (X+1) or more words. A data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Empty flag synchronizing clock are required after a FIFO write for its Almost-Empty flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing (X+1) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the (X+1) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the (X+1) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the write that fills the FIFO to (X+1) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle. (See Figures 24 and 25).

ALMOST-FULL FLAGS ($\overline{AFA}$, $\overline{AFC}$)

The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The almost-full state is defined by the contents of register Y1 for $\overline{AFA}$ and register Y2 for $\overline{AFC}$. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see *Almost-Empty flag and Almost-Full flag offset programming* section). An Almost-Full flag is LOW when the number of words in its FIFO is greater than or equal to (256-Y), (512-Y), or (1,024-Y) for the IDT723626, IDT723636, or IDT723646 respectively. An Almost-Full flag is HIGH when the number of words in its FIFO is less than or equal to [256-(Y+1)], [512-(Y+1)], or [1,024-(Y+1)] for the IDT723626, IDT723636, or IDT723646 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for its Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Full flag of a FIFO containing [256/512/1,024-(Y+1)] or less words remains LOW if two cycles of its synchronizing clock have not elapsed since the read that reduced the number of words in memory to [256/512/1,024-(Y+1)]. An Almost-Full flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO read that reduces the number of words in memory to [256/512/1,024-(Y+1)]. A LOW-to-HIGH transition of an Almost-Full flag synchronizing clock begins the first synchronization cycle if it occurs at time t_{SKEW2} or greater after the read that reduces the number of words in memory to [256/512/1,024-(Y+1)]. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle (see Figures 26 and 27).

MAILBOX REGISTERS

Each FIFO has an 18-bit bypass register allowing the passage of command and control information from Port A to Port B or from Port C to Port A without putting it in queue. The Mailbox Select (MBA, MBB and MBC) inputs choose between a mail register and a FIFO for a port data transfer operation. The usable width of both the Mail1 and Mail2 registers matches the selected bus size for ports B and C.

When sending data from Port A to Port B via the Mail1 Register, the following is the case: A LOW-to-HIGH transition on CLKA writes data to the Mail1 Register when a Port A write is selected by $\overline{CSA}$, W/$\overline{R}$A, and ENA with MBA HIGH. If the selected Port B bus size is 18 bits, then the usable width of the Mail1 Register employs data lines A0-A17. (In this case, A18-A35 are don't care inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail1 Register employs data lines A0-A8. (In this case, A9-A35 are don't care inputs.)

When sending data from Port C to Port A via the Mail2 Register, the following is the case: A LOW-to-HIGH transition on CLKC writes data to the Mail2 Register when a Port C write is selected by WENC with MBC HIGH. If the selected Port C bus size is 18 bits, then the usable width of the Mail2 Register employs data lines C0-C17. If the selected Port C bus size is 9 bits, then the usable width of the Mail2 Register employs data lines C0-C8. (In this case, C9-C17 are don't care inputs.)

Writing data to a mail register sets its corresponding flag ($\overline{MBF1}$ or $\overline{MBF2}$) LOW. Attempted writes to a mail register are ignored while the mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from the FIFO output register when the port Mailbox select input is LOW and from the mail register when the port mailbox select input is HIGH.

The Mail1 Register Flag ($\overline{MBF1}$) is set HIGH by a LOW-to-HIGH transition on CLKB when a Port B read is selected by $\overline{CSB}$, and RENB with MBB HIGH. For an 18-bit bus size, 18 bits of mailbox data are placed on B0-B17. For the 9-bit bus size, 9 bits of mailbox data are placed on B0-B8. (In this case, B9-B17 are indeterminate.)

The Mail2 Register Flag ($\overline{MBF2}$) is set HIGH by a LOW-to-HIGH transition on CLKA when a Port A read is selected by $\overline{CSA}$, W/$\overline{R}$A, and ENA with MBA HIGH. The data in a mail register remains intact after it is read and changes only when new data is written to the register. For an 18-bit bus size, 18 bits of mailbox

data appear on A18-A35. (In this case, A0-A17 are indeterminate.) For a 9-bit bus size, 9 bits of mailbox data appear on A18-A26. (In this case, A0-A17 and A27-A35 are indeterminate.)

The data in a mail register remains intact after it is read and changes only when new data is written to the register. The Endian Select feature has no effect on mailbox data.

Note that MBC must be HIGH during Master Reset (until $\overline{FFA}$/IRA and $\overline{FFC}$/IRC go HIGH. MBA and MBB are don't care inputs during Master Reset. For mail registers and mail register flag timing diagrams, see Figure 28 and 29.

BUS SIZING

Port B may be configured in either an 18-bit word or a 9-bit byte format for data read from FIFO1. Port C may be configured in either an 18-bit word or a 9-bit byte format for data written to FIFO2. The bus size can be selected independently for Ports B and C. The level applied to the Port B Size Select (SIZEB) input determines the Port B bus size and the level applied to the Port C Size Select (SIZEC) input determines the Port C bus size. These levels should be static throughout FIFO operation. Both bus size selections are implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH, as shown in Figures 2 and 3.

Two different methods for sequencing data transfer are available for Ports B and C regardless of whether the bus size selection is byte- or word-size. They are referred to as Big-Endian (most significant byte first) and Little-Endian (least significant byte first). The level applied to the Big-Endian Select (BE) input during the LOW-to-HIGH transition of $\overline{MRS1}$ and $\overline{MRS2}$ selects the endian method that will be active during FIFO operation. This selection applies to both ports B and C. The endian method is implemented at the completion of Master Reset, by the time the Full/Input Ready flag is set HIGH, as shown in Figures 2 and 3 (see Endian Selection section).

Only 36-bit long word data is written to or read from the two FIFO memories on these devices. Bus-matching operations are done after data is read from the FIFO1 RAM (Port B) and before data is written to the FIFO2 RAM (Port C).

The Endian Select operations are not available when transferring data via mailbox registers. Furthermore, both the word- and byte-size bus selections limit the width of the data bus that can be used for mail register operations. In this case, only those byte lanes belonging to the selected word- or byte-size bus can carry mailbox data. The remaining data outputs will be indeterminate. The remaining data inputs will be don't care inputs. For example, when a word-size bus is selected on Port B, then mailbox data can be transmitted only from A0-A17 to B0-B17. When a byte-size bus is selected on Port B, then mailbox data can be transmitted only from A0-A8 to B0-B8. Similarly, when a word-size bus is selected on Port C, then mailbox data can be transmitted only from C0-C17 to A18-A35. When a byte-size bus is selected on Port C, then mailbox data can be transmitted only from C0-C8 to A18-A26. (See Figures 28 and 29).

BUS-MATCHING FIFO1 READS

Data is read from the FIFO1 RAM in 36-bit long word increments. Since Port B can have a byte or word size, only the first one or two bytes appear on the selected portion of the FIFO1 output register, with the rest of the long word stored in auxiliary registers. In this case, subsequent FIFO1 reads output the rest of the long word to the FIFO1 output register in the order shown by Figure 2.

When reading data from FIFO1 in byte format, the unused B9-B17 outputs are indeterminate.

BUS-MATCHING FIFO2 WRITES

Data is written to the FIFO2 RAM in 36-bit long word increments. Data written to FIFO2 with a byte or word bus size stores the initial bytes or words in auxiliary registers. The CLKC rising edge that writes the fourth byte or the second word of long word to FIFO2 also stores the entire long word in the FIFO2 memory. The bytes are arranged in the manner shown in Figure 3.

When writing data to FIFO2 in byte format, the unused C9-C17 inputs are don't care inputs.

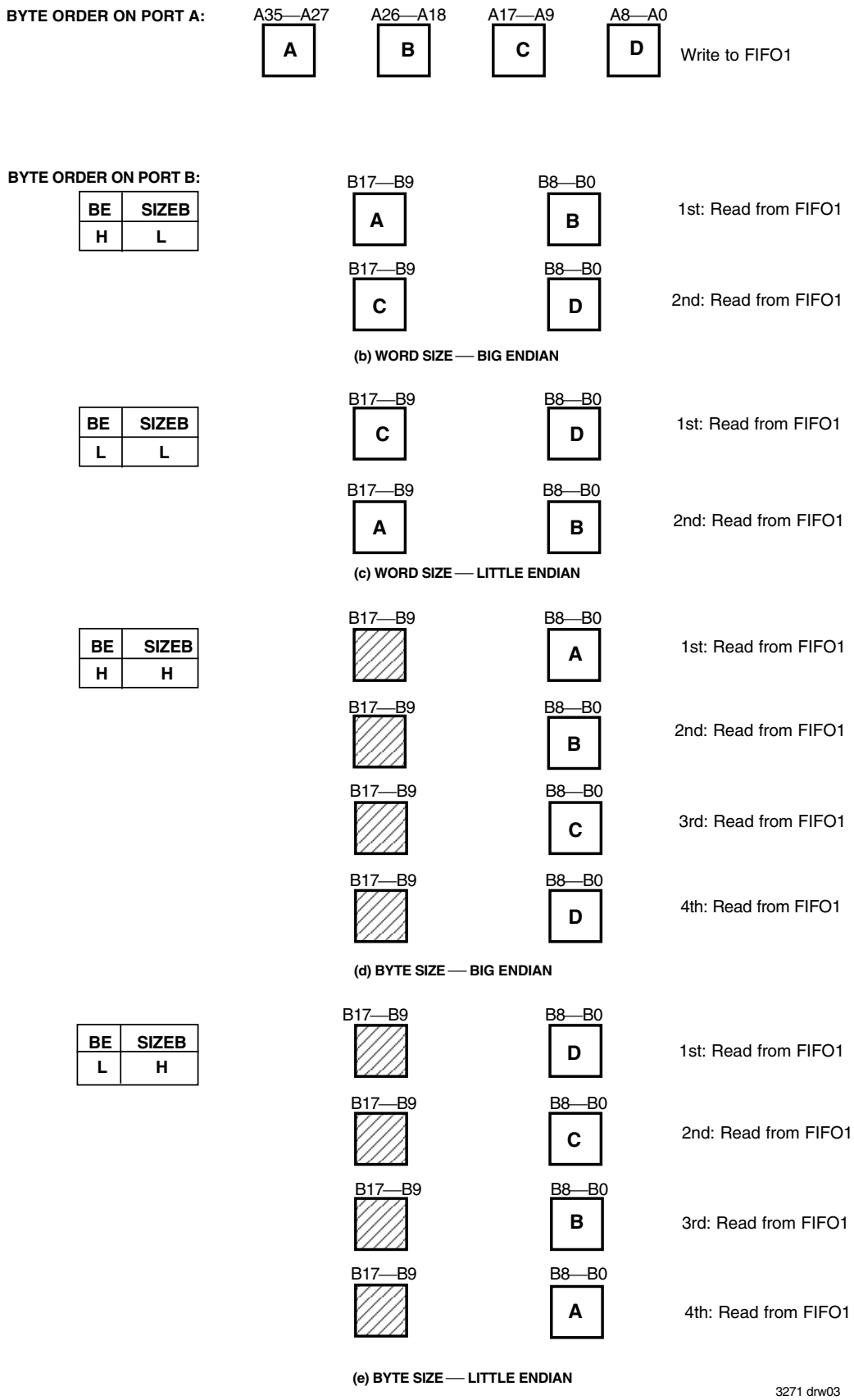


Figure 2. Port B Bus Sizing

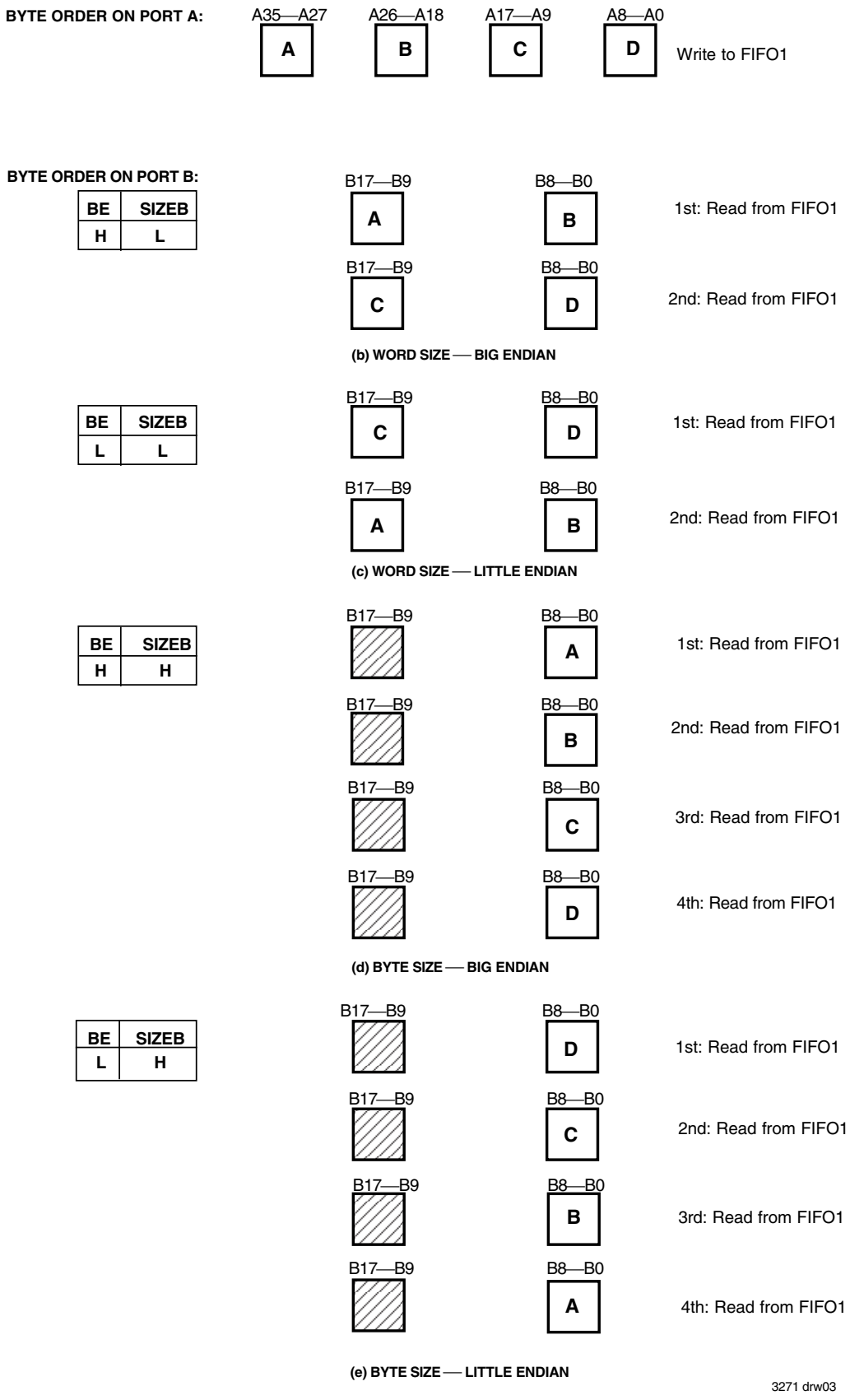
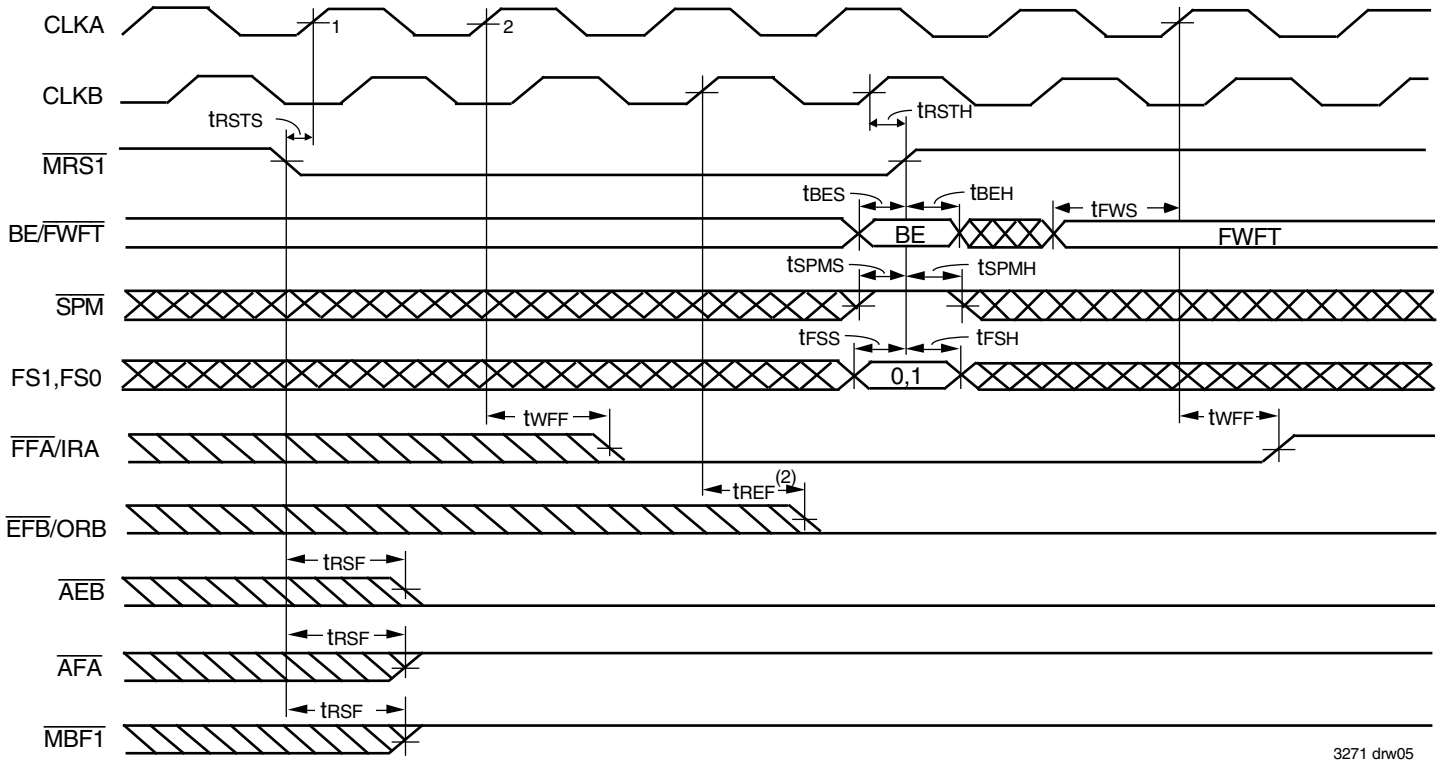
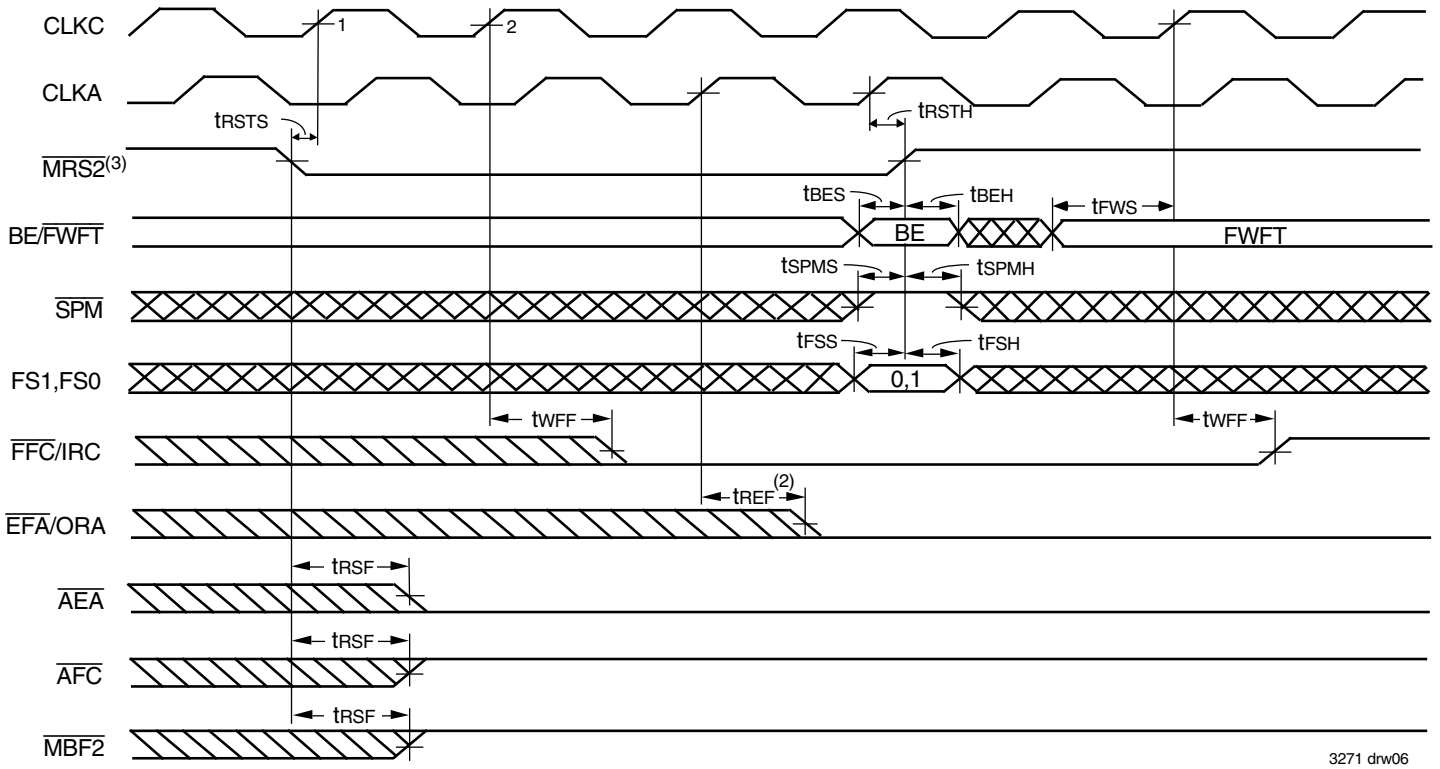


Figure 3. Port C Bus Sizing



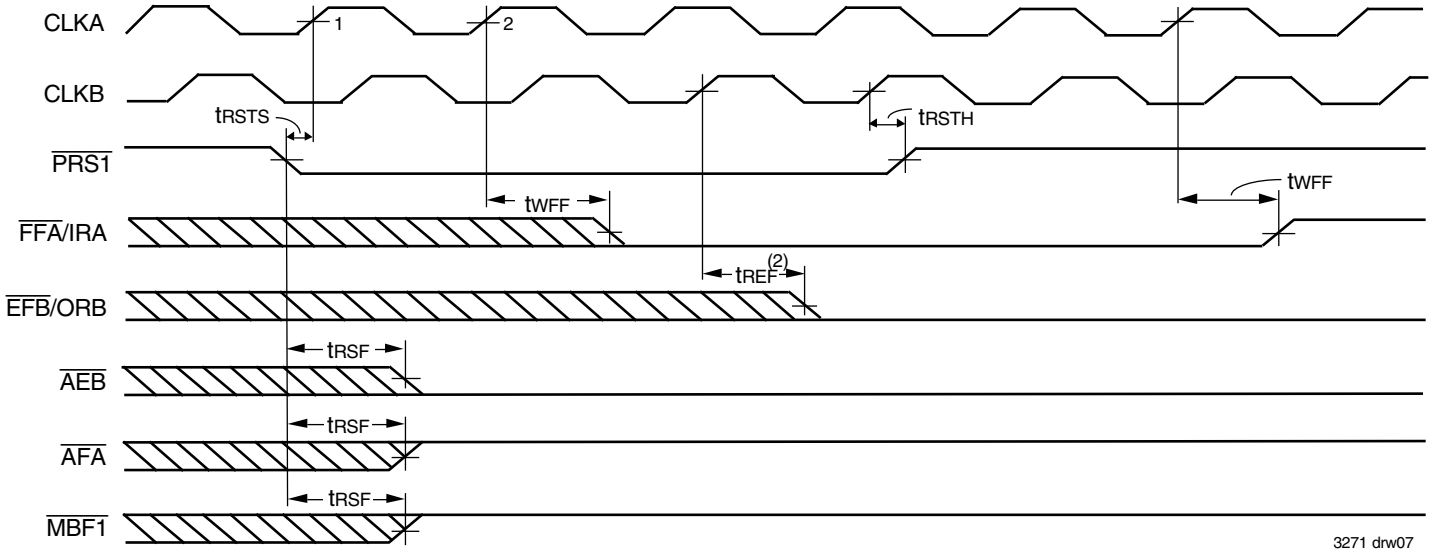
NOTES:
1. PRS1 and MBC must be HIGH during Master Reset until the rising edge of FFA/IRA goes HIGH.
2. If BE/FWFT is HIGH, then EFB/ORB will go LOW one CLKB cycle earlier than in this case where BE/FWFT is LOW.

Figure 4. FIFO1 Master Reset and Loading X1 and Y1 with a Preset Value of Eight (IDT Standard and FWFT Modes)



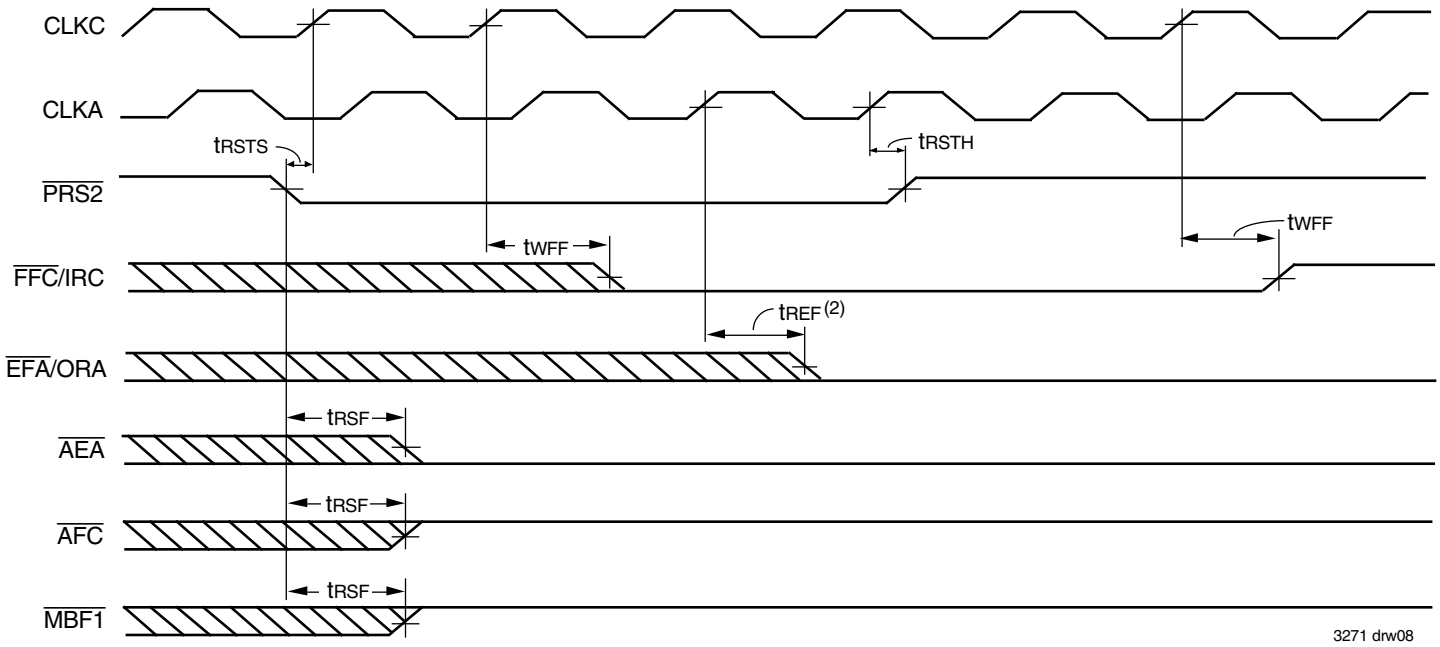
NOTES:
1. PRS2 and MBC must be HIGH during Master Reset until the rising edge of FFC/IRC goes HIGH.
2. If BE/FWFT is HIGH, then EFA/ORA will go LOW one CLKA cycle earlier than in this case where BE/FWFT is LOW.
3. MRS2 must toggle simultaneously with MRS1.

Figure 5. FIFO2 Master Reset and Loading X2 and Y2 with a Preset Value of Eight (IDT Standard and FWFT Modes)



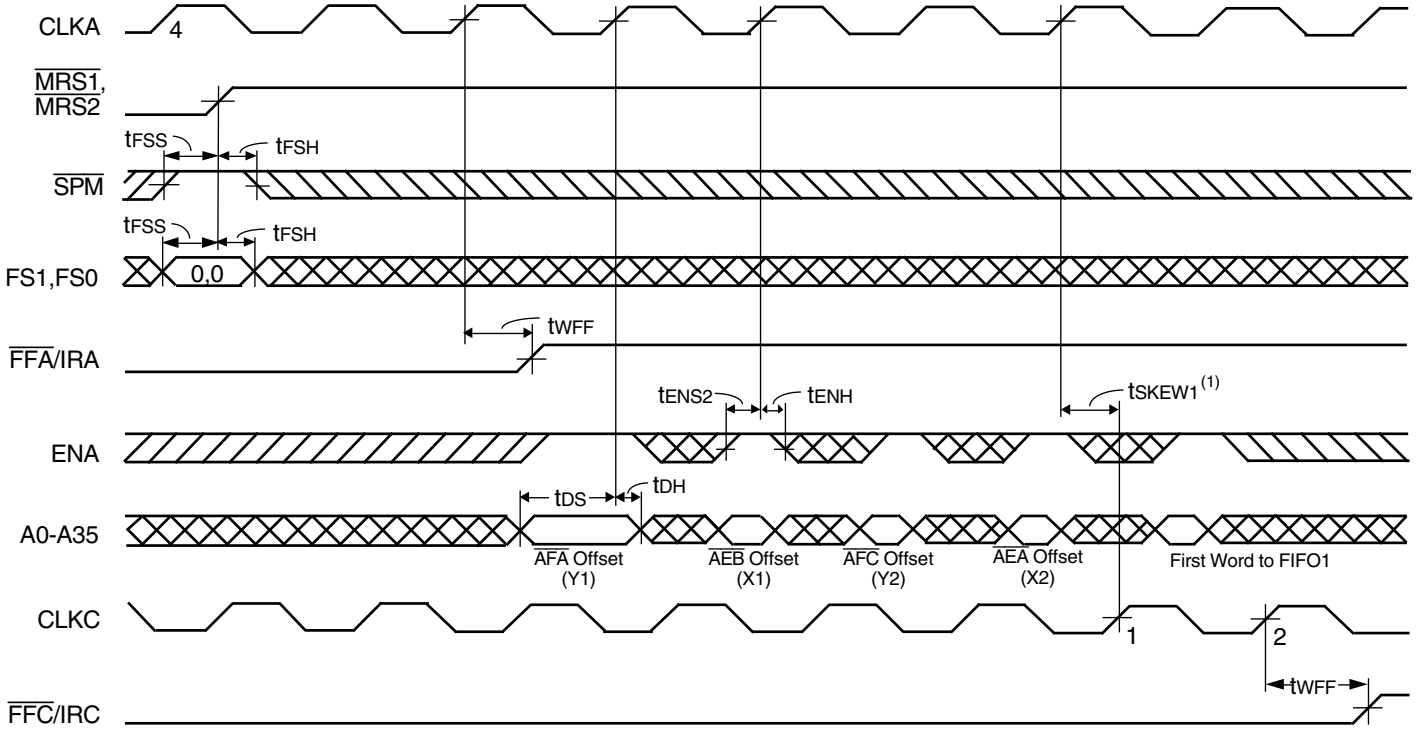
NOTES:
1. $\overline{MRS1}$ must be HIGH during Partial Reset.
2. If BE/$\overline{FWFT}$ is HIGH, then $\overline{EFB}$/ORB will go LOW one CLKB cycle earlier than in this case where BE/$\overline{FWFT}$ is LOW.

Figure 6. FIFO1 Partial Reset (IDT Standard and FWFT Modes)



NOTES:
1. $\overline{MRS2}$ must be HIGH during Partial Reset.
2. If BE/$\overline{FWFT}$ is HIGH, then $\overline{EFA}$/ORA will go LOW one CLKA cycle earlier than in this case where BE/$\overline{FWFT}$ is LOW.

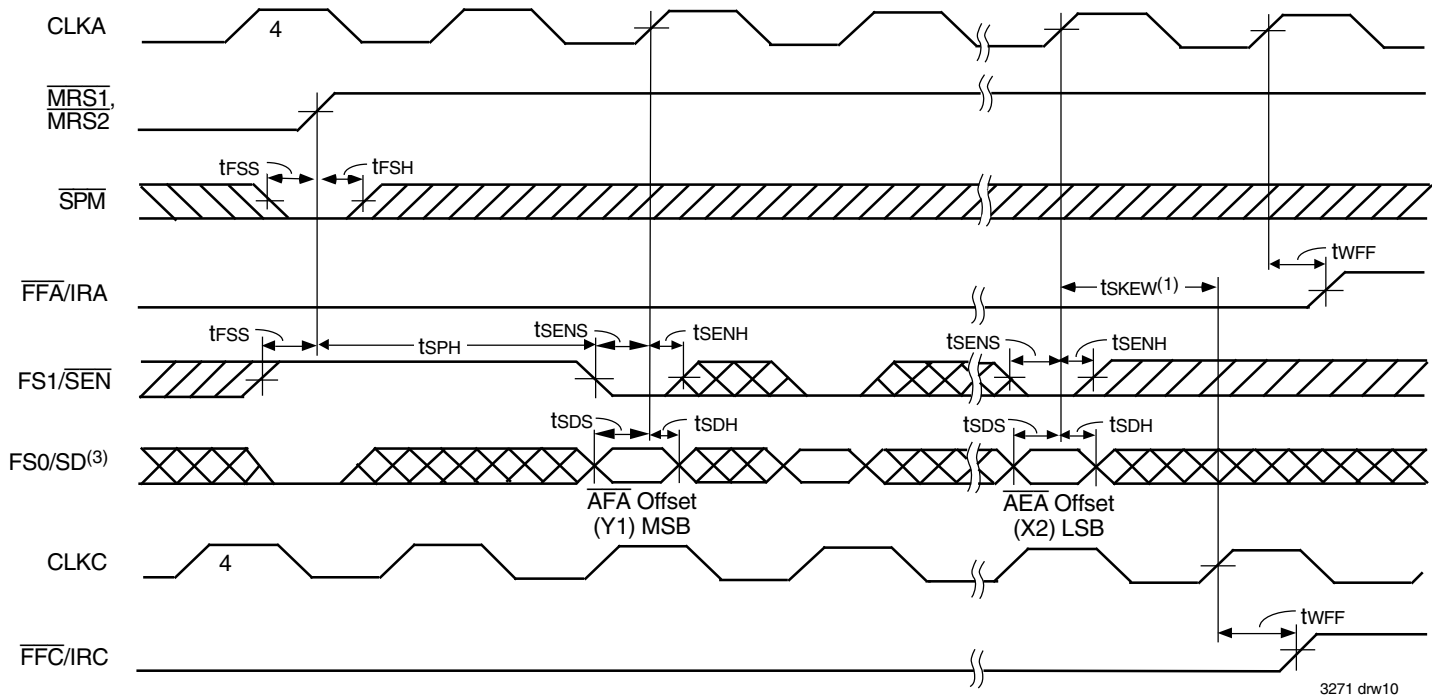
Figure 7. FIFO2 Partial Reset (IDT Standard and FWFT Modes)



NOTES:
3271 drw09

1. t_{SKEW1} is the minimum time between the rising CLKA edge and a rising CLKC edge for $\overline{FFC}$/IRC to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKC is less than t_{SKEW1}, then $\overline{FFC}$/IRC may transition HIGH one CLKC cycle later than shown.
2. $\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW. It is not necessary to program Offset register on consecutive clock cycles.

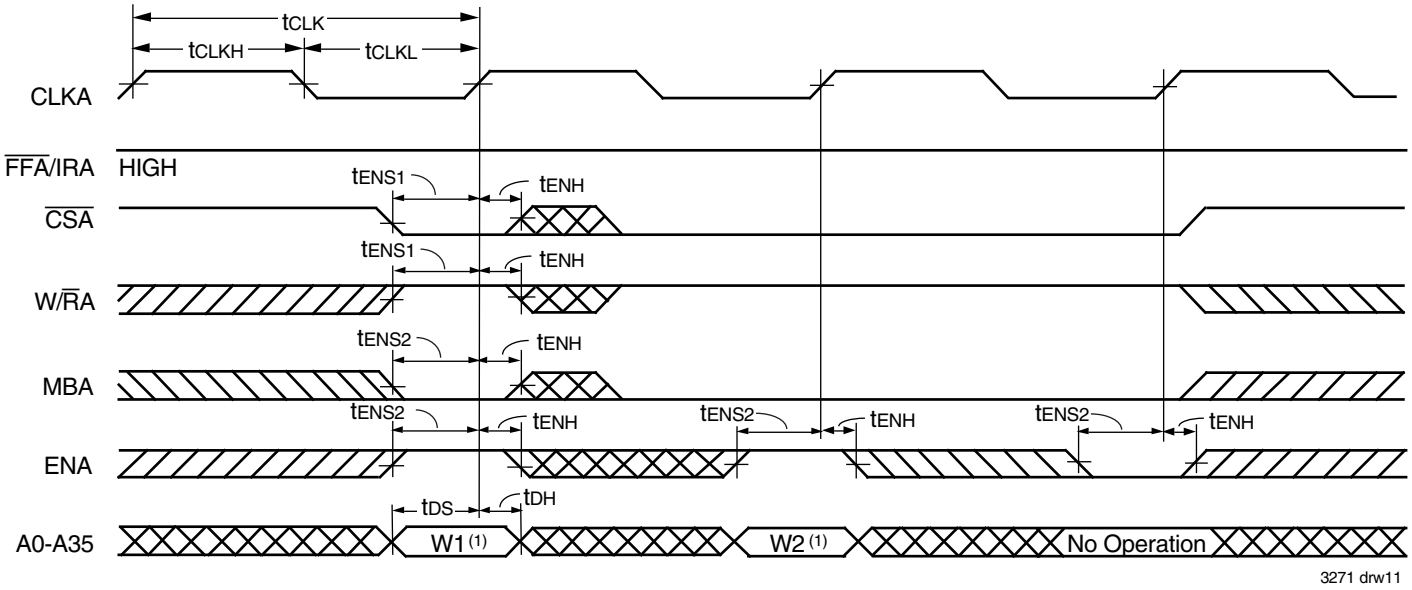
Figure 8. Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)



NOTES:
3271 drw10

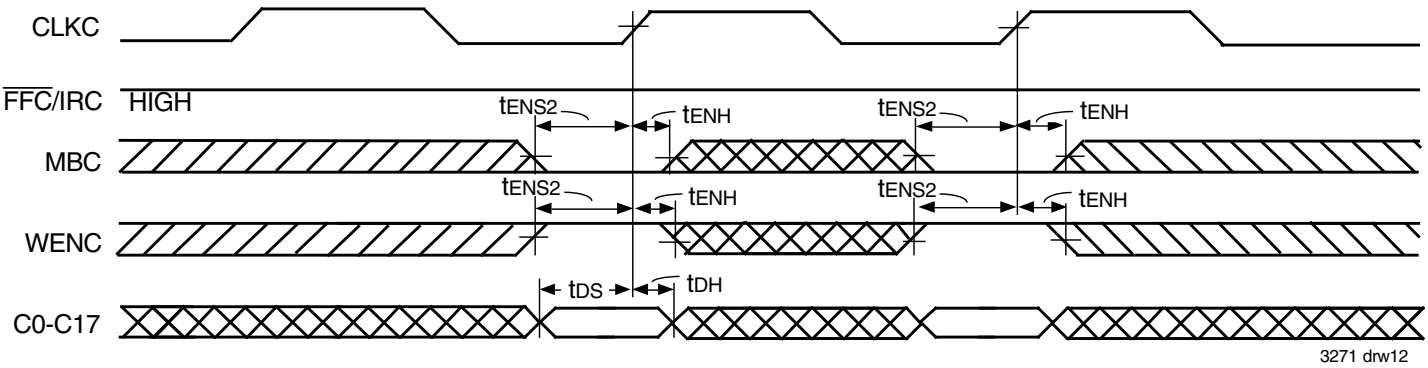
1. t_{SKEW1} is the minimum time between the rising CLKA edge and a rising CLKC edge for $\overline{FFC}$/IRC to transition HIGH in the next cycle. If the time between the rising edge of CLKA and rising edge of CLKC is less than t_{SKEW1}, then $\overline{FFC}$/IRC may transition HIGH one CLKC cycle later than shown.
2. It is not necessary to program Offset register bits on consecutive clock cycles. FIFO write attempts are ignored until $\overline{FFA}$/IRA, $\overline{FFC}$/IRC is set HIGH.
3. Programmable offsets are written serially to the SD input in the order $\overline{AFA}$ offset (Y1), $\overline{AEB}$ offset (X1), $\overline{AFC}$ offset (Y2), and $\overline{AEA}$ offset (X2).

Figure 9. Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)



NOTE:
1. Written to FIFO1.

Figure 10. Port A Write Cycle Timing for FIFO1 (IDT Standard and FWFT Modes)

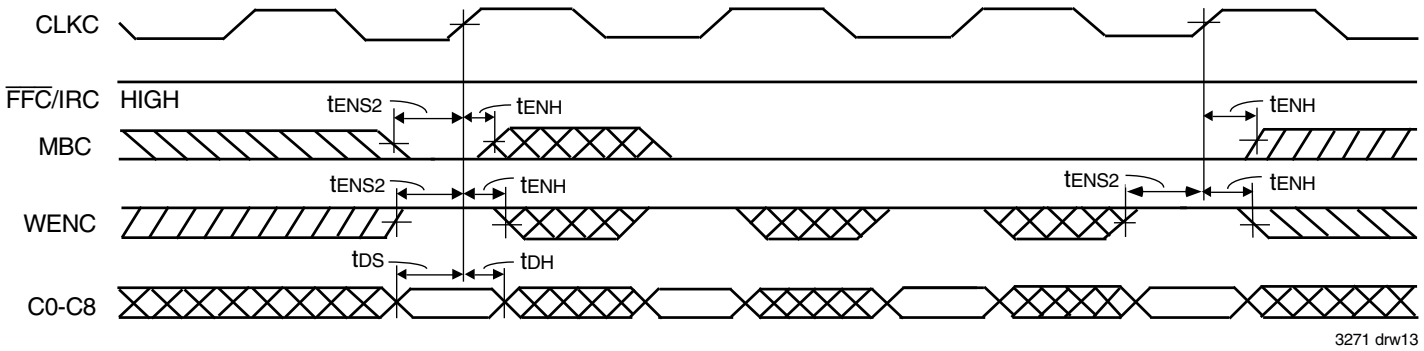


DATA SIZE TABLE FOR WORD WRITES TO FIFO2

SIZE MODE(1)		WRITE NO.	DATA WRITTEN TO FIFO2		DATA READ FROM FIFO2			
SIZEC	BE		C17-C9	C8-C0	A35-A27	A26-A18	A17-A9	A8-A0
L	H	1 2	A C	B D	A	B	C	D
L	L	1 2	C A	D B	A	B	C	D

NOTE:
1. BE is selected at Master Reset; SIZEB and SIZEC must be static throughout device operation.

Figure 11. Port C Word Write Cycle Timing for FIFO2 (IDT Standard and FWFT Modes)

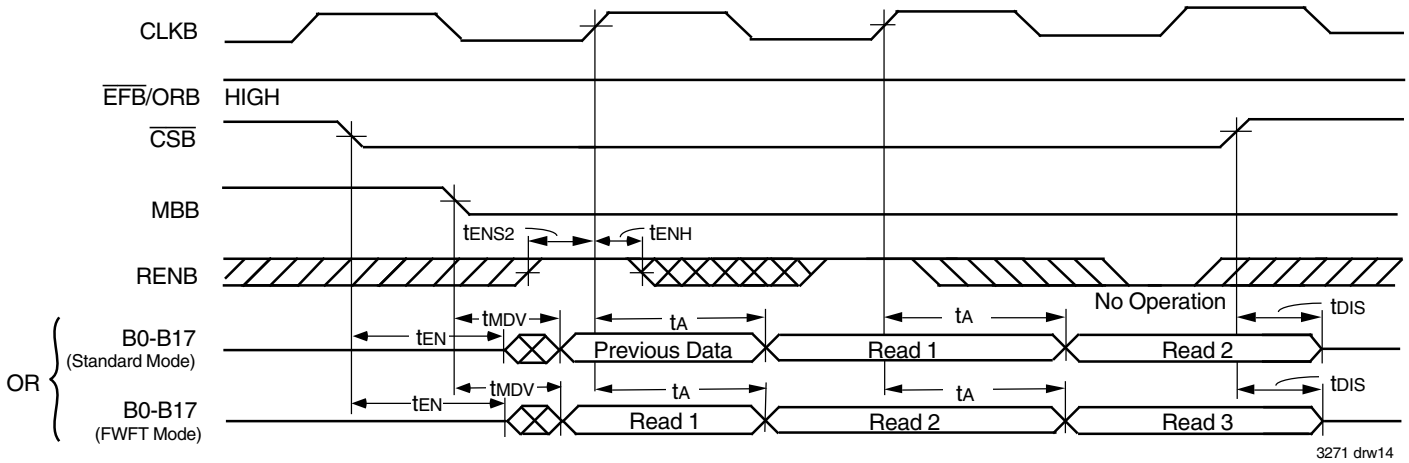


DATA SIZE TABLE FOR BYTE WRITES TO FIFO2

SIZE MODE(1)		WRITE NO.	DATA WRITTEN TO FIFO2	DATA READ FROM FIFO2			
SIZEC	BE		C8-C0	A35-A27	A26-A18	A17-A9	A8-A0
H	H	1	A	A	B	C	D
		2	B				
		3	C				
		4	D				
H	L	1	D	A	B	C	D
		2	C				
		3	B				
		4	A				

NOTE:
1. BE is selected at Master Reset; SIZEB and SIZEC must be static throughout device operation.

Figure 12. Port C Byte Write Cycle Timing for FIFO2 (IDT Standard and FWFT Modes)

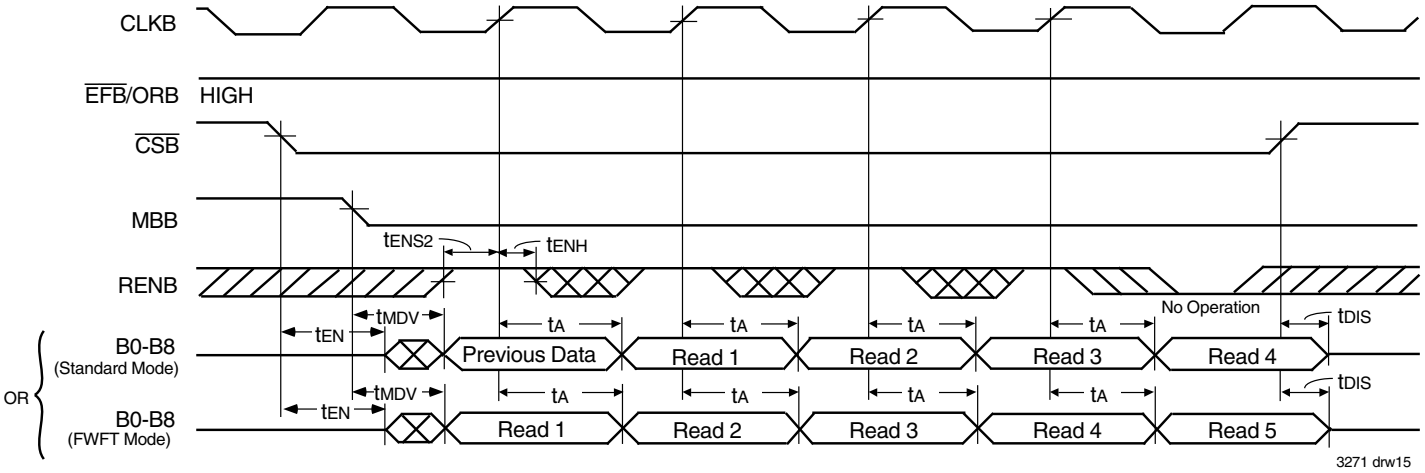


DATA SIZE TABLE FOR WORD READS FROM FIFO1

SIZE MODE(1)		DATA WRITTEN TO FIFO1				READ NO.	DATA READ FROM FIFO1	
SIZEB	BE	A35-A27	A26-A18	A17-A9	A8-A0		B17-B9	B8-B0
H	H	A	B	C	D	1	A	B
						2	C	D
H	L	A	B	C	D	1	C	D
						2	A	B

NOTE:
1. BE is selected at Master Reset; SIZEB and SIZEC must be static throughout device operation.

Figure 13. Port B Word Read Cycle Timing for FIFO1 (IDT Standard and FWFT Modes)



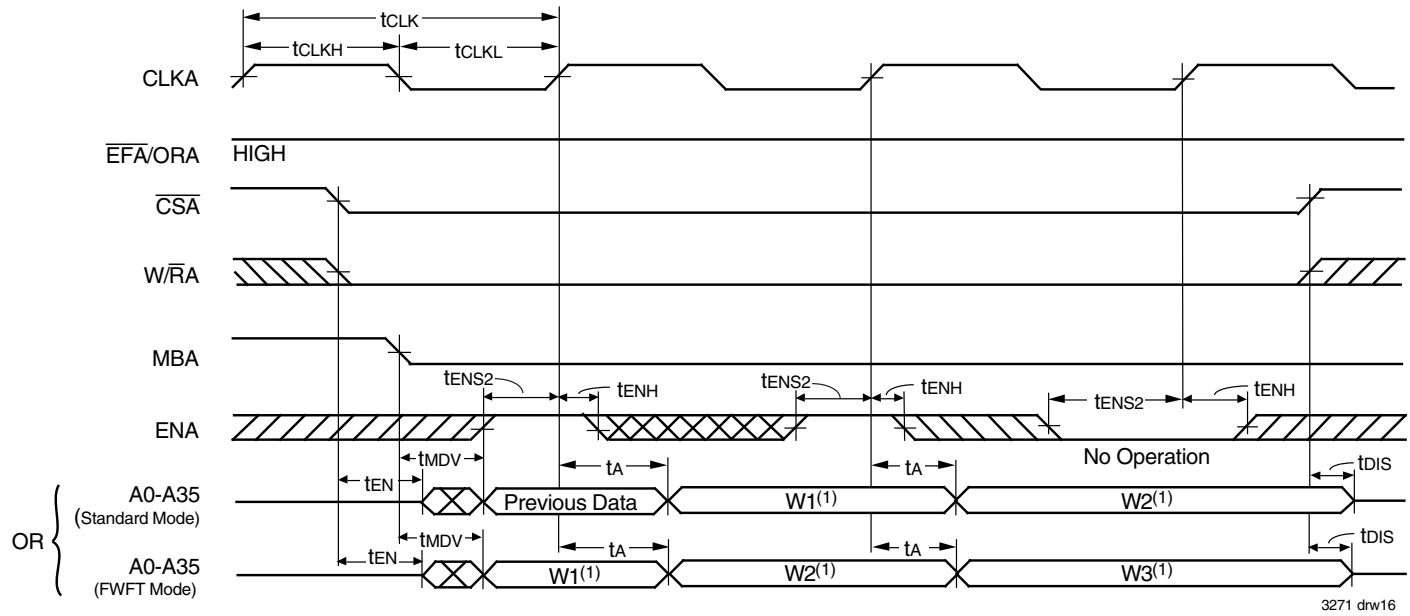
NOTE:
1. Unused bytes B9-B17 are indeterminate for byte-size reads.

DATA SIZE TABLE FOR BYTE READS FROM FIFO1

SIZE MODE(1)		DATA WRITTEN TO FIFO1			READ		DATA READ FROM FIFO1
SIZEB	BE	A35-A27	A26-A18	A17-A9	A8-A0	NO.	B8-B0
H	H	A	B	C	D	1 2 3 4	A B C D
H	L	A	B	C	D	1 2 3 4	D C B A

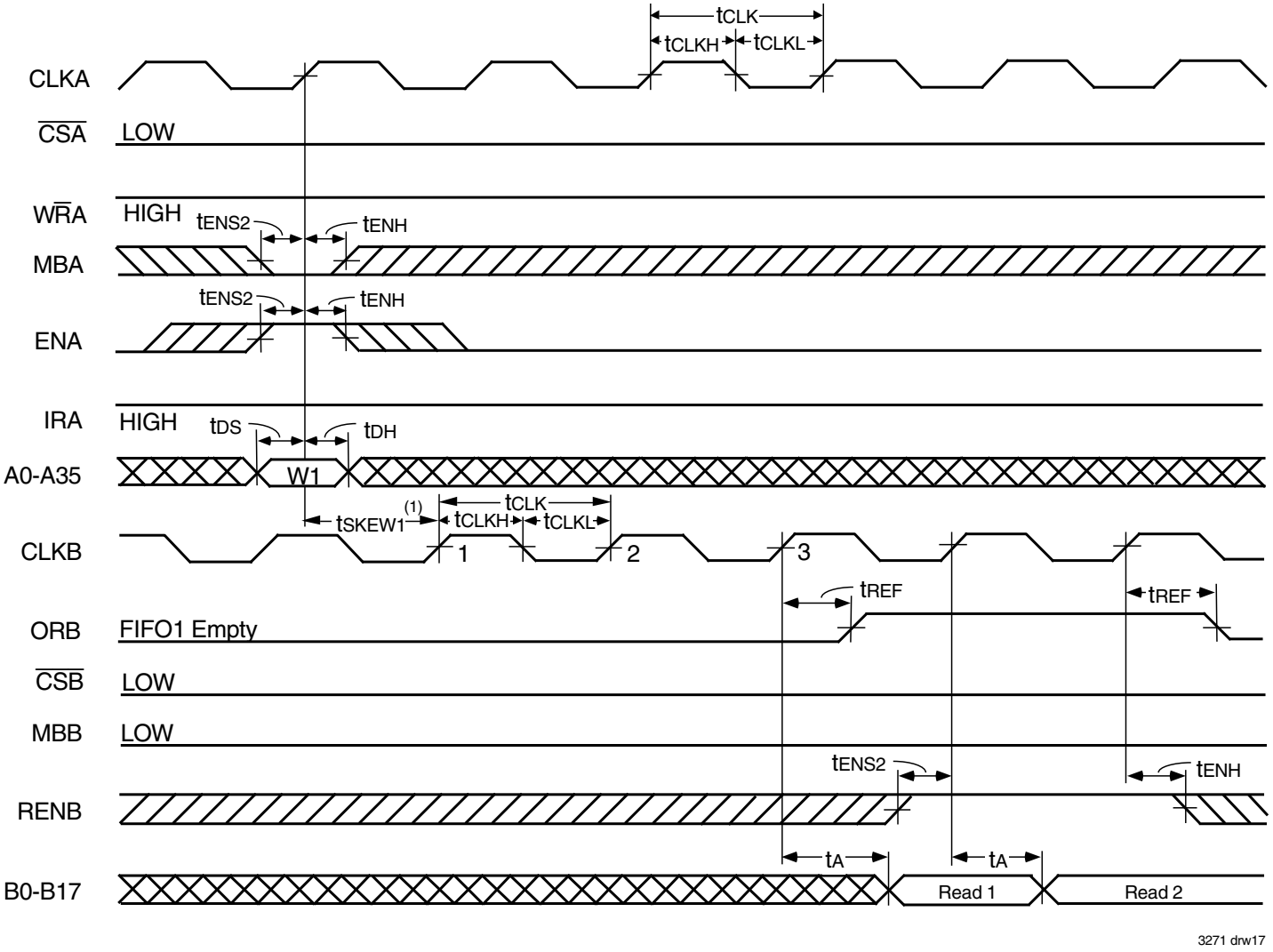
NOTE:
1. BE is selected at Master Reset; SIZEB must be static throughout device operation.

Figure 14. Port B Byte Read Cycle Timing for FIFO1 (IDT Standard and FWFT Modes)



NOTE:
1. Read From FIFO2.

Figure 15. Port A Read Cycle Timing for FIFO2 (IDT Standard and FWFT Modes)

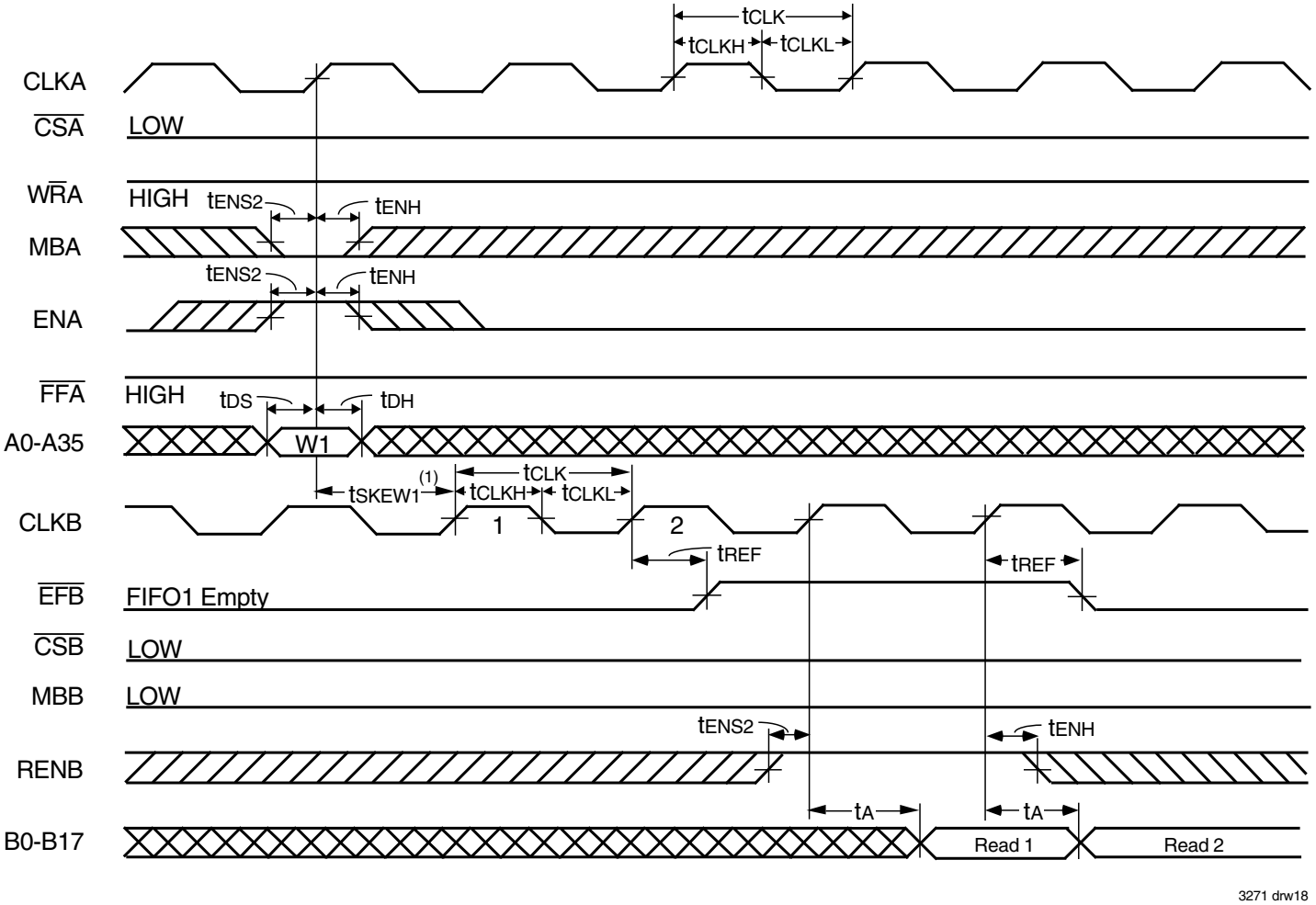


3271 drw17

NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for ORB to transition HIGH and to clock the next word to the FIFO1 output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of ORB HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, ORB is set LOW by the last word or byte read from FIFO1, respectively (the word-size case is shown).

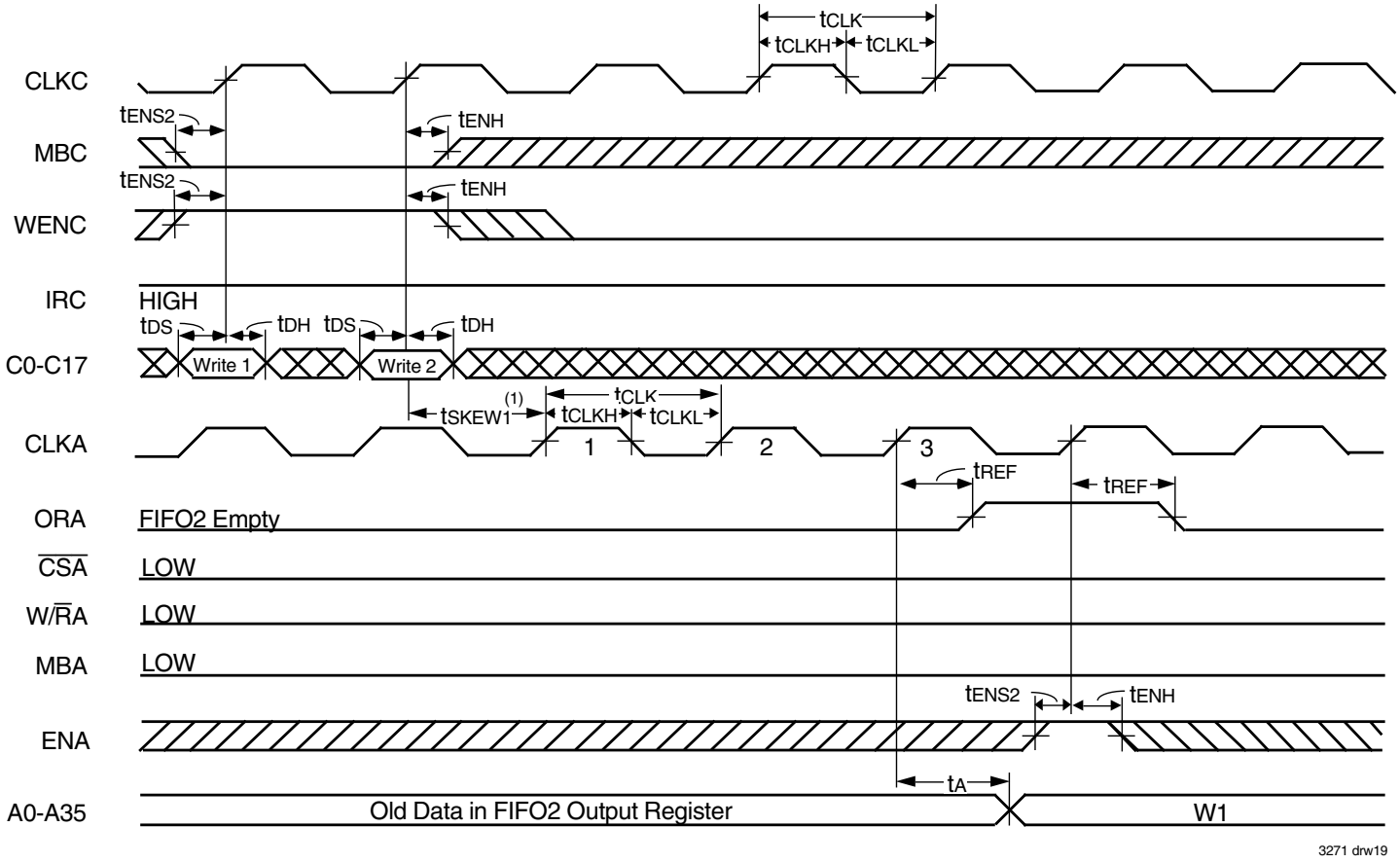
Figure 16. ORB Flag Timing and First Data Word Fall Through when FIFO1 is Empty (FWFT Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{EFB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW1}, then the transition of $\overline{EFB}$ HIGH may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, $\overline{ERB}$ is set LOW by the last word or byte read from FIFO1, respectively (the word-size case is shown).

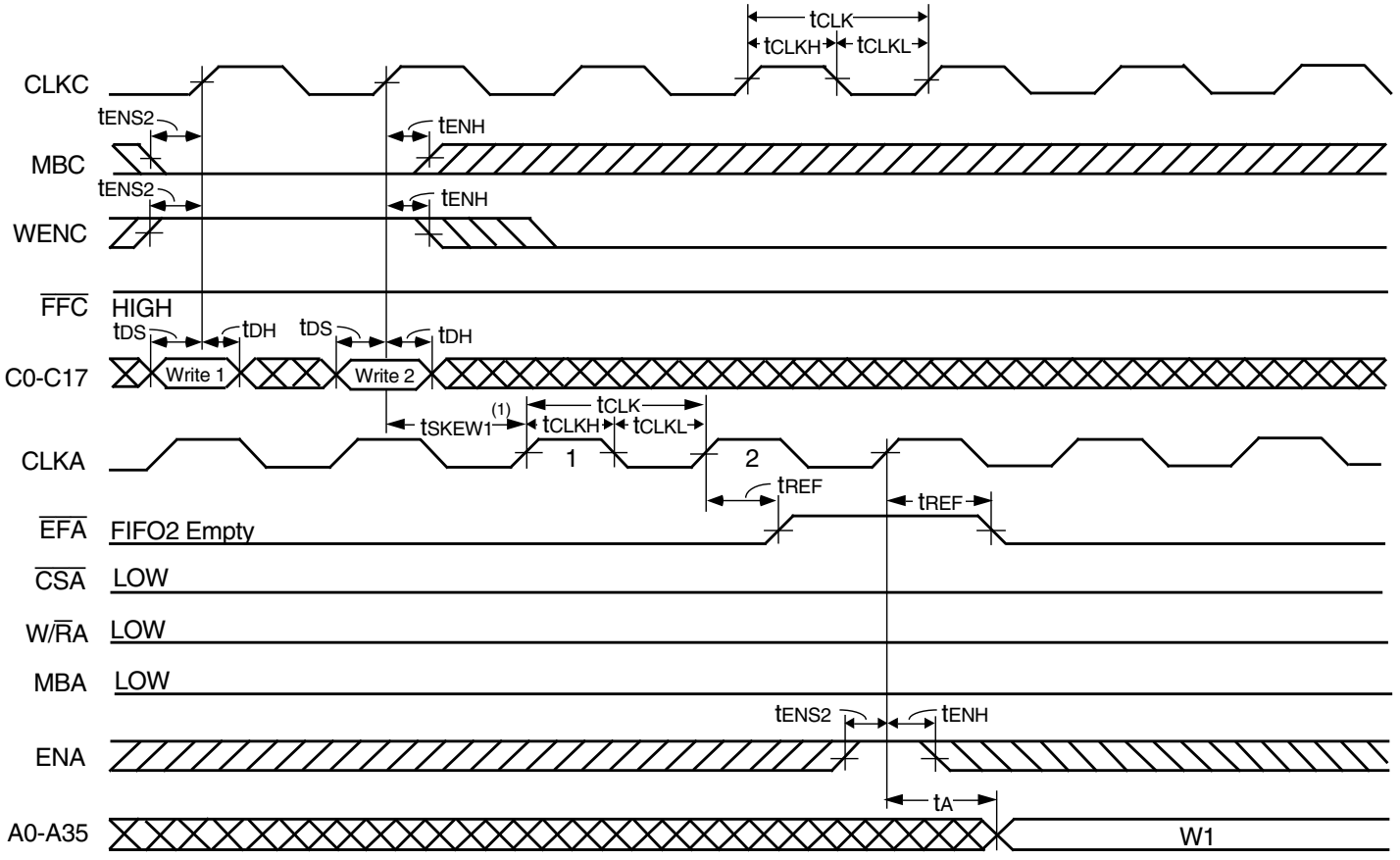
Figure 17. $\overline{EFB}$ Flag Timing and First Data Read Fall Through when FIFO1 is Empty (IDT Standard Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKC edge and a rising CLKA edge for ORA to transition HIGH and to clock the next word to the FIFO2 output register in three CLKA cycles. If the time between the CLKC edge and the rising CLKA edge is less than t_{SKEW1}, then the transition of ORA HIGH and load of the first word to the output register may occur one CLKA cycle later than shown.
2. If Port C size is word or byte, t_{SKEW1} is referenced to the rising CLKC edge that writes the last word or byte write of the long word, respectively.

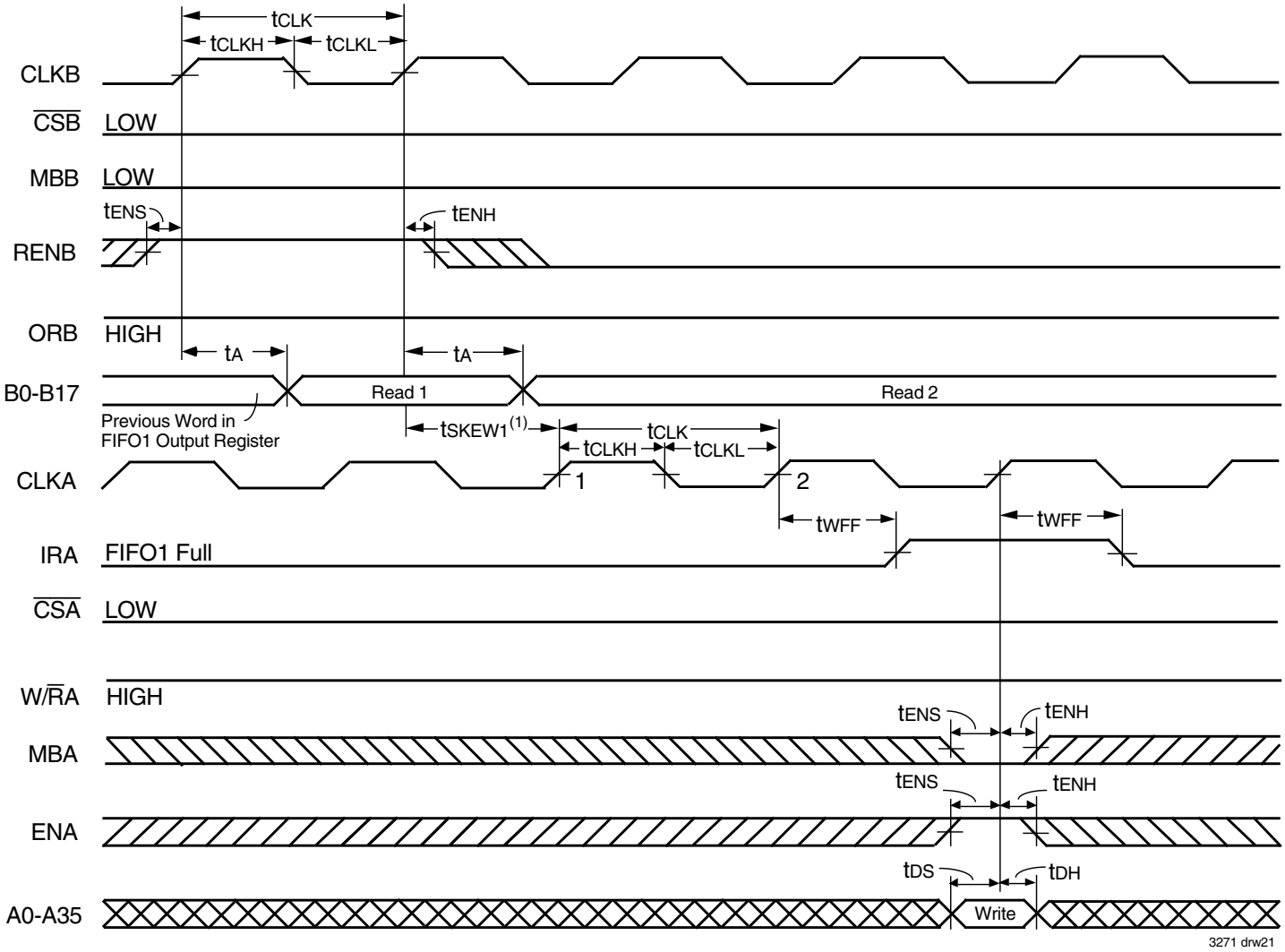
Figure 18. ORA Flag Timing and First Data Word Fall through when FIFO2 is Empty (FWFT Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKC edge and a rising CLKA edge for $\overline{EFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKC edge and rising CLKA edge is less than t_{SKEW1}, then the transition of $\overline{EFA}$ HIGH may occur one CLKA cycle later than shown.
2. If Port C size is word or byte, t_{SKEW1} is referenced to the rising CLKC edge that writes the last word or byte of the long word, respectively.

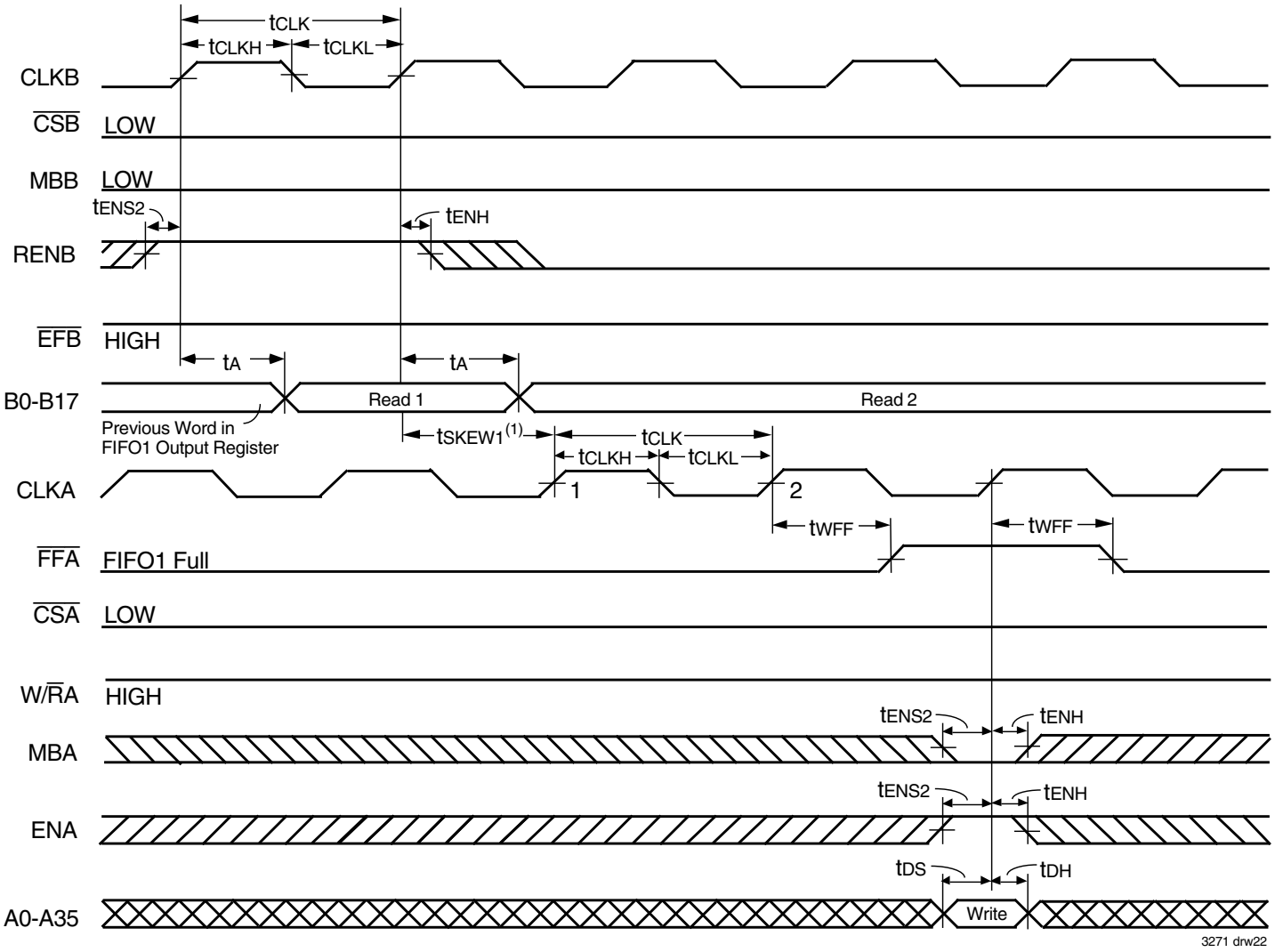
Figure 19. $\overline{EFA}$ Flag Timing and First Data Read when FIFO2 is Empty (IDT Standard Mode)



NOTE:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for IRA to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then IRA may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, t_{SKEW1} is referenced to the rising CLKB edge that reads the last word or byte write of the long word, respectively (the word-size case is shown).

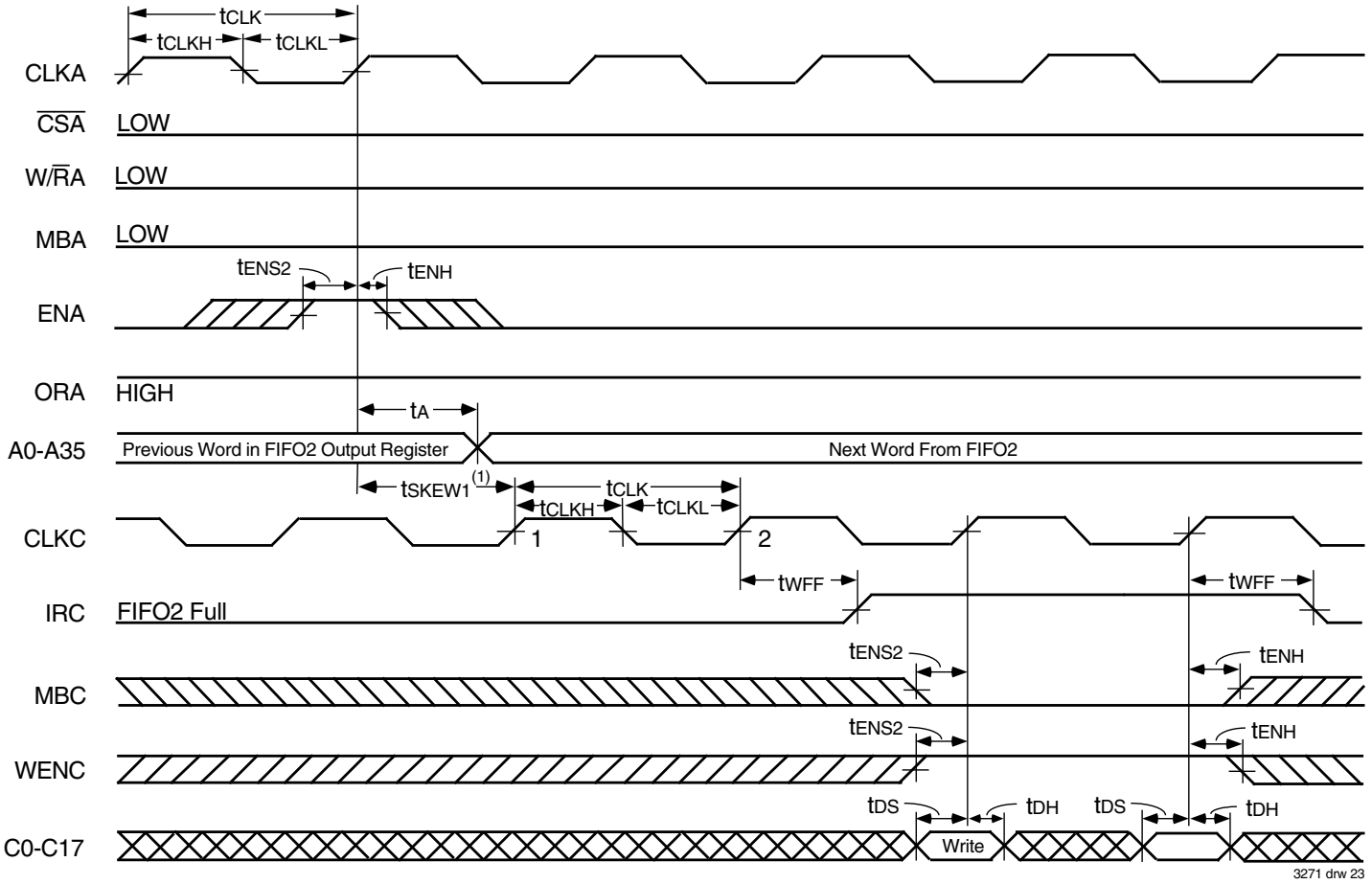
Figure 20. IRA Flag Timing and First Available Write when FIFO1 is Full (FWFT Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKB edge and a rising CLKA edge for $\overline{FFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than t_{SKEW1}, then $\overline{FFA}$ may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, t_{SKEW1} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively (the word-size case is shown).

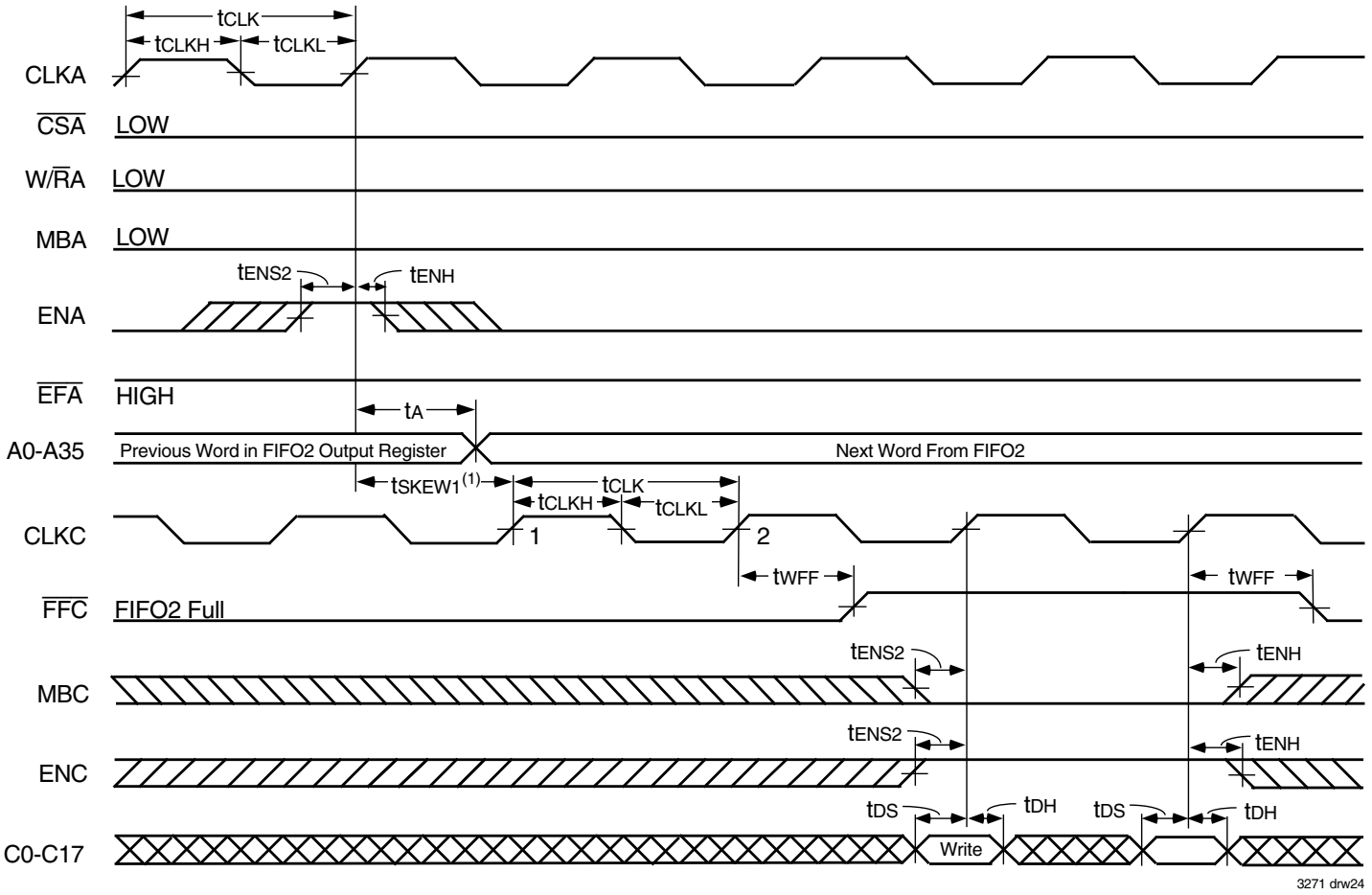
Figure 21. $\overline{FFA}$ Flag Timing and First Available Write when FIFO1 is Full (IDT Standard Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising CLKC edge and a rising CLKC edge for IRC to transition HIGH in the next CLKC cycle. If the time between the rising CLKA edge and rising CLKC edge is less than t_{SKEW1}, then IRC may transition HIGH one CLKC cycle later than shown.
2. If Port C size is word or byte, IRC is set LOW by the last word or byte write of the long word, respectively (the word-size case is shown).

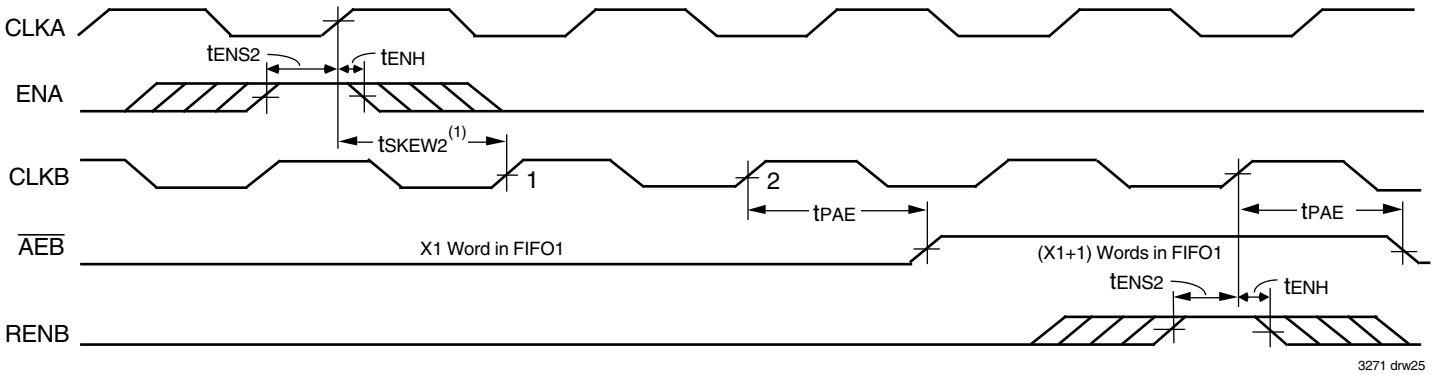
Figure 22. IRC Flag Timing and First Available Write when FIFO2 is Full (FWFT Mode)



NOTES:

1. tSKEW1 is the minimum time between a rising CLKA edge and a rising CLKC edge for $\overline{FFC}$ to transition HIGH in the next CLKC cycle. If the time between the rising CLKA edge and rising CLKC edge is less than tSKEW1, then $\overline{FFC}$ may transition HIGH one CLKC cycle later than shown.
2. If Port C size is word or byte, $\overline{FFC}$ is set LOW by the last word or byte write of the long word, respectively (the word-size case is shown).

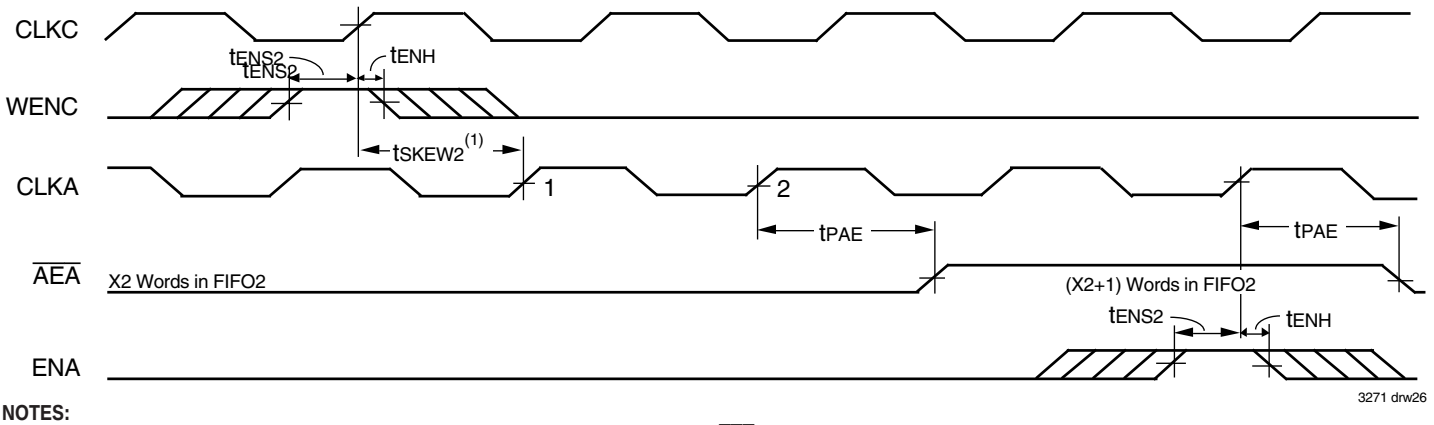
Figure 23. $\overline{FFC}$ Flag Timing and First Available Write when FIFO2 is Full (IDT Standard Mode)



NOTES:

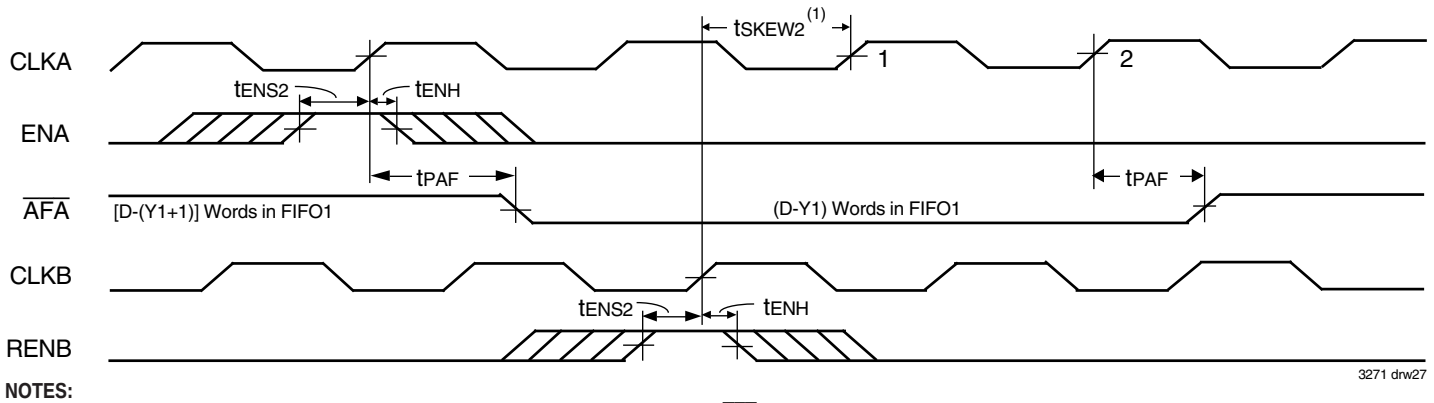
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AEB}$ to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then $\overline{AEB}$ may transition HIGH one CLKB cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
3. If Port B size is word or byte, $\overline{AEB}$ is set LOW by the last word or byte read from FIFO1, respectively.

Figure 24. Timing for $\overline{AEB}$ when FIFO1 is Almost-Empty (IDT Standard and FWFT Modes)



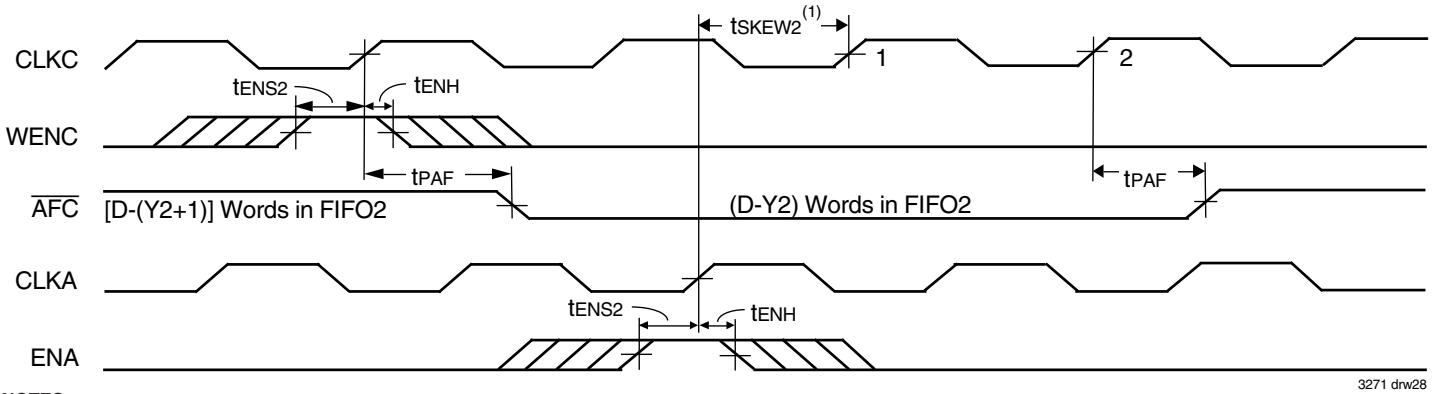
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKC edge and a rising CLKA edge for $\overline{AEA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKC edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AEA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO2 Write (MBC = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.
3. If Port C size is word or byte, t_{SKEW2} is referenced to the rising CLKC edge that writes the last word or byte of the long word, respectively.

Figure 25. Timing for $\overline{AEA}$ when FIFO2 is Almost-Empty (IDT Standard and FWFT Modes)



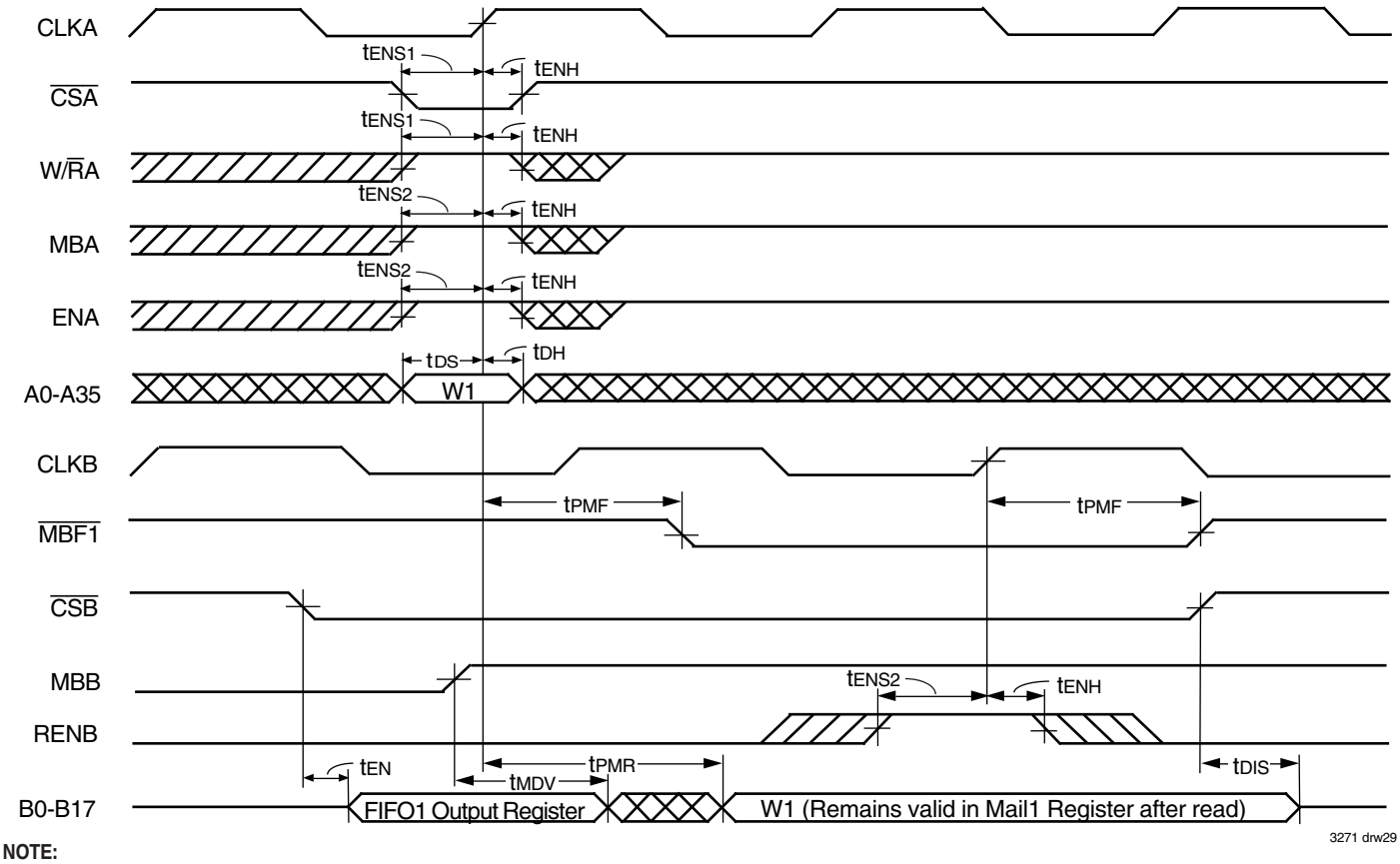
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKA edge and a rising CLKB edge for $\overline{AFA}$ to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than t_{SKEW2}, then $\overline{AFA}$ may transition HIGH one CLKA cycle later than shown.
2. FIFO1 Write ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = HIGH, MBA = LOW), FIFO1 read ($\overline{CSB}$ = LOW, MBB = LOW). Data in the FIFO1 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 256 for the IDT723626, 512 for the IDT723636, 1,024 for the IDT723646.
4. If Port B size is word or byte, t_{SKEW2} is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

Figure 26. Timing for $\overline{AFA}$ when FIFO1 is Almost-Full (IDT Standard and FWFT Modes)



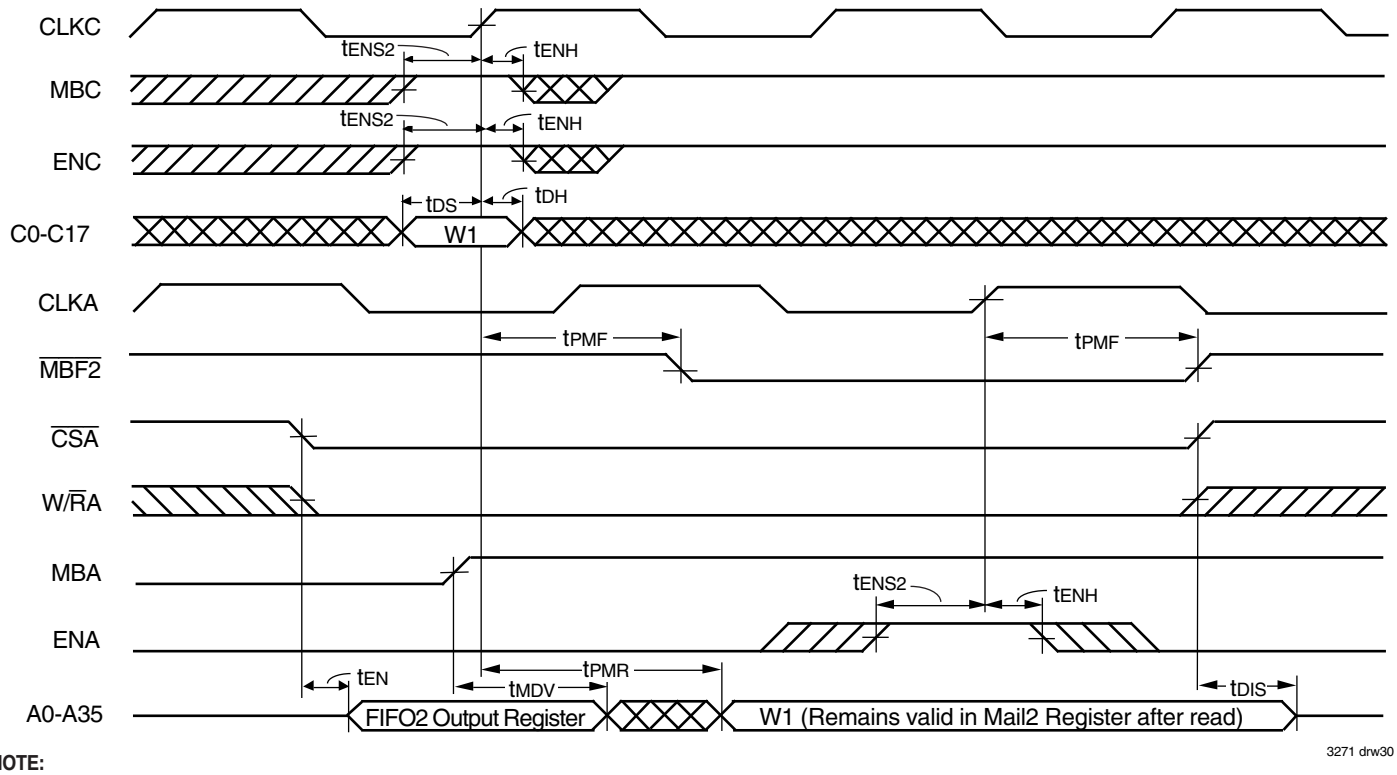
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLKC edge and a rising CLKA edge for $\overline{AFC}$ to transition HIGH in the next CLKC cycle. If the time between the rising CLKC edge and rising CLKA edge is less than t_{SKEW2}, then $\overline{AFC}$ may transition HIGH one CLKC cycle later than shown.
2. FIFO2 write (MBC = LOW), FIFO2 read ($\overline{CSA}$ = LOW, W/$\overline{RA}$ = LOW, MBA = LOW). Data in the FIFO2 output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 256 for the IDT723626, 512 for the IDT723636, 1,024 for the IDT723646.
4. Port C size is word or byte, $\overline{AFC}$ is set LOW by the last word or byte write of the long word, respectively.

Figure 27. Timing for $\overline{AFC}$ when FIFO2 is Almost-Full (IDT Standard and FWFT Modes)



NOTE:
1. If Port B is configured for word size, data can be written to the Mail1 register using A0-A17 (A18-A35 are don't care inputs). In this first case B0-B17 will have valid data. If Port B is configured for byte size, data can be written to the Mail1 Register using A0-A8 (A9-A35 are don't care inputs). In this second case, B0-B8 will have valid data (B9-B17 will be indeterminate).

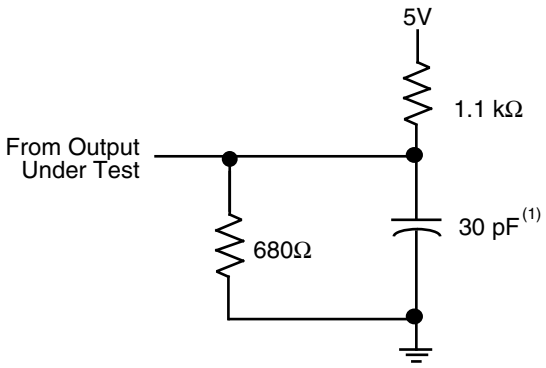
Figure 28. Timing for Mail1 Register and $\overline{\text{MBF1}}$ Flag (IDT Standard and FWFT Modes)



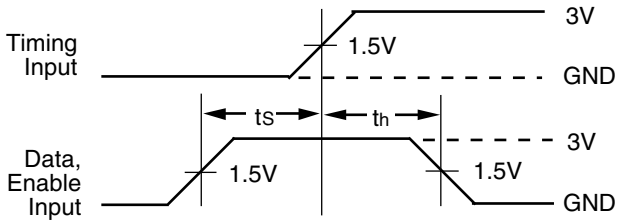
NOTE:
1. If Port C is configured for word size, data can be written to the Mail2 register using C0-C17. In this first case, A18-A35 will have valid data (A0-A17 will be indeterminate). If Port C is configured for byte size, data can be written to the Mail2 register using C0-C8 (C9-C17 are don't care inputs). In this second case, A18-A26 will have valid data (A0-A17 and A27-A35 will be indeterminate).

Figure 29. Timing for Mail2 Register and $\overline{\text{MBF2}}$ Flag (IDT Standard and FWFT Modes)

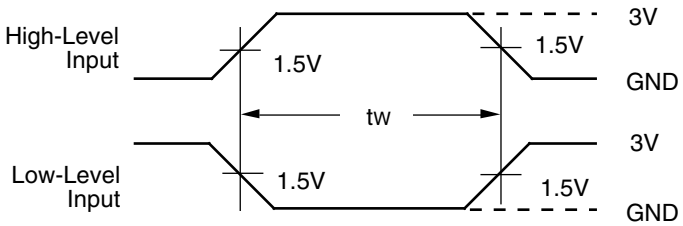
PARAMETER MEASUREMENT INFORMATION



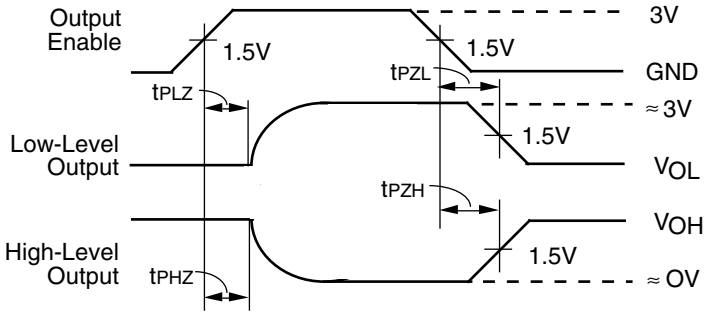
**PROPAGATION DELAY
LOAD CIRCUIT**



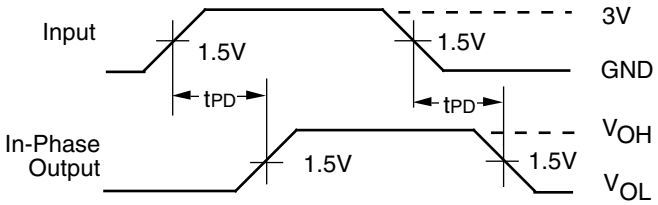
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES**



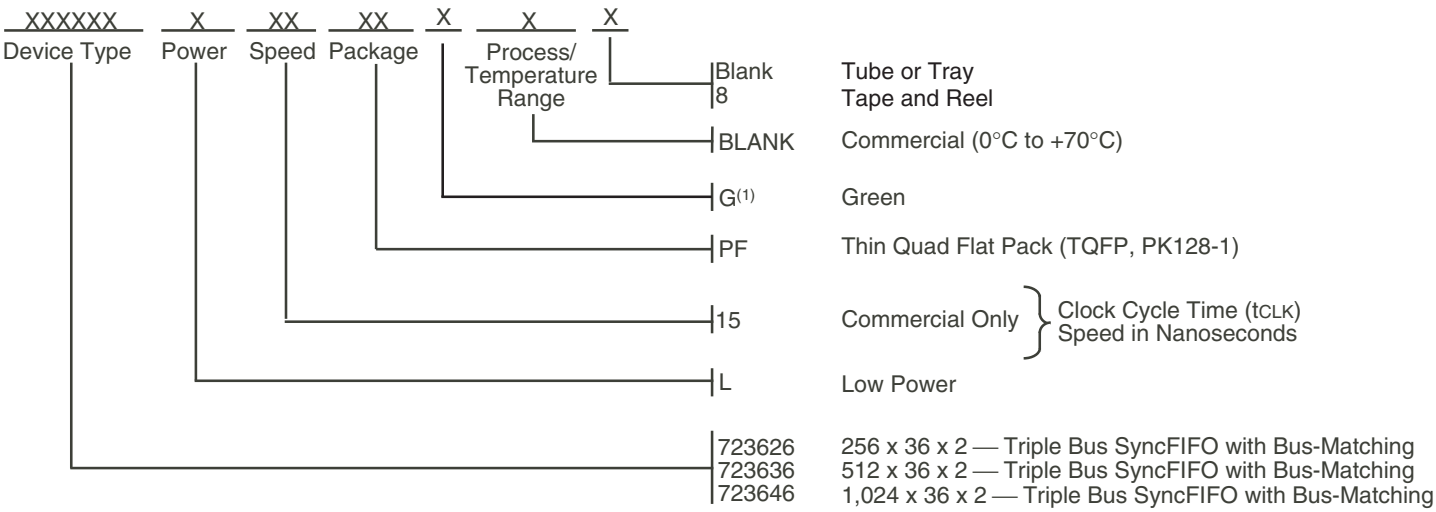
**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**

3271 drw31

NOTE:
1. Includes probe and jig capacitance.

Figure 30. Load Circuit and Voltage Waveforms

ORDERING INFORMATION



3271 drw32

NOTE:

1. Green parts are available. For specific speeds and packages please contact your sales office.
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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
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Contact Information

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