FEATURES:
- Industry’s largest FIFO memory organization: IDT72T36135 — 524,288 x 36 - 18M-bits
- Up to 200 MHz Operation of Clocks
- Functionally and pin compatible to 9Mbit IDT72T36125 TeraSync devices
- User selectable HSTL/LVTTL Input and/or Output
- User selectable Asynchronous read and/or write port timing
- Mark & Retransmit, resets read pointer to user marked position
- Write Chip Select (WCS) input disables Write Port
- Read Chip Select (RCS) synchronous to RCLK
- Programmable Almost-Empty and Almost-Full flags, each flag can default to one of eight preselected offsets
- Program programmable flags by either serial or parallel means
- Selectable synchronous/asynchronous timing modes for Almost-Empty and Almost-Full flags
- Separate SCLK input for Serial programming of flag offsets
- Auto power down minimizes standby power consumption
- Master Reset clears entire FIFO
- Partial Reset clears data, but retains programmable settings
- Empty and Full flags signal FIFO status
- Select IDT Standard timing (using EF[1:2] and FF[1:2] flags) or First Word Fall Through timing (using OR[1:2] and IR[1:2] flags)
- Output enables put data outputs into high impedance state
- JTAG port, provided for Boundary Scan function
- Available in 240-pin (19mm x 19mm) Plastic Ball Grid Array (PBGA) 50% more space saving than the leading 9M-bit FIFOs
- Independent Read and Write Clocks (permit reading and writing simultaneously)
- High-performance submicron CMOS technology
- Industrial temperature range (–40°C to +85°C) is available
- Green parts available, see ordering information

FUNCTIONAL BLOCK DIAGRAM

INPUT REGISTER
OFFSET REGISTER
RAM ARRAY 524,288 x 36
FLAG LOGIC
WRITE CONTROL LOGIC
WRITE POINTER
OFFSET REGISTER
READ CONTROL LOGIC
READ POINTER
OUTPUT REGISTER
HSTL I/O CONTROL
RESET LOGIC
JTAG CONTROL (BOUNDARY SCAN)
INPUT REGISTER
OFFSET REGISTER
RAM ARRAY 524,288 x 36
FLAG LOGIC
WRITE CONTROL LOGIC
WRITE POINTER
OFFSET REGISTER
READ CONTROL LOGIC
READ POINTER
OUTPUT REGISTER
HSTL I/O CONTROL
RESET LOGIC
JTAG CONTROL (BOUNDARY SCAN)
**PIN CONFIGURATION**

**NOTE:**
1. DNC - Do Not Connect.

**PBGA:** 1mm pitch, 19mm x 19mm (BB240, order code: BB)

**TOP VIEW**
DESCRIPTION:

The IDT72T36135M is an exceptionally deep, extremely high speed, CMOS First-In-First-Out (FIFO) memory with clocked read and write controls and a wide extended x36 bus to allow ample data flow. These FIFOs offer several key user benefits:

- High density offering of 18 Mbit
- 200MHz R/W Clocks supporting 7.2Gbps of data throughput
- User selectable MARK location for retransmit
- User selectable I/O structure for HSTL or LVTTL
- Asynchronous/Synchronous translation on the read or write ports
- The first word data latency period, from the time the first word is written to an empty FIFO to the time it can be read, is fixed and short.

TeraSync FIFOs are particularly appropriate for network, video, telecommunications, data communications and other applications that need to buffer large amounts of data at very high performance.

The input port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the input port is controlled by a Write Clock (WCLK) input and a Write Enable (WEN) input. Data present on the Dn data inputs is written into the FIFO on every rising edge of WCLK when WEN is asserted. During Asynchronous operation only the WR input is used to write data into the FIFO. Data is written on a rising edge of WR, the WEN input should be tied to its active state, (LOW).

The input port can be selected for either 2.5V LVTTL or HSTL operation, this operation is selected by the state of the WHSTL input during a master reset. A Write Chip Select input (WCS) is provided for use when the write port is in both LVTTL and HSTL modes. During operation the WCS input can be used to disable write port inputs (data only).

The output port can be selected as either a Synchronous (clocked) interface, or Asynchronous interface. During Synchronous operation the output port is controlled by a Read Clock (RCLK) input and Read Enable (REN) input. Data is read from the FIFO on every rising edge of RCLK when REN is asserted. During Asynchronous operation only the RD input is used to read data from the FIFO. Data is read on a rising edge of RD, the REN input should be tied to its active state, LOW. When Asynchronous operation is selected on the output port the FIFO must be configured for Standard IDT mode, also the RCS should be tied LOW and the OE input used to provide three-state control of the outputs, Qn.

The output port can be selected for either 2.5V LVTTL or HSTL operation, this operation is selected by the state of the RHSTL input during a master reset. An Output Enable (OE) input is provided for three-state control of the outputs. A Read Chip Select (RCS) input is also provided, the RCS input is synchronized to the read clock, and also provides three-state control of the Qn data outputs. When RCS is disabled, the data outputs will be high impedance. During Asynchronous operation of the output port, RCS should be enabled, held LOW.

The frequencies of both the RCLK and the WCLK signals may vary from 0 to fMAX with complete independence. There are no restrictions on the frequency of the one clock input with respect to the other.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall Through (FWFT) mode.

In **IDT Standard mode**, the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating REN and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines.

In **FWFT mode**, the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A REN does not have to be asserted for accessing the first word. However, subsequent words written to the FIFO do require a LOW on REN for access. The state of the FWFT/SI input during Master Reset determines the timing mode in use.

For applications requiring more data storage capacity than a single FIFO can provide, the FWFT timing mode permits depth expansion by chaining FIFOs in series (i.e. the data outputs of one FIFO are connected to the corresponding data inputs of the next). No external logic is required.

The 18M-bit TeraSync FIFO has 8 flag pins, EF/OR[1:2] (Empty Flag or Output Ready), FF/IR[1:2] (Full Flag or Input Ready), PAE[1:2] (Programmable Almost-Empty flag) and PAF[1:2] (Programmable Almost-Full flag). The EF[1:2] and FF[1:2] functions are selected in IDT Standard mode. The IR[1:2] and OR[1:2] functions are selected in FWFT mode. PAE[1:2] and PAF[1:2] are always available for use, irrespective of timing mode. Each flag has a double because the 18M FIFO was designed as a Multi-chip Module, so each set of flags supports its respective internal 9M FIFO. Some extra external gating logic will have to be used to accurately read each flag output. This will be covered in the flagging section of the datasheet.

PAE[1:2] and PAF[1:2] can be programmed independently to switch at any point in memory. Programmable offsets determine the flag switching threshold and can be loaded by two methods: parallel or serial. Eight default offset settings are also provided, so that PAE[1:2] can be set to switch at a predefined number of locations from the empty boundary and the PAF[1:2] threshold can also be set at similar predefined values from the full boundary. The default offset values are set during Master Reset by the state of the FSELO, FSEL1, and LD pins.

For serial programming, SEN together with LD on each rising edge of SCLK, are used to load the offset registers via the Serial Input (SI). For parallel programming, SEN together with LD on each rising edge of WCLK, are used to load the offset registers via Dn. REN together with LD on each rising edge of RCLK can be used to read the offsets in parallel from Qn regardless of whether serial or parallel offset loading has been selected.

During Master Reset (MRS) the following events occur: the read and write pointers are set to the first location of the FIFO. The FWFT pin selects IDT Standard mode or FWFT mode.

The Partial Reset (PRS) also sets the read and write pointers to the first location of the memory. However, the timing mode, programmable flag programming method, and default or programmed offset settings existing before Partial Reset remain unchanged. The flags are updated according to the timing mode and offsets in effect. PRS is useful for resetting a device in mid-operation, when reprogramming programmable flags would be undesirable.

It is also possible to select the timing mode of the PAE[1:2] (Programmable Almost-Empty flag) and PAF[1:2] (Programmable Almost-Full flag) outputs. The timing modes can be set to be either asynchronous or synchronous for the PAE[1:2] and PAF[1:2] flags.

If asynchronous PAE/PAF[1:2] configuration is selected, the PAE[1:2] is asserted LOW on the LOW-to-HIGH transition of RCLK. PAE[1:2] is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the PAF[1:2] is asserted LOW on the LOW-to-HIGH transition of WCLK and PAF[1:2] is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous PAE/PAF[1:2] configuration is selected, the PAE[1:2] is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, PAF[1:2] is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during Master Reset by the state of the Programmable Flag Mode (PFM) pin.

This device includes a Retransmit from Mark feature that utilizes two control inputs, MARK and RT (Retransmit). If the MARK input is enabled with respect to the RCLK, the memory location being read at that point will be marked. Any subsequent retransmit operation, RT goes LOW, will reset the read pointer to this ‘marked’ location.

If, at any time, the FIFO is not actively performing an operation, the chip will automatically power down. Once in the power down state, the standby supply current consumption is minimized. Initiating any operation (by activating control
DESCRIPTION (CONTINUED)

Both an Asynchronous Output Enable pin (OE) and Synchronous Read Chip Select pin (RCS) are provided on the FIFO. The Synchronous Read Chip Select is synchronized to the RCLK. Both the output enable and read chip select control the output buffer of the FIFO, causing the buffer to be either HIGH impedance or LOW impedance.

A JTAG test port is provided, here the FIFO has fully functional Boundary Scan feature, compliant with IEEE 1449.1 Standard Test Access Port and Boundary Scan Architecture. Special consideration should be taken into account for JTAG testing since the device is a MCM. Please see JTAG section for further details.

The TeraSync FIFO has the capability of operating its ports (write and/or read) in either LVTTL or HSTL mode, each ports selection independent of the other. The write port selection is made via WHSTL and the read port selection via RHSTL. An additional input HSTL is also provided, this allows the user to select HSTL operation for other pins on the device (not associated with the write or read ports).

The IDT72T36135M is fabricated using high speed submicron CMOS technology.
Figure 1. Single Device Configuration Signal Flow Diagram
# PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name</th>
<th>I/O TYPE</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ĀSYR</td>
<td>Asynchronous Read Port</td>
<td>LVTTL</td>
<td>A HIGH on this input during Master Reset will select Synchronous read operation for the output port. A LOW will select Asynchronous operation. If Asynchronous is selected the FIFO must operate in IDT Standard mode.</td>
</tr>
<tr>
<td>ĀSYW</td>
<td>Asynchronous Write Port</td>
<td>LVTTL</td>
<td>A HIGH on this input during Master Reset will select Synchronous write operation for the input port. A LOW will select Asynchronous operation.</td>
</tr>
<tr>
<td>D0–D35</td>
<td>Data Inputs</td>
<td>HSTL-LVTT</td>
<td>Data inputs for a 36-bit bus.</td>
</tr>
<tr>
<td>EF/ OR</td>
<td>Empty Flag/Output Ready</td>
<td>HSTL-LVTT</td>
<td>In the IDT Standard mode, the EF[1:2] function is selected. EF[1:2] indicates whether or not the FIFO memory is empty. In FWT mode, the OR[1:2] function is selected. OR[1:2] indicates whether or not there is valid data available at the outputs. Please see Flagging section for external gating instructions of these flags.</td>
</tr>
<tr>
<td>FF/IR</td>
<td>Full Flag/Input Ready</td>
<td>HSTL-LVTT</td>
<td>In the IDT Standard mode, the FF[1:2] function is selected. FF[1:2] indicates whether or not the FIFO memory is full. In the FWFT mode, the IR[1:2] function is selected. IR[1:2] indicates whether or not there is space available for writing to the FIFO memory. Please see Flagging section for external gating instructions of these flags.</td>
</tr>
<tr>
<td>FSEL0</td>
<td>Flag Select Bit 0</td>
<td>LVTTL</td>
<td>During Master Reset, this input along with FSEL1 and the LD pin, will select the default offset values for the programmable flags PAE[1:2] and PAF[1:2]. There are up to eight possible settings available.</td>
</tr>
<tr>
<td>FSEL1</td>
<td>Flag Select Bit 1</td>
<td>LVTTL</td>
<td>During Master Reset, this input along with FSEL0 and the LD pin will select the default offset values for the programmable flags PAE[1:2] and PAF[1:2]. There are up to eight possible settings available.</td>
</tr>
<tr>
<td>FWFT/ SI</td>
<td>First Word Fall Through/Serial In</td>
<td>HSTL-LVTT</td>
<td>During Master Reset, selects First Word Fall Through or IDT Standard mode. After Master Reset, this pin functions as a serial input for loading offset registers. If Asynchronous operation of the read port has been selected then the FIFO must be set-up in IDT Standard mode.</td>
</tr>
<tr>
<td>LD</td>
<td>Load</td>
<td>HSTL-LVTT</td>
<td>This is a dual purpose pin. During Master Reset, the state of the LD input along with FSEL0 and FSEL1, determines one of eight default offset values for the PAE[1:2] and PAF[1:2]flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 1). After Master Reset, this pin enables writing to and reading from the offset registers.</td>
</tr>
<tr>
<td>MARK</td>
<td>Mark for Retransmit</td>
<td>HSTL-LVTT</td>
<td>When this pin is asserted the current location of the read pointer will be marked. Any subsequent Retransmit operation will reset the read pointer to this position.</td>
</tr>
<tr>
<td>MRS</td>
<td>Master Reset</td>
<td>HSTL-LVTT</td>
<td>MRS initializes the read and write pointers to zero and sets the output register to all zeroes. During Master Reset, the FIFO is configured for either FWFT or IDT Standard mode. Synchronous/Asynchronous operation of the read or write port, one of eight programmable flag default settings, serial or parallel programming of the offset settings, zero latency timing mode, and synchronous versus asynchronous programmable flag timing modes.</td>
</tr>
<tr>
<td>ŸOE</td>
<td>Output Enable</td>
<td>HSTL-LVTT</td>
<td>ŸOE provides Asynchronous three-state control of the data outputs, Qn. During a Master or Partial Reset the ŸOE input is the only input that provide High-Impedance control of the data outputs.</td>
</tr>
<tr>
<td>PAE[1:2]</td>
<td>Programmable Almost-Empty Flag</td>
<td>HSTL-LVTT</td>
<td>PAE[1:2] goes LOW if the number of words in the FIFO memory is less than offset n, which is stored in the Empty Offset register. PAE[1:2] goes HIGH if the number of words in the FIFO memory is greater than or equal to offset n. Please see Flagging section for external gating instructions of these flags.</td>
</tr>
<tr>
<td>PAF[1:2]</td>
<td>Programmable Almost-Full Flag</td>
<td>HSTL-LVTT</td>
<td>PAF[1:2] goes HIGH if the number of free locations in the FIFO memory is more than offset m, which is stored in the Full Offset register. PAF[1:2] goes LOW if the number of free locations in the FIFO memory is less than or equal to m. Please see Flagging section for external gating instructions of these flags.</td>
</tr>
<tr>
<td>PFM</td>
<td>Programmable Flag Mode</td>
<td>LVTTL</td>
<td>During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode.</td>
</tr>
<tr>
<td>PRS</td>
<td>Partial Reset</td>
<td>HSTL-LVTT</td>
<td>PRS initializes the read and write pointers to zero and sets the output register to all zeroes. During Partial Reset, the existing mode (IDT or FWFT), programming method (serial or parallel), and programmable flag settings are all retained.</td>
</tr>
<tr>
<td>Q0–Q35</td>
<td>Data Outputs</td>
<td>HSTL-LVTT</td>
<td>Data outputs for an 36-bit bus.</td>
</tr>
<tr>
<td>RCLK/ RD</td>
<td>Read Clock/Read Stobe</td>
<td>HSTL-LVTT</td>
<td>If Synchronous operation of the read port has been selected, when enabled by REN, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers. If LD is LOW, the values loaded into the offset registers is output on a rising edge of RCLK. If Asynchronous operation of the read port has been selected, when enabled by REN, the rising edge of RCLK reads data from the FIFO memory and offsets from the programmable registers.</td>
</tr>
</tbody>
</table>
### PIN DESCRIPTION (CONTINUED)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name</th>
<th>I/O TYPE</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RCLK/ RD</td>
<td>Read Clock/Read Strobe</td>
<td>HSTL-LVTTL INPUT</td>
<td>port has been selected, a rising edge on RD reads data from the FIFO in an Asynchronous manner. REN should be tied LOW.</td>
</tr>
<tr>
<td>RCS</td>
<td>Read Chip Select</td>
<td>HSTL-LVTTL INPUT</td>
<td>RCS provides synchronous control of the read port and output impedance of Qn, synchronous to RCLK. During a Master Reset or Partial Reset the RCS input is don't care, if OE is LOW the output will be Low-Impedance regardless of RCS.</td>
</tr>
<tr>
<td>REN</td>
<td>Read Enable</td>
<td>HSTL-LVTTL INPUT</td>
<td>If Synchronous operation of the read port has been selected, REN enables RCLK for reading data from the FIFO memory and offset registers. If Asynchronous operation of the read port has been selected, the REN input should be tied LOW.</td>
</tr>
<tr>
<td>RHSTL(1)</td>
<td>Read Port HSTL Select</td>
<td>LVTTL INPUT</td>
<td>This pin is used to select HSTL or 2.5v LVTTL outputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW.</td>
</tr>
<tr>
<td>RT</td>
<td>Retransmit</td>
<td>HSTL-LVTTL INPUT</td>
<td>RT asserted on the rising edge of RCLK initializes the READ pointer to zero, sets the EF[1:2] flag to LOW (OR[1:2] to HIGH in FWFT mode) and doesn't disturb the write pointer, programming method, existing timing mode or programmable flag settings. If a mark has been set via the MARK input pin, then the read pointer will jump to the 'mark' location.</td>
</tr>
<tr>
<td>SCLK</td>
<td>Serial Clock</td>
<td>HSTL-LVTTL INPUT</td>
<td>A rising edge on SCLK will clock the serial data present on the SI input into the offset registers providing that SEN is enabled.</td>
</tr>
<tr>
<td>SEN</td>
<td>Serial Enable</td>
<td>HSTL-LVTTL INPUT</td>
<td>SEN enables serial loading of programmable flag offsets.</td>
</tr>
<tr>
<td>SHSTL</td>
<td>System HSTL Select</td>
<td>LVTTL INPUT</td>
<td>All inputs not associated with the write or read port can be selected for HSTL operation via the SHSTL input.</td>
</tr>
<tr>
<td>TCK(2)</td>
<td>JTAG Clock</td>
<td>HSTL-LVTTL INPUT</td>
<td>Clock input for JTAG function. TMS and TDI are sampled on the rising edge of TCK. Data is output on TDO on the falling edge.</td>
</tr>
<tr>
<td>TRST(2)</td>
<td>JTAG Reset</td>
<td>HSTL-LVTTL INPUT</td>
<td>TRST is an asynchronous reset pin for the JTAG controller.</td>
</tr>
<tr>
<td>TMS</td>
<td>JTAG Mode Select</td>
<td>HSTL-LVTTL INPUT</td>
<td>TMS is a serial input pin. Bits are serially loaded on the rising edge of TCK, which selects 1 of 5 modes of operation for the JTAG boundary scan.</td>
</tr>
<tr>
<td>TDI</td>
<td>Test Data Input</td>
<td>HSTL-LVTTL INPUT</td>
<td>During JTAG boundary scan operation test data is serially loaded via TDI on the rising edge of TCK.</td>
</tr>
<tr>
<td>TDO</td>
<td>Test Data Output</td>
<td>HSTL-LVTTL OUTPUT</td>
<td>During JTAG boundary scan operation test data is serially output via TDO on the falling edge of TCK.</td>
</tr>
<tr>
<td>WEN</td>
<td>Write Enable</td>
<td>HSTL-LVTTL INPUT</td>
<td>When Synchronous operation of the write port has been selected, WEN enables WCLK for writing data into the FIFO memory and offset registers. If Asynchronous operation of the write port has been selected, the WEN input should be tied LOW.</td>
</tr>
<tr>
<td>WCS</td>
<td>Write Chip Select</td>
<td>HSTL-LVTTL INPUT</td>
<td>This pin disables the write port data inputs when the device write port is configured for HSTL mode. This provides added power savings.</td>
</tr>
<tr>
<td>WCLK/ WR</td>
<td>Write Clock/Write Strobe</td>
<td>HSTL-LVTTL INPUT</td>
<td>If Synchronous operation of the write port has been selected, when enabled by WEN, the rising edge of WCLK writes data into the FIFO. If Asynchronous operation of the write port has been selected, WR writes data into the FIFO on a rising edge in an Asynchronous manner. (WEN should be tied to its active state).</td>
</tr>
<tr>
<td>WHSTL(1)</td>
<td>Write Port HSTL Select</td>
<td>LVTTL INPUT</td>
<td>This pin is used to select HSTL or 2.5v LVTTL inputs for the FIFO. If HSTL inputs are required, this input must be tied HIGH. Otherwise it should be tied LOW.</td>
</tr>
<tr>
<td>Vcc</td>
<td>+2.5v Supply</td>
<td>Power</td>
<td>These are Vcc supply inputs and must be connected to the 2.5V supply rail.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground Pin</td>
<td>GND</td>
<td>These are Ground pins and must be connected to the GND rail.</td>
</tr>
<tr>
<td>Vref</td>
<td>Reference Voltage</td>
<td>I</td>
<td>This is a Voltage Reference input and must be connected to a voltage level determined from the table, “Recommended DC Operating Conditions”. This provides the reference voltage when using HSTL class inputs. If HSTL class inputs are not being used, this pin should be tied LOW.</td>
</tr>
<tr>
<td>VDDQ</td>
<td>O/P Rail Voltage</td>
<td>I</td>
<td>This pin should be tied to the desired voltage rail for providing power to the output drivers.</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Inputs should not change state after Master Reset.
2. If the JTAG feature is not being used, TCK and TRST should be tied LOW.
## ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Commercial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTERM</td>
<td>Terminal Voltage with respect to GND</td>
<td>–0.5 to +3.6(2)</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>–55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>–50 to +50</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Compliant with JEDEC JESD8-5. VCC terminal only.

## CAPACITANCE \( T_A = +25\degree C, f = 1.0\text{MHz} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter(1)</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN(2,3)</td>
<td>Input Capacitance</td>
<td>V_N = 0V</td>
<td>15(3)</td>
<td>pF</td>
</tr>
<tr>
<td>COUT(1,2)</td>
<td>Output Capacitance</td>
<td>V_OUT = 0V</td>
<td>10.5</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTES:**
1. With output deselected, \((\overline{OE} \geq V_{IL})\).
2. Characterized values, not currently tested.
3. Cn for Vref is 40pF.

## RECOMMENDED DC OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>Supply Voltage</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage</td>
<td>1.7</td>
<td>—</td>
<td>3.45</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— LVTTL</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— eHSTL</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— HSTL</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— VREF+0.2</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— VREF+0.2</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>-0.3</td>
<td>—</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— LVTTL</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— eHSTL</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— HSTL</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— VREF-0.2</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— VREF-0.2</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VREF(1)</td>
<td>Voltage Reference Input</td>
<td>0.8</td>
<td>0.9</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— eHSTL</td>
<td>0.68</td>
<td>0.75</td>
<td>0.9</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>— HSTL</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Commercial</td>
<td>0</td>
<td>—</td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature Industrial</td>
<td>-40</td>
<td>—</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTE:**
1. VREF is only required for HSTL or eHSTL inputs. VREF should be tied LOW for LV TTL operation.
2. Outputs are not 3.3V tolerant.
# DC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 2.5V ± 0.125V, TA = 0°C to +70°C; Industrial: Vcc = 2.5V ± 0.125V, TA = -40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ill</td>
<td>Input Leakage Current</td>
<td>–10</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>Iol</td>
<td>Output Leakage Current</td>
<td>–10</td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>Voh(5)</td>
<td>Output Logic “1” Voltage, $I_{OH} = -8 mA$ @VDDQ = 2.5V ± 0.125V (LVTTL)</td>
<td>VDDQ -0.4</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDQ -0.4</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VDDQ -0.4</td>
<td>—</td>
<td>V</td>
</tr>
<tr>
<td>Vol</td>
<td>Output Logic “0” Voltage, $I_{OL} = 8 mA$ @VDDQ = 2.5V ± 0.125V (LVTTL)</td>
<td>—</td>
<td>0.4V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.4V</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>—</td>
<td>0.4V</td>
<td>V</td>
</tr>
<tr>
<td>Icc1(1)(2)</td>
<td>Active Vcc Current (Vcc = 2.5V)</td>
<td>I/O = LVTTL</td>
<td>120</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O = HSTL</td>
<td>180</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O = eHSTL</td>
<td>180</td>
<td>mA</td>
</tr>
<tr>
<td>Icc2(1)</td>
<td>Standby Vcc Current (Vcc = 2.5V)</td>
<td>I/O = LVTTL</td>
<td>40</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O = HSTL</td>
<td>140</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I/O = eHSTL</td>
<td>140</td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Both WCLK and RCLK toggling at 20MHz. Data inputs toggling at 10MHz. WCS = HIGH, REN or RCS = HIGH.
2. For the IDT72T36135M, typical ICC calculation (with data outputs in Low-impedance):
3. For all devices, typical IDDQ calculation:
   - with data outputs in High-impedance: $IDQ (mA) = 0.15 \times f_s = WCLK = RCLK$ frequency (in MHz)
   - with data outputs in Low-impedance: $IDQ (mA) = (C_L x VDDQ x f_s x N)/2000$
     $f_s = WCLK = RCLK$ frequency (in MHz), $VDDQ = 2.5V$ for LVTTL; $1.5V$ for HSTL; $1.8V$ for eHSTL, $C_L$ = capacitive load (pf), $TA = 25^\circ C$, $N =$ Number of outputs switching.
4. Total Power consumed: $PT = (VCC \times ICC) + VDDQ \times IDDQ$.
5. Outputs are not 3.3V tolerant.
## AC ELECTRICAL CHARACTERISTICS (1) — SYNCHRONOUS TIMING

(Commercial: Vcc = 2.5V ± 5%, TA = 0°C to +70°C; Industrial: Vcc = 2.5V ± 5%, TA = -40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Com’l &amp; Ind’l</th>
</tr>
</thead>
<tbody>
<tr>
<td>tC</td>
<td>Clock Cycle Frequency (Synchronous)</td>
<td>—</td>
<td>166 MHz</td>
</tr>
<tr>
<td>tA</td>
<td>Data Access Time</td>
<td>0.6 — 3.6 ns</td>
<td>0.6 — 3.8 ns</td>
</tr>
<tr>
<td>tCLK</td>
<td>Clock Cycle Time</td>
<td>5 — 6 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tCH</td>
<td>Clock High Time</td>
<td>2.5 — 3.0 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tCL</td>
<td>Clock Low Time</td>
<td>2.5 — 3.0 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tCS</td>
<td>Data Setup Time</td>
<td>1.5 — 2.0 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tCH</td>
<td>Data Hold Time</td>
<td>0.5 — 0.5 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tENS</td>
<td>Enable Setup Time</td>
<td>1.5 — 2.0 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tENH</td>
<td>Enable Hold Time</td>
<td>0.5 — 0.5 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tDS</td>
<td>Load Setup Time</td>
<td>1.5 — 2.0 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tDH</td>
<td>Load Hold Time</td>
<td>0.5 — 0.5 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tWCS</td>
<td>WCS setup time</td>
<td>1.5 — 2.0 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tWCSH</td>
<td>WCS hold time</td>
<td>0.5 — 0.5 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>fS</td>
<td>Clock Cycle Frequency (SCLK)</td>
<td>— 10 MHz</td>
<td>— 10 MHz</td>
</tr>
<tr>
<td>tSCLK</td>
<td>Serial Clock Cycle</td>
<td>100 — 100 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tSCH</td>
<td>Serial Clock High</td>
<td>45 — 45 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tSCL</td>
<td>Serial Clock Low</td>
<td>45 — 45 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tSDS</td>
<td>Serial Data In Setup</td>
<td>15 — 15 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tSDH</td>
<td>Serial Data In Hold</td>
<td>5 — 5 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tSENS</td>
<td>Serial Enable Setup</td>
<td>5 — 5 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tSENH</td>
<td>Serial Enable Hold</td>
<td>5 — 5 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tRS</td>
<td>Reset Pulse Width(3)</td>
<td>10 — 10 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tRSS</td>
<td>Reset Setup Time</td>
<td>15 — 15 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tRSTS</td>
<td>HSTL Reset Setup Time</td>
<td>4 — 4 μs</td>
<td>— μs</td>
</tr>
<tr>
<td>tRSR</td>
<td>Reset Recovery Time</td>
<td>10 — 10 ns</td>
<td>— ns</td>
</tr>
<tr>
<td>tRSF</td>
<td>Reset to Flag and Output Time</td>
<td>— 15 ns</td>
<td>— 15 ns</td>
</tr>
<tr>
<td>tWFF</td>
<td>Write Clock to FF[1:2] or IR[1:2]</td>
<td>— 3.6 ns</td>
<td>— 3.7 ns</td>
</tr>
<tr>
<td>tREF</td>
<td>Read Clock to EF[1:2] or OR[1:2]</td>
<td>— 3.6 ns</td>
<td>— 3.7 ns</td>
</tr>
<tr>
<td>tPAFS</td>
<td>Write Clock to Synchronous PA[1:2]</td>
<td>— 3.6 ns</td>
<td>— 3.7 ns</td>
</tr>
<tr>
<td>tPAES</td>
<td>Read Clock to Synchronous PAE[1:2]</td>
<td>— 3.6 ns</td>
<td>— 3.7 ns</td>
</tr>
<tr>
<td>tRCLZ</td>
<td>RCLK to Active from High-Z(3)</td>
<td>— 3.6 ns</td>
<td>— 3.7 ns</td>
</tr>
<tr>
<td>tRCHZ</td>
<td>RCLK to High-Z(3)</td>
<td>— 3.6 ns</td>
<td>— 3.7 ns</td>
</tr>
<tr>
<td>tSKW1</td>
<td>Skew time between RCLK and WCLK for EF[1:2] and FF[1:2]</td>
<td>— 4 ns</td>
<td>— 5 ns</td>
</tr>
<tr>
<td>tSKW2</td>
<td>Skew time between RCLK and WCLK for PAE[1:2] and PAF[1:2]</td>
<td>— 5 ns</td>
<td>— 6 ns</td>
</tr>
</tbody>
</table>

### NOTES:
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.
4. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.
### AC ELECTRICAL CHARACTERISTICS — ASYNCHRONOUS TIMING

(Commercial: Vcc = 2.5V ± 5%, TA = 0°C to +70°C; Industrial: Vcc = 2.5V ± 5%, TA = -40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Com’l &amp; Ind’l</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>IDT72T36135ML5</td>
<td>IDT72T36135ML6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Max.</td>
</tr>
<tr>
<td>fA</td>
<td>Cycle Frequency (Asynchronous)</td>
<td>—</td>
<td>83</td>
</tr>
<tr>
<td>tAA</td>
<td>Data Access Time</td>
<td>0.6</td>
<td>10</td>
</tr>
<tr>
<td>tCYC</td>
<td>Cycle Time</td>
<td>12</td>
<td>—</td>
</tr>
<tr>
<td>tOH</td>
<td>Cycle HIGH Time</td>
<td>5</td>
<td>—</td>
</tr>
<tr>
<td>tOL</td>
<td>Cycle LOW Time</td>
<td>5</td>
<td>—</td>
</tr>
<tr>
<td>tPE</td>
<td>Read Pulse after EF[1:2] HIGH</td>
<td>10</td>
<td>—</td>
</tr>
<tr>
<td>tFFA</td>
<td>Clock to Asynchronous FF[1:2]</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tPEFA</td>
<td>Clock to Asynchronous Programmable Almost-Full Flag</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tPAFA</td>
<td>Clock to Asynchronous Programmable Almost-Empty Flag</td>
<td>—</td>
<td>10</td>
</tr>
<tr>
<td>tOLZ</td>
<td>Output Enable to Output in Low Z&lt;sup&gt;3&lt;/sup&gt;</td>
<td>0</td>
<td>—</td>
</tr>
<tr>
<td>tOE</td>
<td>Output Enable to Output Valid</td>
<td>—</td>
<td>3.6</td>
</tr>
<tr>
<td>tOHZ</td>
<td>Output Enable to Output in High Z&lt;sup&gt;3&lt;/sup&gt;</td>
<td>—</td>
<td>3.6</td>
</tr>
<tr>
<td>tHF</td>
<td>Clock to HF</td>
<td>—</td>
<td>10</td>
</tr>
</tbody>
</table>

**NOTES:**
1. All AC timings apply to both Standard IDT mode and First Word Fall Through mode.
2. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.
3. Values guaranteed by design, not currently tested.
HSTL

**1.5V AC TEST CONDITIONS**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pulse Levels</td>
<td>0.25 to 1.25V</td>
</tr>
<tr>
<td>Input Rise/Fall Times</td>
<td>0.4ns</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>0.75</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>VDDQ/2</td>
</tr>
</tbody>
</table>

**NOTE:**
1. VDDQ = 1.5V±.

EXTENDED HSTL

**1.8V AC TEST CONDITIONS**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pulse Levels</td>
<td>0.4 to 1.4V</td>
</tr>
<tr>
<td>Input Rise/Fall Times</td>
<td>0.4ns</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>0.9</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>VDDQ/2</td>
</tr>
</tbody>
</table>

**NOTE:**
1. VDDQ = 1.8V±.

2.5V LVTTL

**2.5V AC TEST CONDITIONS**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Pulse Levels</td>
<td>GND to 2.5V</td>
</tr>
<tr>
<td>Input Rise/Fall Times</td>
<td>1ns</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>Vcc/2</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>VDDQ/2</td>
</tr>
</tbody>
</table>

**NOTE:**
1. For LVTTL Vcc = VDDQ.
**OUTPUT ENABLE & DISABLE TIMING**

![Diagram of Output Enable & Disable Timing]

**NOTES:**
1. REN is HIGH.
2. RCS is LOW.

**READ CHIP SELECT ENABLE & DISABLE TIMING**

![Diagram of Read Chip Select Enable & Disable Timing]

**NOTES:**
1. REN is HIGH.
2. OE is LOW.
FUNCTIONAL DESCRIPTION

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72T36135M support two different timing modes of operation: IDT Standard mode or First Word Fall Through (FWFT) mode. The selection of which mode will operate is determined during Master Reset, by the state of the FWFT/SL input.

If, at the time of Master Reset, FWFT/SL is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag (EF[1:2]) to indicate whether or not there are any words present in the FIFO. It also uses the Full Flag function (FF[1:2]) to indicate whether or not the FIFO has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable (REN) and RCLK.

If, at the time of Master Reset, FWFT/SL is HIGH, then FWFT mode will be selected. This mode uses Output Ready (OR[1:2]) to indicate whether or not there is valid data at the data outputs (Qn). It also uses Input Ready (IR[1:2]) to indicate whether or not the FIFO has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Qn after three RCLK rising edges. REN = LOW is not necessary. Subsequent words must be accessed using the Read Enable (REN) and RCLK.

Various signals, both input and output signals operate differently depending on which timing mode is in effect.

IDT STANDARD MODE

In this mode, the status flags, FF[1:2], PAF[1:2], PAE[1:2], and EF[1:2] operate in the manner outlined in Table 2. To write data into the FIFO, Write Enable (WEN) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag (EF[1:2]) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag (PAE[1:2]) will go HIGH after n + 1 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

Continuing to write data into the FIFO will cause the Programmable Almost-Full flag (PAF[1:2]) to go LOW. Again, if no reads are performed, the PAF[1:2] will go LOW. The offset “m” is the full offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

When the FIFO is full, the Full Flag (FF[1:2]) will go LOW, inhibiting further write operations. If no reads are performed after a reset, FF[1:2] will go LOW after D writes to the FIFO.

If the FIFO is full, the first read operation will cause FF[1:2] to go HIGH. Subsequent read operations will cause PAF[1:2] to go HIGH at the conditions described in Table 2. If further read operations occur, without write operations, PAE[1:2] will go LOW when there are n words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, the EF[1:2] will go LOW inhibiting further read operations. REN is ignored when the FIFO is empty.

When configured in IDT Standard mode, the EF[1:2] and FF[1:2] outputs are double register-buffered outputs.

Relevant timing diagrams for IDT Standard mode can be found in Figure 10, 11, 12 and 17.

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags, IR[1:2], PAF[1:2], PAE[1:2], and OR[1:2] operate in the manner outlined in Table 3. To write data into to the FIFO, WEN must be LOW. Data presented to the DATA IN lines will be cycled into the FIFO on subsequent transitions of WCLK. After the first write is performed, the Output Ready (OR[1:2]) flag will go LOW. Subsequent writes will continue to fill up the FIFO. PAE[1:2] will go HIGH after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default setting for these values are stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

When the FIFO is full, the Input Ready (IR[1:2]) flag will go HIGH, inhibiting further write operations. If no reads are performed after a reset, IR[1:2] will go HIGH after D writes to the FIFO. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation will cause the IR[1:2] flag to go LOW. Subsequent read operations will cause the PAF[1:2] to go HIGH at the conditions described in Table 3. If further read operations occur, without write operations, the PAE[1:2] will go LOW when there are n + 1 words in the FIFO, where n is the empty offset value. Continuing read operations will cause the FIFO to become empty. When the last word has been read from the FIFO, OR[1:2] will go HIGH inhibiting further read operations. REN is ignored when the FIFO is empty.

When configured in FWFT mode, the OR[1:2] flag output is triple register-buffered, and the IR[1:2] flag output is double register-buffered.

Relevant timing diagrams for FWFT mode can be found in Figure 13, 14, 15 and 18.
PROGRAMMING FLAG OFFSETS

Full and Empty Flag offset values are user programmable. The IDT72T36135M have internal registers for these offsets. There are eight default offset values selectable during Master Reset. These offset values are shown in Table 1. Offset values can also be programmed into the FIFO in one of two ways; serial or parallel loading method. The selection of the loading method is done using the LD (Load) pin. During Master Reset, the state of the LD input determines whether serial or parallel flag offset programming is enabled. A HIGH on LD during Master Reset selects serial loading of offset values. A LOW on LD during Master Reset selects parallel loading of offset values.

In addition to loading offset values into the FIFO, it is also possible to read the current offset values. Offset values can be read via the parallel output port Q0-Qn, regardless of the programming mode selected (serial or parallel). It is not possible to read the offset values in serial fashion.

Figure 3, Programmable Flag Offset Programming Sequence, summarizes the control pins and sequence for both serial and parallel programming modes. For a more detailed description, see discussion that follows.

The offset registers may be programmed (and reprogrammed) any time after Master Reset, regardless of whether serial or parallel programming has been selected. Valid programming ranges are from 0 to D-1.

SYNCHRONOUS vs ASYNCHRONOUS PROGRAMMABLE FLAG TIMING SELECTION

The IDT72T36135M can be configured during the Master Reset cycle with either synchronous or asynchronous timing for PAF[1:2] and PAE[1:2] flags by use of the PFM pin.

If synchronous PAF/PAE[1:2] configuration is selected (PFM, HIGH during MRS), the PAF is asserted and updated on the rising edge of WCLK only and not RCLK. Similarly, PAE[1:2] is asserted and updated on the rising edge of RCLK only and not WCLK. For detail timing diagrams, see Figure 22 for synchronous PAF[1:2] timing and Figure 23 for synchronous PAE[1:2] timing.

If asynchronous PAF/PAE[1:2] configuration is selected (PFM, LOW during MRS), the PAF is asserted LOW on the LOW-to-HIGH transition of WCLK and PAF[1:2] is reset to HIGH on the LOW-to-HIGH transition of RCLK. Similarly, PAE[1:2] is asserted LOW on the LOW-to-HIGH transition of RCLK. PAE[1:2] is reset to HIGH on the LOW-to-HIGH transition of WCLK. For detail timing diagrams, see Figure 24 for asynchronous PAF[1:2] timing and Figure 25 for asynchronous PAE[1:2] timing.

### Table 1 — Default Programmable Flag Offsets

<table>
<thead>
<tr>
<th>IDT72T36135M</th>
<th>*LD</th>
<th>FSEL1</th>
<th>FSEL0</th>
<th>Offsets n,m</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>1,023</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>511</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>255</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>127</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>63</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>31</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>15</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>7</td>
</tr>
</tbody>
</table>

*THIS PIN MUST BE HIGH AFTER MASTER RESET TO WRITE OR READ DATA TO/FROM THE FIFO MEMORY.

### Table 2 — Status Flags for IDT Standard Mode

<table>
<thead>
<tr>
<th>Number of Words in FIFO</th>
<th>IDT72T36135M</th>
<th>FF</th>
<th>PAF</th>
<th>PAE</th>
<th>EF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>1 to n</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>(524,288-m) to 524,287</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>524,288</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: 1. See Table 1 for values for n, m.

### Table 3 — Status Flags for FWFT Mode

<table>
<thead>
<tr>
<th>Number of Words in FIFO</th>
<th>IDT72T36135M</th>
<th>TR</th>
<th>PAF</th>
<th>PAE</th>
<th>OR</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>1 to n+1</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>(524,289-m) to 524,288</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>524,289</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: 1. See Table 1 for values for n, m.
### IDT72T36135M 2.5V 18M-BIT TeraSync™ 36-BIT FIFO

#### COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

<table>
<thead>
<tr>
<th>LD</th>
<th>WEN</th>
<th>REN</th>
<th>SEN</th>
<th>WCLK</th>
<th>RCLK</th>
<th>SCLK</th>
<th>IDT72T36135M</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>X</td>
<td></td>
<td></td>
<td>Parallel write to registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>X</td>
<td></td>
<td></td>
<td>Parallel read from registers: Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
<td></td>
<td></td>
<td>Serial shift into registers: 38 bits for the IDT72T36135M 1 bit for each rising SCLK edge Starting with Empty Offset (LSB) Ending with Full Offset (MSB)</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Consecutive reads of the offset registers is not permitted. The read operation must be disabled for a minimum of one RCLK cycle in between offset register accesses. (Please refer to Figure 21, Parallel Read of Programmable Flag Registers (IDT Standard and FWFT Modes) for more details).
2. Parallel reading of the offset registers is always permitted regardless of which programming method has been selected.
3. The programming sequence applies to both IDT Standard and FWFT modes.

**Figure 3. Programmable Flag Offset Programming Sequence**

---

© 2019 Renesas Electronics Corporation
SERIAL PROGRAMMING MODE

If Serial Programming mode has been selected, as described above, then programming of PAF[1:2] and PAF[1:2] values can be achieved by using a combination of the LD, SEN, SCLK and SI inputs. Programming PAF[1:2] and PAF[1:2] proceeds as follows: when LD and SEN are set LOW, data on the SI input are written, one bit for each SCLK rising edge, starting with the Empty Offset LSB and ending with the Full Offset MSB. 38 bits total required. See Figure 19, Serial Loading of Programmable Flag Registers, for the timing diagram for this mode.

Using the serial method, individual registers cannot be programmed selectively. PAF[1:2] and PAF[1:2] can show a valid status only after the complete set of bits (for all offset registers) has been entered. The registers can be reprogrammed as long as the complete set of new offset bits is entered. When LD is LOW and SEN is HIGH, no serial write to the registers can occur.

Write operations to the FIFO are allowed before and during the serial programming sequence. In this case, the programming of all offset bits does not have to occur at once. A select number of bits can be written to the SI input and then, by bringing LD and SEN HIGH, data can be written to FIFO memory via Dn by toggling WEN. When WEN is brought HIGH with LD and SEN restored to a LOW, the next offset bit in sequence is written to the registers via SI. If an interruption of serial programming is desired, it is sufficient to set LD LOW and deactivate SEN or to set SEN LOW and deactivate LD. Once LD and SEN are both restored to a LOW level, serial offset programming continues.

From the time serial programming has begun, neither programmable flag will be valid until the full set of bits required to fill all the offset registers has been written. Measuring from the rising SCLK edge that achieves the above criteria: PAF[1:2] will be valid after three more rising WCLK edges plus tPAE, PAF[1:2] will be valid after the next three rising RCLK edges plus tPAE.

It is only possible to read the flag offset values via the parallel output port Qn.

PARALLEL MODE

If Parallel Programming mode has been selected, as described above, then programming of PAF[1:2] and PAF[1:2] values can be achieved by using a combination of the LD, WCLK, WEN and Dn input pins. Programming PAF[1:2] and PAF[1:2] proceeds as follows: LD and WEN must be set LOW. When programming the Offset Registers of the TeraSync FIFO’s the number of programming cycles will be based on the bus width, the following rules apply:

4 enabled write cycles are required to program the offset registers, (2 per offset). Data on the inputs Dn are written into the Empty Offset Register on the first two LOW-to-HIGH transition of WCLK. Upon the third and fourth LOW-to-HIGH transition of WCLK, data are written into the Full Offset Register. See Figure 3, Programmable Flag Offset Programming Sequence for more details.

RETRANSMIT FROM MARK OPERATION

The Retransmit from Mark feature allows FIFO data to be read repeatedly starting at a user-selected position. The FIFO is first put into retransmit mode that will ‘mark’ a beginning word and also set a pointer that will prevent ongoing FIFO write operations from over-writing retransmit data. The retransmit data can be read repeatedly any number of times from the ‘marked’ position. The FIFO can be taken out of retransmit mode at any time to allow normal device operation. The ‘mark’ position can be selected any number of times, each selection overwriting the previous mark location. Retransmit operation is available in both IDT standard and FWFT modes.

During IDT standard mode the FIFO is put into retransmit mode by a Low-to-High transition on RCLK when the ‘MARK’ input is HIGH and EF[1:2] is HIGH. The rising RCLK edge ‘marks’ the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a rising edge on RCLK occurs while MARK is LOW.

Once a ‘marked’ location has been set (and the device is still in retransmit mode, MARK is HIGH), a retransmit can be initiated by a rising edge on RCLK while the retransmit input (RT) is LOW. REN must be HIGH (reads disabled) before bringing RT LOW. The device indicates the start of retransmit setup by setting EF[1:2] LOW, also preventing reads. When EF[1:2] goes HIGH, retransmit setup is complete and read operations may begin starting with the first data at the MARK location. Since IDT standard mode is selected, every word reading including the first ‘marked’ word following a retransmit setup requires a LOW on REN (read enabled).

Note, write operations may continue as normal during all retransmit functions, however write operations to the ‘marked’ location will be prevented. See Figure 17, Retransmit from Mark (IDT standard mode), for the relevant timing diagram.

During FWFT mode the FIFO is put into retransmit mode by a rising RCLK edge when the ‘MARK’ input is HIGH and OR[1:2] is LOW. The rising RCLK edge ‘marks’ the data present in the FIFO output register as the first retransmit data. The FIFO remains in retransmit mode until a rising RCLK edge occurs while MARK is LOW.

Once a marked location has been set (and the device is still in retransmit mode, MARK is HIGH), a retransmit can be initiated by a rising RCLK edge while the retransmit input (RT) is LOW. REN must be HIGH (reads disabled) before bringing RT LOW. The device indicates the start of retransmit setup by setting OR[1:2] HIGH.

When OR[1:2] goes LOW, retransmit setup is complete and on the next rising RCLK edge after retransmit setup is complete, (RT goes HIGH), the contents of the first retransmit location are loaded onto the output register. Since FWFT mode is selected, the first word appears on the outputs regardless of REN, a LOW on REN is not required for the first word. Reading all subsequent words requires a LOW on REN to enable the rising RCLK edge. See Figure 18, Retransmit from Mark timing (FWFT mode), for the relevant timing diagram.

Note, there must be a minimum of 128 words of data between the write pointer and read pointer when the MARK is asserted. Also, once the MARK is set, the write pointer will not increment past the “marked” location until the MARK is deasserted. This prevents “overwriting” of retransmit data.

HSTL/LVTTL I/O

Both the write port and read port are user selectable between HSTL or LVTTL I/O, via two select pins, WHSTL and RHSTL respectively. All other control pins are selectable via SHSTL, see Table 4 for details of groupings. Note, that when the write port is selected for HSTL mode, the user can reduce the power consumption (in stand-by mode by utilizing the WCS input). All “Static Pins” must be tied to Vcc or GND. These pins are LVTTL only, and are purely device configuration pins.
## TABLE 4 — I/O CONFIGURATION

<table>
<thead>
<tr>
<th>WHSTL SELECT</th>
<th>RHSTL SELECT</th>
<th>SHSTL SELECT</th>
<th>STATIC PINS</th>
</tr>
</thead>
<tbody>
<tr>
<td>WHSTL: HIGH = HSTL LOW = LVTTL</td>
<td>RHSTL: HIGH = HSTL LOW = LVTTL</td>
<td>SHSTL: HIGH = HSTL LOW = LVTTL</td>
<td>LVTTL ONLY</td>
</tr>
<tr>
<td>Dn (I/P)</td>
<td>RCLK/RD (I/P)</td>
<td>EF/OR[1:2] (O/P)</td>
<td>PRS (I/P)</td>
</tr>
<tr>
<td>WCLK/WR (I/P)</td>
<td>RCS (I/P)</td>
<td>PAF[1:2] (O/P)</td>
<td>ASYR (I/P)</td>
</tr>
<tr>
<td>WEN (I/P)</td>
<td>MARK (I/P)</td>
<td>PAE[1:2] (O/P)</td>
<td>FSEL1 (I/P)</td>
</tr>
<tr>
<td>WCS (I/P)</td>
<td>REN (I/P)</td>
<td>FF/IR[1:2] (O/P)</td>
<td>SHSTL (I/P)</td>
</tr>
<tr>
<td></td>
<td>OĒ (I/P)</td>
<td>TDO (O/P)</td>
<td>PFM (I/P)</td>
</tr>
<tr>
<td></td>
<td>RT (I/P)</td>
<td></td>
<td>WHSTL (I/P)</td>
</tr>
<tr>
<td></td>
<td>Qn (O/P)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
SIGNAL DESCRIPTION

INPUTS:

DATA IN (D0 - Dn)
Data inputs for 36-bit wide data (D0 - D35).

CONTROLS:

MASTER RESET (MRS)
A Master Reset is accomplished whenever the MRS input is taken to a LOW state. This operation sets the internal read and write pointers to the first location of the RAM array. PAE[1:2] will go LOW, PAF[1:2] will go HIGH. If FWFT/SI is LOW during Master Reset then the IDT Standard mode, along with EF[1:2] and FF[1:2] are selected. EF[1:2] will go LOW and FF[1:2] will go HIGH. If FWFT/SI is HIGH, then the First Word Fall Through mode (FWFT), along with IR[1:2] and OR[1:2], are selected. OR[1:2] will go HIGH and IR[1:2] will go LOW.

All control settings such as RM and PFM are defined during the Master Reset cycle.

During a Master Reset, the output register is initialized to all zeroes. A Master Reset is required after power up, before a write operation can take place. MRS is asynchronous.

See Figure 8, MasterResetTiming, for the relevant timing diagram.

PARTIAL RESET (PRS)

A Partial Reset is accomplished whenever the PRS input is taken to a LOW state. As in the case of the Master Reset, the internal read and write pointers are set to the first location of the RAM array. PAE[1:2] goes LOW, PAF[1:2] goes HIGH.

Whichever mode is active at the time of Partial Reset, IDT Standard mode or First Word Fall Through, that mode will remain selected. If the IDT Standard mode is active, then FF[1:2] will go HIGH and EF[1:2] will go LOW. If the First Word Fall Through mode is active, then OR[1:2] will go HIGH, and IR[1:2] will go LOW.

Following Partial Reset, all values held in the offset registers remain unchanged. The programming method (parallel or serial) currently active at the time of Partial Reset is also retained. The output register is initialized to all zeroes. PRS is asynchronous.

A Partial Reset is useful for resetting the device during the course of operation, when reprogramming programmable flag offset settings may not be convenient.

See Figure 9, PartialResetTiming, for the relevant timing diagram.

ASYNCHRONOUS WRITE (ASYW)

The write port can be configured for either Synchronous or Asynchronous mode of operation. If during Master Reset the ASYW input is LOW, then Asynchronous operation of the write port will be selected. During Asynchronous operation of the write port the WCLK input becomes WR input, this is the Asynchronous write strobe input. A rising edge on WR will write data present on the Dn inputs into the FIFO. (WEN must be tied LOW when using the write port in Asynchronous mode).

When the write port is configured for Asynchronous operation the full flag (FF[1:2]) operates in an asynchronous manner, that is, the full flag will be updated based in both a write operation and read operation. Note, if Asynchronous mode is selected, FWFT is not permissible. Refer to Figures 26, 27, 30 and 31 for relevant timing and operational waveforms.

ASYNCHRONOUS READ (ASYR)

The read port can be configured for either Synchronous or Asynchronous mode of operation. If during a Master Reset the ASYR input is LOW, then Asynchronous operation of the read port will be selected. During Asynchronous operation of the read port the RCLK input becomes RD input, this is the Asynchronous read strobe input. A rising edge on RD will read data from the FIFO via the output register and Qn port. (REN must be tied LOW during Asynchronous operation of the read port).

The OÆ input provides three-state control of the Qn output bus, in an asynchronous manner. (RCS, provides three-state control of the read port in Synchronous mode).

When the read port is configured for Asynchronous operation the device must be operating on IDT standard mode, FWFT mode is not permissible if the read port is Asynchronous. The Empty Flag (EF[1:2]) operates in an Asynchronous manner, that is, the empty flag will be updated based on both a read operation and a write operation. Refer to figures 28, 29, 30 and 31 for relevant timing and operational waveforms.

RETRANSMIT (RT)

The Retransmit (RT) input is used in conjunction with the MARK input, together they provide a means by which data previously read out of the FIFO can be reread any number of times. If retransmit operation has been selected (i.e. the MARK input is HIGH), a rising edge on RCLK while RT is LOW will reset the read pointer back to the memory location set by the user via the MARK input.

If IDT standard mode has been selected the EF[1:2] flag will go LOW and remain LOW for the time that RT is held LOW. RT can be held LOW for any number of RCLK cycles, the read pointer being reset to the marked location. The next rising edge of RCLK after RT has returned HIGH, will cause EF[1:2] to go HIGH, allowing read operations to be performed on the FIFO. The next read operation will access data from the ‘marked’ memory location.

Subsequent retransmit operations may be performed, each time the read pointer returning to the ‘marked’ location. See Figure 17, Retrnsmit from Mark (IDT Standard mode) for the relevant timing diagram.

If FWFT mode has been selected the OR[1:2] flag will go HIGH and remain HIGH for the time that RT is held LOW. RT can be held LOW for any number of RCLK cycles, the read pointer being reset to the ‘marked’ location. The next RCLK rising edge after RT has returned HIGH, will cause OR[1:2] to go LOW and due to FWFT operation, the contents of the marked memory location will be loaded onto the output register, a read operation being required for all subsequent data reads.

Subsequent retransmit operations may be performed each time the read pointer returning to the ‘marked’ location. See Figure 18, Retransmit from Mark (FWF mode) for the relevant timing diagram.

MARK

The MARK input is used to select Retransmit mode of operation. An RCLK rising edge while MARK is HIGH will mark the memory location of the data currently present on the output register, the device will also be placed into retransmit mode. For the IDT72T36135M a minimum of 128 words (x36). Also, once the MARK is set, the write pointer will not increment past the “marked” location until the MARK is deasserted. This prevents “overwriting” of retransmit data.

The MARK input must remain HIGH during the whole period of retransmit mode, a falling edge of RCLK while MARK is LOW will take the device out of retransmit mode and into normal mode. Any number of MARK locations can be set during FIFO operation, only the last marked location taking effect. Once a
mark location has been set the write pointer cannot be incremented past this marked location. During retransmit mode write operations to the device may continue without hindrance.

**FIRST WORD FALL THROUGH/SERIAL IN (FWFT/SI)**

This is a dual purpose pin. During Master Reset, the state of the FWFT/SI input determines whether the device will operate in IDT Standard mode or First Word Fall Through (FWFT) mode.

If, at the time of Master Reset, FWFT/SI is LOW, then IDT Standard mode will be selected. This mode uses the Empty Flag (EF[1:2]) to indicate whether or not there is valid data at the data outputs (Qn). It also uses the Full Flag function (FF[1:2]) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using the Read Enable (REN) and RCLK.

If, at the time of Master Reset, FWFT/SI is HIGH, then FWFT mode will be selected. This mode uses the Output Ready (OR[1:2]) to indicate whether or not there is valid data at the data outputs (Qn). It also uses Input Ready (IR[1:2]) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to Qn after three RCLK rising edges, REN = LOW is not necessary. Subsequent words must be accessed using the Read Enable (REN) and RCLK.

After Master Reset, FWFT/SI acts as a serial input for loading PAE[1:2] and PAF[1:2] offsets into the programmable registers. The serial input function can only be used when the serial loading method has been selected during Master Reset. Serial programming using the FWFT/SI pin functions the same way in both IDT Standard and FWFT modes.

**WRITE STROBE & WRITE CLOCK (WR/WCLK)**

If Synchronous operation of the write port has been selected via ASYR, this input behaves as WCLK.

A write cycle is initiated on the rising edge of the WCLK input. Data setup and hold times must be met with respect to the LOW-to-HIGH transition of the WCLK. It is permissible to stop the WCLK. Note that while WCLK is idle, the FF/IR[1:2], and PAE[1:2] flags will not be updated. The Write and Read Clocks can be independent or coincident.

If Asynchronous operation has been selected this input is WR (write strobe).

Data is Asynchronously written from the FIFO via the DN inputs whenever there is a rising edge on WR. In this mode the WREN input must be tied LOW.

**WRITE ENABLE (WREN)**

When the WREN input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When WREN is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the IDT Standard mode, FF[1:2] will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, FF[1:2] will go HIGH allowing a write to occur. The FF[1:2] is updated by two WCLK cycles + tSKEW after the RCLK cycle.

To prevent data overflow in the FWFT mode, IR[1:2] will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, IR[1:2] will go LOW allowing a write to occur. The IR[1:2] flag is updated by two WCLK cycles + tSKEW after the valid RCLK cycle.

WREN is ignored when the FIFO is full in either FWFT or IDT Standard mode.

If Asynchronous operation of the write port has been selected, then WREN must be held active, (tied LOW).

**READ STROBE & READ CLOCK (RD/RCLK)**

If Synchronous operation of the read port has been selected via ASYR, this input behaves as RCLK. A read cycle is initiated on the rising edge of the RCLK input. Data can be read on the outputs, on the rising edge of the RCLK input. It is permissible to stop the RCLK. Note that while RCLK is idle, the EF/OR[1:2], and PAE[1:2] flags will not be updated. The Write and Read Clocks can be independent or coincident.

If Asynchronous operation has been selected this input is RD (Read Strobe).

Data is Asynchronously read from the FIFO via the output register whenever there is a rising edge on RD. In this mode the REN and RCS inputs must be tied LOW. The OE input is used to provide Asynchronous control of the three-state Qn outputs.

**WRITE CHIP SELECT (WCS)**

The WCS disables all Write Port inputs (data only) if it is held HIGH. To perform normal operations on the write port, the WCS must be enabled, held LOW.

**READ ENABLE (REN)**

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty. When the REN input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Qn-Qn maintain the previous data value.

In the IDT Standard mode, every word accessed at Qn, including the first word written to an empty FIFO, must be requested using REN provided that RCS is LOW. When the last word has been read from the FIFO, the Empty Flag (EF[1:2]) will go LOW, inhibiting further read operations. REN is ignored when the FIFO is empty. Once a write is performed, EF[1:2] will go HIGH allowing a read to occur. The EF[1:2] flag is updated by two RCLK cycles + tSKEW after the valid WCLK cycle. Both RCS and REN must be active, LOW for data to be read out on the rising edge of RCLK.

In the FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Qn, on the third valid LOW-to-HIGH transition of RCLK + tSKEW after the first write. REN and RCS do not need to be asserted LOW for the First Word to fall through to the output register. In order to access all other words, a read must be executed using REN and RCS. The RCLK LOW-HIGH transition after the last word has been read from the FIFO, Output Ready (OR[1:2]) will go HIGH with a true read (RCLK with REN = LOW, RCS = LOW), inhibiting further read operations. REN is ignored when the FIFO is empty.

If Asynchronous operation of the Read port has been selected, then REN must be held active, (tied LOW).

**SERIAL ENABLE (SEN)**

The SEN input is an enable used only for serial programming of the offset registers. The serial programming method must be selected during Master Reset. SEN is always used in conjunction with LD. When these lines are both LOW, data at the SI input can be loaded into the program register one bit for each LOW-to-HIGH transition of SCLK.

When SEN is HIGH, the programmable registers retains the previous settings and no offsets are loaded. SEN functions the same way in both IDT Standard and FWFT modes.

**OUTPUT ENABLE (OE)**

When Output Enable is enabled (LOW), the parallel output buffers receive data from the output register. When OE is HIGH, the output data bus (Qn) goes into a high impedance state. During Master or a Partial Reset the OE is the only input that can place the output bus Qn, into High-Impedance. During Reset the RCS input can be HIGH or LOW, it has no effect on the Qn outputs.
READ CHIP SELECT (RCS)

The Read Chip Select input provides synchronous control of the Read output port. When RCS goes LOW, the next rising edge of RCLK causes the Qn outputs to go to the Low-Impedance state. When RCS goes HIGH, the next RCLK rising edge causes the Qn outputs to return to HIGH-Z. During a Master or Partial Reset the RCS input has no effect on the Qn output bus. OE is the only input that provides High-Impedance control of the Qn outputs. If OE is LOW the Qn data outputs will be Low-Impedance regardless of RCS until the first rising edge of RCLK after a Reset is complete. Then if RCS is HIGH the data outputs will go to High-Impedance.

The RCS input does not effect the operation of the flags. For example, when the first word is written to an empty FIFO, the EF[1:2] will still go from LOW to HIGH based on a rising edge of RCLK, regardless of the state of the RCS input.

Also, when operating the FIFO in FWFT mode the first word written to an empty FIFO will still be clocked through to the output register based on RCLK, regardless of the state of RCS. For this reason the user must take care when a data word is written to an empty FIFO in FWFT mode. If RCS is disabled when an empty FIFO is written into, the first word will fall through to the output register, but will not be available on the Qn outputs which are in HIGH-Z. The user must take RCS active LOW to access this first word, place the output bus in LOW-Z. RCS must remain disabled HIGH for at least one cycle after RCS has gone LOW. A rising edge of RCLK with RCS and REN active LOW, will read out the next word. Care must be taken so as not to lose the first word written to an empty FIFO when RCS is HIGH. Refer to Figure 16, RCS and REN Read Operation (FWFT Mode).

The RCS pin must also be active (LOW) in order to perform a Retransmit. See Figure 12 for Read Cycle and Read Chip Select Timing (IDT Standard Mode). See Figure 15 for Read Cycle and Read Chip Select Timing (First Word Fall Through Mode).

If Asynchronous operation of the Read port has been selected, then RCS must be held active, (tied LOW). OE provides three-state control of Qn.

WRITE PORT HSTL SELECT (WHSTL)

The control inputs, data inputs and flag outputs associated with the write port can be setup to be either HSTL or LV TTL. If WHSTL is HIGH during the Master Reset, then HSTL operation of the write port will be selected. If WHSTL is LOW at Master Reset, then LV TTL will be selected.

The inputs and outputs associated with the write port are listed in Table 4, I/O Configuration.

READ PORT HSTL SELECT (RHSTL)

The control inputs, data inputs and flag outputs associated with the read port can be setup to be either HSTL or LV TTL. If RHSTL is HIGH during the Master Reset, then HSTL operation of the read port will be selected. If RHSTL is LOW at Master Reset, then LV TTL will be selected for the read port.

The inputs and outputs associated with the read port are listed in Table 4, I/O Configuration.

SYSTEM HSTL SELECT (SHSTL)

All inputs not associated with the write and read port can be setup to be either HSTL or LV TTL. If SHSTL is HIGH during Master Reset, then HSTL operation of all the inputs not associated with the write and read port will be selected. If SHSTL is LOW at Master Reset, then LV TTL will be selected. The inputs associated with SHSTL are listed in Table 4, I/O Configuration.

LOAD (LD)

This is a dual purpose pin. During Master Reset, the state of the LD input, along with FSEL0 and FSEL1, determines one of eight default offset values for the PAE[1:2] and PAF[1:2] flags, along with the method by which these offset registers can be programmed, parallel or serial (see Table 1). After Master Reset, LD enables write operations to and read operations from the offset registers. Only the offset loading method currently selected can be used to write to the registers. Offset registers can be read only in parallel.

After Master Reset, the LD pin is used to activate the programming process of the flag offset values PAE[1:2] and PAF[1:2]. Pulling LD LOW will begin a serial loading or parallel load or read of these offset values. THIS PIN MUST BE HIGH AFTER MASTER RESET TO WRITE OR READ DATA TO/FROM THE FIFO MEMORY.

PROGRAMMABLE FLAG MODE (PFM)

During Master Reset, a LOW on PFM will select Asynchronous Programmable flag timing mode. A HIGH on PFM will select Synchronous Programmable flag timing mode. If asynchronous PAE/PAF[1:2] configuration is selected (PFM, LOW during MRS), the PAE[1:2] is asserted LOW on the LOW-to-HIGH transition of RCLK. PAF[1:2] is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the PAF[1:2] is asserted LOW on the LOW-to-HIGH transition of WCLK and PAF[1:2] is reset to HIGH on the LOW-to-HIGH transition of RCLK.

If synchronous PAE/PAF[1:2] configuration is selected (PFM, HIGH during MRS), the PAE[1:2] is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, PAF[1:2] is asserted and updated on the rising edge of WCLK only and not RCLK. The mode desired is configured during master reset by the state of the Programmable Flag Mode (PFM) pin.

OUTPUTS:

FULL FLAG (FF[IR[1:2]])

This is a dual purpose pin. In IDT Standard mode, the Full Flag (FF[1:2]) function is selected. When the FIFO is full, FF[1:2] will go LOW, inhibiting further write operations. When FF[1:2] is HIGH, the FIFO is not full. If no reads are performed after a reset (either MRS or PRS), FF[1:2] will go LOW after a write to the FIFO (D = 524,288 for the IDT72T36135M). See Figure 10, Write Cycle and Full Flag Timing (IDT Standard Mode), for the relevant timing information. Please see Flaging section for external gating instructions of these flags.

In FWFT mode, the Input Ready (IR[1:2]) function is selected. IR[1:2] goes LOW when memory space is available for writing in data. When there is no longer any free space left, IR[1:2] goes HIGH, inhibiting further write operations. If no reads are performed after a reset (either MRS or PRS), IR[1:2] will go HIGH after a write to the FIFO (D = 524,288 for the IDT72T36135M). See Figure 13, Write Timing (FWFT Mode), for the relevant timing information.

The IR[1:2] status not only measures the contents of the FIFO memory, but also counts the presence of a word in the output register. Thus, in FWFT mode, the total number of write operations necessary to deassert IR[1:2] is one greater than needed to assert FF[1:2] in IDT Standard mode.

FF[IR[1:2]] is synchronous and updated on the rising edge of WCLK. FF/ IR[1:2] are double register-buffered outputs.

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the ‘marked’ location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

EMPTY FLAG (EF/IR[1:2])

This is a dual purpose pin. In the IDT Standard mode, the Empty Flag (EF[1:2]) function is selected. When the FIFO is empty, EF[1:2] will go LOW, inhibiting further read operations. When EF[1:2] is HIGH, the FIFO is not empty. See Figure 11, Read Cycle, Empty Flag and First Word Latency Timing (IDT Standard Mode), for the relevant timing information. Please see Flaging section for external gating instructions of these flags.
In FWFT mode, the Output Ready (OR[1:2]) function is selected. OR[1:2] goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. OR[1:2] stays LOW after the RCLK LOW to HIGH transition that shifts the last word from the FIFO memory to the outputs. OR[1:2] goes HIGH only with a true read (RCLK with REN = LOW). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until OR[1:2] goes LOW again. See Figure 14, Read Timing (FWFT Mode), for the relevant timing information.

EF/OR[1:2] is synchronous and updated on the rising edge of RCLK.

In IDT Standard mode, EF[1:2] is a double register-buffered output. In FWFT mode, OR[1:2] is a triple register-buffered output.

**PROGRAMMABLE ALMOST-FULL FLAG (PAF[1:2])**

The Programmable Almost-Full flag (PAF[1:2]) will go LOW when the FIFO reaches the almost-full condition. In IDT Standard mode, if no reads are performed after reset (MRS), PAF[1:2] will go LOW after (D - m) words are written to the FIFO. The PAF[1:2] will go LOW after (524,288-m) writes for the IDT72T36135M. The offset “m” is the full offset value. The default setting for this value is stated in the footnote of Table 2, Status Flags for IDT Standard Mode. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the PAF[1:2] will go LOW after (524,289-m) writes for the IDT72T36135M, where m is the full offset value. The default setting for this value is stated in Table 3, Status Flags for FWFT Mode.

See Figure 22, Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Mode), for the relevant timing information.

If asynchronous PAF[1:2] configuration is selected, the PAF[1:2] is asserted LOW on the LOW-to-HIGH transition of the Write Clock (WCLK). PAF[1:2] is reset to HIGH on the LOW-to-HIGH transition of the Read Clock (RCLK). If synchronous PAF[1:2] configuration is selected, the PAF[1:2] is updated on the rising edge of WCLK. See Figure 24, Asynchronous Almost-Full Flag Timing (IDT Standard and FWFT Mode).

Note, when the device is in Retransmit mode, this flag is a comparison of the write pointer to the ‘marked’ location. This differs from normal mode where this flag is a comparison of the write pointer to the read pointer.

**PROGRAMMABLE ALMOST-EMPTY FLAG (PAE[1:2])**

The Programmable Almost-Empty flag (PAE[1:2]) will go LOW when the FIFO reaches the almost-empty condition. In IDT Standard mode, PAE[1:2] will go LOW when there are n words or less in the FIFO. The offset “n” is the empty offset value. The default setting for this value is stated in the footnote of Table 1. Please see Flagging section for external gating instructions of these flags.

In FWFT mode, the PAE[1:2] will go LOW when there are n+1 words or less in the FIFO. The default setting for this value is stated in Table 1.

See Figure 23, Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode), for the relevant timing information.

If asynchronous PAE[1:2] configuration is selected, the PAE[1:2] is asserted LOW on the LOW-to-HIGH transition of the Read Clock (RCLK). PAE[1:2] is reset to HIGH on the LOW-to-HIGH transition of the Write Clock (WCLK). If synchronous PAE[1:2] configuration is selected, the PAE[1:2] is updated on the rising edge of WCLK. See Figure 25, Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Mode).
CONSIDERATIONS FOR READING FLAG OUTPUTS

On this device, there are two sets of flagging outputs for the empty flag (EF1 & EF2), full flag (FF1 & FF2), Programmable Almost Empty Flag (PAE1 & PAE2), and Programmable Almost Full Flag (PAF1 & PAF2) the user must work with in order to be correctly read the status of each flag. Since this device is a multi-chip module (MCM), both die’s flags must be read accordingly to avoid skewing problems between the two internal die.

To remedy this function, the user must tie together FF1 & FF2, and EF1 & EF2 flag outputs to an external gate from a neighboring programmable device such as an FPGA or PLD and read from the output of the logical gate. An OR gate is used for FWFT mode and an AND gate is used for IDT mode. This must be done to avoid timing skew problems between the two sets of flags. For the PAE[1:2] and PAF[1:2] active low output flags, the user has the option to leave the PAE[1:2] and PAF[1:2] as is and use both pins at different programmable water marks for measuring buffer status. Please see the section on Parallel Programming Mode to understand how to program these two sets of flags as different water marks in Functional Description section of the datasheet. This gives added flexibility for queue management. Below is an example diagram for how this is accomplished.

PIN COMPATIBILITY WITH 9M TERASYNC (IDT72T36125) CONSIDERATIONS

The IDT72T36135M can be a drop and replacement for the 9M TeraSync (IDT72T36125) if specific pin changes are made to the 18M FIFO. Since the 18M TeraSync is a Multi-Chip Module (MCM), containing two 9M TeraSyncs (IDT72T18125) in width expansion mode, certain functionality can not be offered in the 18M TeraSync such as bus matching, single flag outputs and interspersed parity. From these changes, the 18M FIFO has removed specific inputs such as IW, OW, BM, BE, IP, while also gaining another set of output flags as specified in Considerations for Reading Flag Outputs which are EF2, FF2, PAE2, and PAF2.

To maintain drop-in replacement compatibility for the 18M TeraSync, the pin changes on the pin diagram for the 18M TeraSync FIFO from the 9M TeraSync FIFO have been identified, and listed in the table below.

| TABLE 5 — PIN CHANGES BETWEEN 9M TERASYNC AND 18M TERASYNC |
|-------------------|-------------------|
| 9M TeraSync FIFO (IDT72T36125) | 18M TeraSync FIFO (IDT72T36135M) |
| pins changed | new pins |
| BM | EF2 |
| IP | PAE2 |
| IW | NC (No Connect) |
| OW | NC (No Connect) |
| HF | PAF2 |
| EREN | FF2 |
| ERCLK | NC (No Connect) |
| BE | GND |

NOTES:
1. Internally, the 9M pins on the left side of the table will be tied to the GND or VDD plane, respectively in the 18M device.
2. Please see IDT72T36125 TeraSync FIFO datasheet for additional features listed.
JTAG FUNCTIONALITY AND CONFIGURATION

The IDT72T36135M is composed of two independent memory arrays, and thus cannot be treated as a single JTAG device in the scan chain. The two arrays (A and B) each have identical characteristics and commands but must be treated as separate entities in JTAG operations. Please refer to Figure 5, JTAG Configuration for IDT72T36135M.

JTAG signaling must be provided serially to each array and utilize the information provided in the Scan Register Descriptions, JTAG Instruction Description. Specifically, commands for Array B must precede those Array A in any JTAG operations sent to the IDT72T36135M. Please reference Application Note AN-411, “JTAG Testing of Multichip Modules” for specific instructions on performing JTAG testing on the IDT72T36135M. AN-411 is available at www.idt.com.

Figure 5. JTAG Configuration for IDT72T36135M
### SYSTEM INTERFACE PARAMETERS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Output</td>
<td>tDo(1)</td>
<td></td>
<td>-</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>Data Output Hold</td>
<td>tDoh(1)</td>
<td></td>
<td>0</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Data Input</td>
<td>tDs</td>
<td>rise=3ns</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>tDh</td>
<td>fall=3ns</td>
<td>10</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTE:**
1. 50pf loading on external output signals.

### JTAG AC ELECTRICAL CHARACTERISTICS

(\(Vcc = 2.5V \pm 5\%\); \(Tcase = 0^\circ\text{C} \text{ to } +85^\circ\text{C}\))

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>IDT72T36135M</th>
</tr>
</thead>
<tbody>
<tr>
<td>JTAG Clock Input Period</td>
<td>tTCK</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>JTAG Clock HIGH</td>
<td>tTCKHIGH</td>
<td></td>
<td>100</td>
</tr>
<tr>
<td>JTAG Clock Low</td>
<td>tTCKLOW</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>JTAG Clock Rise Time</td>
<td>tTCKRISE</td>
<td></td>
<td>40</td>
</tr>
<tr>
<td>JTAG Clock Fall Time</td>
<td>tTCKFALL</td>
<td></td>
<td>-</td>
</tr>
<tr>
<td>JTAG Reset</td>
<td>tRST</td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>JTAG Reset Recovery</td>
<td>tRSR</td>
<td></td>
<td>50</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Guaranteed by design.
JTAG INTERFACE

Five additional pins (TDI, TDO, TMS, TCK and TRST) are provided to support the JTAG boundary scan interface. The IDT72T36135M incorporates the necessary tap controller and modified pad cells to implement the JTAG facility. Note that IDT provides appropriate Boundary Scan Description Language program files for these devices. The Standard JTAG interface consists of four basic elements:

- Test Access Port (TAP)
- TAP controller
- Instruction Register (IR)
- Data Register Port (DR)

The following sections provide a brief description of each element. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

The Figure below shows the standard Boundary-Scan Architecture.

**Figure 6. Boundary Scan Architecture**

TEST ACCESS PORT (TAP)

The Tap interface is a general-purpose port that provides access to the internal of the processor. It consists of four input ports (TCLK, TMS, TDI, TRST) and one output port (TDO).

THE TAP CONTROLLER

The Tap controller is a synchronous finite state machine that responds to TMS and TCLK signals to generate clock and control signals to the Instruction and Data Registers for capture and update of data.
Refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1) for the full state diagram.

All state transitions within the TAP controller occur at the rising edge of the TCLK pulse. The TMS signal level (0 or 1) determines the state progression that occurs on each TCLK rising edge. The TAP controller takes precedence over the FIFO memory and must be reset after power up of the device. See TRST description for more details on TAP controller reset.

**Test-Logic-Reset** All test logic is disabled in this controller state enabling the normal operation of the IC. The TAP controller state machine is designed in such a way that, no matter what the initial state of the controller is, the Test-Logic-Reset state can be entered by holding TMS at high and pulsing TCK five times. This is the reason why the Test Reset (TRST) pin is optional.

**Run-Test-Idle** In this controller state, the test logic in the IC is active only if certain instructions are present. For example, if an instruction activates the self test, then it will be executed when the controller enters this state. The test logic in the IC is idles otherwise.

**Select-DR-Scan** This is a controller state where the decision to enter the Data Path or the Select-IR-Scan state is made.

**Select-IR-Scan** This is a controller state where the decision to enter the Instruction Path is made. The Controller can return to the Test-Logic-Reset state otherwise.

**Capture-IR** In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be "01".

**Shift-IR** In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

**Exit1-IR** This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

**Pause-IR** This state is provided in order to allow the shifting of instruction register to be temporarily halted.

**Exit2-DR** This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

**Update-IR** In this controller state, the instruction in the instruction register is latched in to the latch bank of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

**Capture-DR** In this controller state, the shift register bank in the Instruction Register parallel loads a pattern of fixed values on the rising edge of TCK. The last two significant bits are always required to be "01".

**Shift-DR** In this controller state, the instruction register gets connected between TDI and TDO, and the captured pattern gets shifted on each rising edge of TCK. The instruction available on the TDI pin is also shifted in to the instruction register.

**Exit1-DR** This is a controller state where a decision to enter either the Pause-IR state or Update-IR state is made.

**Pause-DR** This state is provided in order to allow the shifting of instruction register to be temporarily halted.

**Exit2-DR** This is a controller state where a decision to enter either the Shift-IR state or Update-IR state is made.

**Update-DR** In this controller state, the instruction in the instruction register is latched in to the latch bank of the Instruction Register on every falling edge of TCK. This instruction also becomes the current instruction once it is latched.

**NOTES:**
1. Five consecutive TCK cycles with TMS = 1 will reset the TAP.
2. TAP controller does not automatically reset upon power-up. The user must provide a reset to the TAP controller (either by TRST or TMS).
3. TAP controller must be reset before normal FIFO operations can begin.
SCAN REGISTER DESCRIPTIONS

THE INSTRUCTION REGISTER

The Instruction register allows an instruction to be shifted in serially into the processor at the rising edge of TCLK.

The Instruction register is used to select the test to be performed, or the test data register to be accessed, or both. The instruction shifted into the register is latched at the completion of the shifting process when the TAP controller is at Update-IR state.

The instruction register must contain 8 bit instruction register-based cells which hold instruction data. These mandatory cells are located nearest the serial outputs they are the least significant bits.

THE TEST DATA REGISTER

The Test Data register contains three test data registers: the Bypass, the Boundary Scan Register and Device ID register.

These registers are connected in parallel between a common serial input and a common serial data output.

The following sections provide a brief description of each element. For a complete description, refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

TEST BYPASS REGISTER

The register is used to allow test data to flow through the device from TDI to TDO. It contains a single stage shift register for a minimum length in serial path. When the bypass register is selected by an instruction, the shift register stage is set to a logic zero on the rising edge of TCLK when the TAP controller is in the Capture-DR state.

The operation of the bypass register should not have any effect on the operation of the device in response to the BYPASS instruction.

THE BOUNDARY-SCAN REGISTER

The Boundary Scan Register allows serial data TDI to be loaded into or read out of the processor input/output ports. The Boundary Scan Register is a part of the IEEE 1149.1-1990 Standard JTAG Implementation.

THE DEVICE IDENTIFICATION REGISTER

The Device Identification Register is a Read Only 64-bit register used to specify the manufacturer, part number and version of the processor to be determined through the TAP in response to the IDCODE instruction.

IDT JEDEC ID number is 0xB3. This translates to 0x33 when the parity is dropped in the 11-bit Manufacturer ID field.

For the IDT72T36135M, the Part Number field contains the following values:

<table>
<thead>
<tr>
<th>Device</th>
<th>Part# Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDT72T36135M</td>
<td>0417</td>
</tr>
</tbody>
</table>

Please note:

The IDT72T36135M device is a two die MCM which means 64 bits will be shifted out of the device when the user is in IDCODE. Since the JTAG device identification register is 32 bits per die.

JTAG INSTRUCTION REGISTER

The Instruction register allows instruction to be serially input into the device when the TAP controller is in the Shift-IR state. The instruction is decoded to perform the following:

- Select test data registers that may operate while the instruction is current. The other test data registers should not interfere with chip operation and the selected data register.
- Define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

The Instruction Register is a 8 bit field (i.e. IR3, IR2, IR1, IR0 per die) to decode 32 different possible instructions. Instructions are decoded as follows.

Please note:

Again, since this device is a two die MCM, the JTAG instructions must be shifted in twice during JTAG testing. To account for each dies 4 bit instruction registers for a total of 8 bits altogether.

JTAG INSTRUCTION DESCRIPTION

<table>
<thead>
<tr>
<th>Hex Value</th>
<th>Instruction</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>EXTEST</td>
<td>Select Boundary Scan Register</td>
</tr>
<tr>
<td>0x22</td>
<td>IDCODE</td>
<td>Select Chip Identification data register</td>
</tr>
<tr>
<td>0x11</td>
<td>SAMPLE/PRELOAD</td>
<td>Select Boundary Scan Register</td>
</tr>
<tr>
<td>0x33</td>
<td>HIGH-IMPEDANCE</td>
<td>JTAG</td>
</tr>
<tr>
<td>0xFF</td>
<td>BYPASS</td>
<td>Select Bypass Register</td>
</tr>
</tbody>
</table>

JTAG Instruction Register Decoding

The following sections provide a brief description of each instruction. For a complete description refer to the IEEE Standard Test Access Port Specification (IEEE Std. 1149.1-1990).

EXTEST

The required EXTEST instruction places the IC into an external boundary-test mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register is accessed to drive test data off-chip via the boundary outputs and receive test data off-chip via the boundary inputs. As such, the EXTEST instruction is the workhorse of IEEE Std 1149.1, providing for probe-less testing of solder-joint opens/shorts and of logic cluster function.

IDCODE

The optional IDCODE instruction allows the IC to remain in its functional mode and selects the optional device identification register to be connected between TDI and TDO. The device identification register is a 64-bit shift register containing information regarding the IC manufacturer, device type, and version code. Accessing the device identification register does not interfere with the operation of the IC. Also, access to the device identification register should be immediately available, via a TAP data-scan operation, after power-up of the IC or after the TAP has been reset using the optional TRST pin or by otherwise moving to the Test-Logic-Reset state.

SAMPLE/PRELOAD

The required SAMPLE/PRELOAD instruction allows the IC to remain in a normal functional mode and selects the boundary-scan register to be connected between TDI and TDO. During this instruction, the boundary-scan register can be accessed via a date scan operation, to take a sample of the functional data entering and leaving the IC. This instruction is also used to preload test data into the boundary-scan register before loading an EXTEST instruction.
HIGH-IMPEDANCE

The optional High-Impedance instruction sets all outputs (including two-state as well as three-state types) of an IC to a disabled (high-impedance) state and selects the one-bit bypass register to be connected between TDI and TDO. During this instruction, data can be shifted through the bypass register from TDI to TDO without affecting the condition of the IC outputs.

BYPASS

The required BYPASS instruction allows the IC to remain in a normal functional mode and selects the one-bit bypass register to be connected between TDI and TDO. The BYPASS instruction allows serial data to be transferred through the IC from TDI to TDO without affecting the operation of the IC.
NOTE:
1. During Master Reset the High-Impedance control of the Qn data outputs is provided by OE only. RCS can be HIGH or LOW until the first rising edge of RCLK after Master Reset is complete.

Figure 8. Master Reset Timing
NOTE:
1. During Partial Reset the High-Impedance control of the Qn data outputs is provided by OE only. RCS can be HIGH or LOW until the first rising edge of RCLK after Master Reset is complete.

Figure 9. Partial Reset Timing
**COMMERCIAL AND INDUSTRIAL**

**TEMPERATURE RANGES**

---

**IDT72T36135M 2.5V 18M-BIT TeraSync™ 36-BIT FIFO**

524,288 x 36

---

**NOTES:**

1. \( t_{SKEW1} \) is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that \( FF[1:2] \) will go HIGH (after one WCLK cycle pux \( t_{WFF} \)). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than \( t_{SKEW1} \), then the \( FF[1:2] \) deassertion may be delayed one extra WCLK cycle.

2. \( LD = \) HIGH, \( OE = \) LOW, \( EF[1:2] = \) HIGH.

3. \( WCS = \) LOW.

---

**Figure 10. Write Cycle and Full Flag Timing (IDT Standard Mode)**

---

**NOTES:**

1. \( t_{SKEW1} \) is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that \( FF[1:2] \) will go HIGH (after one RCLK cycle plus \( t_{WFF} \)). If the time between the rising edge of the RCLK and the rising edge of the WCLK is less than \( t_{SKEW1} \), then the \( FF[1:2] \) deassertion may be delayed one extra RCLK cycle.

2. \( LD = \) HIGH, \( OE = \) LOW, \( EF[1:2] = \) HIGH.

3. \( WCS = \) LOW.

---

**Figure 11. Read Cycle, Output Enable, Empty Flag and First Data Word Latency (IDT Standard Mode)**

---

© 2019 Renesas Electronics Corporation
Figure 12. Read Cycle and Read Chip Select (IDT Standard Mode)

NOTES:
1. $t_{SKEW1}$ is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $EF[1:2]$ will go HIGH (after one RCLK cycle plus $t_{REF}$). If the time between the rising edge of WCLK and the rising edge of RCLK is less than $t_{SKEW1}$, then $EF[1:2]$ deassertion may be delayed one extra RCLK cycle.
2. $LD=HIGH$.
3. First data word latency = $t_{SKEW1} + T_{RCLK} + t_{REF}$.
4. $OE$ is LOW.
Figure 13. Write Timing (First Word Fall Through Mode)
Figure 14. Read Timing (First Word Fall Through Mode)

NOTES:
1. \( t_{SKEW1} \) is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that \( IR[1:2] \) will go LOW after one WCLK cycle plus \( t_{WFF} \). If the time between the rising edge of RCLK and the rising edge of WCLK is less than \( t_{SKEW1} \), then the \( IR[1:2] \) assertion may be delayed one extra WCLK cycle.

2. \( t_{SKEW2} \) is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that \( PAE[1:2] \) will go HIGH after one WCLK cycle plus \( t_{PAFS} \). If the time between the rising edge of RCLK and the rising edge of WCLK is less than \( t_{SKEW2} \), then the \( PAE[1:2] \) deassertion may be delayed one extra WCLK cycle.

3. \( LD = \text{HIGH} \).

4. \( n = PAE[1:2] \) offset, \( m = PAF[1:2] \) offset and \( D = \text{maximum FIFO depth} \).

5. \( D = 524,288 \) for the IDT72T36135M.

6. \( RCS = \text{LOW} \).
**Figure 15. Read Cycle and Read Chip Select Timing (First Word Fall Through Mode)**

**NOTES:**

1. $t_{SKEW1}$ is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $R[1:2]$ will go LOW after one WCLK cycle plus $t_{WFF}$. If the time between the rising edge of RCLK and the rising edge of WCLK is less than $t_{SKEW1}$, then the $R[1:2]$ assertion may be delayed one extra WCLK cycle.

2. $t_{SKEW2}$ is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $PAF[1:2]$ will go HIGH after one WCLK cycle plus $t_{PAFS}$. If the time between the rising edge of RCLK and the rising edge of WCLK is less than $t_{SKEW2}$, then the $PAF[1:2]$ deassertion may be delayed one extra WCLK cycle.

3. $I\bar{O} = \text{HIGH}$.


5. $D = 524,289$ for the IDT72T36135M.

6. $OE = \text{LOW}$.
NOTES:
1. It is very important that the REN be held HIGH for at least one cycle after RCS has gone LOW. If REN goes LOW on the same cycle as RCS or earlier, then Word, W1 will be lost, Word, W2 will be read on the output when the bus goes to LOW-Z.
2. The 1st Word will fall through to the output register regardless of REN and RCS. However, subsequent reads require that both REN and RCS be active, LOW.

Figure 16. RCS and REN Read Operation (FWFT Mode)
NOTES:
1. Retransmit setup is complete when EF[1:2] returns HIGH.
2. OE = LOW; RCS = LOW.
3. RT must be HIGH when reading from FIFO.
4. Once MARK is set, the write pointer will not increment past the 'marked' location, preventing overwrites of Retransmit data.
5. Before a “MARK” can be set there must be at least 64 number of words of data between the Write Pointer and Read Pointer locations.
6. A transition in the PAE[1:2] flag may occur one RCLK cycle earlier than shown, (on cycle 2).

Figure 17. Retransmit from Mark (IDT Standard Mode)
Figure 18. Retransmit from Mark (First Word Fall Through Mode)

NOTES:
1. Retransmit setup is complete when $\overline{OR}[1:2]$ returns LOW.
2. $OE = LOW, RCS = LOW$.
3. RT must be HIGH when reading from FIFO.
4. Once MARK is set, the write pointer will not increment past the ‘marked’ location, preventing overwrites of Retransmit data.
5. Before a “MARK” can be set there must be at least 64 number of words of data between the Write Pointer and Read Pointer locations.
6. A transition in the PAE[1:2] flag may occur one RCLK cycle earlier than shown, (on cycle 2).
Figure 19. Serial Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)

Figure 20. Parallel Loading of Programmable Flag Registers (IDT Standard and FWFT Modes)

Figure 21. Parallel Read of Programmable Flag Registers (IDT Standard and FWFT Modes)

NOTES:
1. OE = LOW.
2. The offset registers cannot be read on consecutive RCLK cycles. The read must be disabled (REN = HIGH) for a minimum of one RCLK cycle in between register accesses.
COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

NOTES:
1. m = PAF[1:2] offset.
2. D = maximum FIFO depth.
   In IDT Standard mode: D = 524,288 for the IDT72T36135M.
   In FWFT mode: D = 524,289 for the IDT72T36135M.
3. tSKEW2 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that PAF[1:2] will go HIGH (after one WCLK cycle plus tPAFS). If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW2, then the PAF[1:2] deassertion time may be delayed one extra WCLK cycle.
4. PAF[1:2] is asserted and updated on the rising edge of WCLK only.
5. Select this mode by setting PFM HIGH during Master Reset.

Figure 22. Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)

NOTES:
1. n = PAE[1:2] offset.
2. For IDT Standard mode
3. For FWFT mode.
4. tSKEW2 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that PAE[1:2] will go HIGH (after one RCLK cycle plus tPAES). If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW2, then the PAE[1:2] deassertion may be delayed one extra RCLK cycle.
5. PAE[1:2] is asserted and updated on the rising edge of WCLK only.
6. Select this mode by setting PFM HIGH during Master Reset.
7. RCS = LOW.

Figure 23. Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)
NOTES:
1. \( m = \text{PAF}[1:2] \) offset.
2. \( D = \text{maximum FIFO Depth}. \)
   In IDT Standard Mode: \( D = 524,288 \) for the IDT72T36135M.
   In FWFT Mode: \( D = 524,289 \) for the IDT72T36135M.
3. \( \text{PAF}[1:2] \) is asserted to LOW on WCLK transition and reset to HIGH on RCLK transition.
4. Select this mode by setting PFM LOW during Master Reset.
5. RCS = LOW.

**Figure 24. Asynchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)**

NOTES:
1. \( n = \text{PAE}[1:2] \) offset.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. \( \text{PAE}[1:2] \) is asserted LOW on RCLK transition and reset to HIGH on WCLK transition.
5. Select this mode by setting PFM LOW during Master Reset.
6. RCS = LOW.

**Figure 25. Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)**
NOTE:
1. OE = LOW, WEN = LOW and RCS = LOW.

*Figure 26. Asynchronous Write, Synchronous Read, Full Flag Operation (IDT Standard Mode)*

NOTE:
1. OE = LOW, WEN = LOW and RCS = LOW.

*Figure 27. Asynchronous Write, Synchronous Read, Empty Flag Operation (IDT Standard Mode)*
NOTE:
1. OE = LOW, RCS = LOW and REN = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 28. Synchronous Write, Asynchronous Read, Full Flag Operation (IDT Standard Mode)

NOTE:
1. OE = LOW, RCS = LOW and REN = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 29. Synchronous Write, Asynchronous Read, Empty Flag Operation (IDT Standard Mode)
Figure 30. Asynchronous Write, Asynchronous Read, Empty Flag Operation (IDT Standard Mode)

NOTES:
1. OE = LOW, WEN = LOW, REN = LOW and RCS = LOW
2. Asynchronous Read is available in IDT Standard Mode only.

Figure 31. Asynchronous Write, Asynchronous Read, Full Flag Operation (IDT Standard Mode)

NOTES:
1. OE = LOW, WEN = LOW, REN = LOW and RCS = LOW.
2. Asynchronous Read is available in IDT Standard Mode only.
### OPTIONAL EXPANSION CONFIGURATION

#### WIDTH EXPANSION CONFIGURATION

Word width may be increased by connecting together the control signals of multiple devices plus using external gating logic. Status flags can be gated and detected from the gate output. The EF[1:2], FF[1:2], PAE[1:2], and PAF[1:2] flags should be gated using logical gates to remove the possibility of clock skew between the two device(s) outputs.

Figure 33 demonstrates a width expansion using two IDT72T36135M devices. D0 - D35 from each device form a 72-bit wide input bus and Q0-Q35 from each device form a 72-bit wide output bus. Any word width can be attained by adding additional IDT72T36135M devices.

#### DEPTH EXPANSION CONFIGURATION (FWFT MODE ONLY)

The IDT72T36135M can easily be adapted to applications requiring depths greater than and 524,288 with an 36-bit bus width. In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next) with no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 33 shows a depth expansion using two IDT72T36135M devices.

For depth expansion mode option #1, "logical OR gates" need to be used to drive the active low input WEN and REN pins respectively from the active low output OR[1:2] and IR[1:2] pins. Two sets of OR gates are used in this mode to derive a feedback loop to the REN and WEN pins to avoid writing or reading to/from a device when the device is not ready to accept data. The 2nd row of OR gates take in the IR or OR pin’s status and allow for data to be written/read to the next FIFO in the chain. If the IR or OR pins are low, this will enable the device to accept writes or reads from the next device in line. To use this mode, the FIFO device’s clock speed depends on the added prop delay of the “OR” gates and setup time between the two FIFO devices. Example, if the “OR” gates being used have a combined 10ns propagation delay, a 1ns jitter buffer, and 1ns clock skew margin, 12ns must be taken into account during each clock cycle. For instance, a 25MHz clock has around a 40ns clock cycle. For a 45% - 55% clock duty cycle, 18ns account for 45% of the duty cycle when the clock is high. This means, 18ns – 12ns = 6ns of setup time for data to be available at the 2nd IDT FIFO which is fine considering the setup time for this FIFO is around 1.5ns.

**Figure 32. Block Diagram of 524,288 x 72 Width Expansion**

---

**NOTES:**
1. An OR gate is used for FWFT mode, AND gate for IDT mode.
2. Do not connect any output control signals directly together.
3. FIFO #1 and FIFO #2 must be the same depth, but may be different word widths.
4. PAE/PAF[1:2] optional, see section of external gating of output flags.
Designers must leave an adequate timing window to allow data to be captured by the 2nd IDT FIFO. Please take this into consideration when using this depth expansion mode to avoid data meta-stability issues.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain — no read operation is necessary but the RCLK of each FIFO must be free-running. Each time the data word appears at the outputs of one FIFO, that device's OR[1:2] line goes LOW, enabling a write to the next FIFO in line. OR gates are used to take in the considerations of the next FIFO in the chains IR pin status. If the IR pins are Low, this will enable the device to accept writes from upstream devices.

For an empty expansion configuration, the amount of time it takes for OR[1:2] of the last FIFO in the chain to go LOW (i.e. valid data to appear on the last FIFO’s outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO and the sum of the OR gate prop delays:

\[(N - 1)*(4*\text{transfer clock}) + 3*\text{TRCLK} + 2*\text{OR prop delay}\]

where \(N\) is the number of FIFOs in the expansion and TRCLK is the RCLK period. Note that extra cycles should be added for the possibility that the tsKEW1 specification is not met between RCLK and transfer clock, or RCLK and transfer clock, for the OR[1:2] flag.

The "ripple down" delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's OR[1:2] line goes LOW, enabling the preceding FIFO to write a word to fill it.

For a full expansion configuration, the amount of time it takes for IR[1:2] of the first FIFO in the chain to go LOW after a word has been read from the last FIFO is the sum of the delays for each individual FIFO and the sum of the OR gate prop delays:

\[(N - 1)*(3*\text{transfer clock}) + 2*\text{TWCLK} + 2*\text{OR prop delay}\]

where \(N\) is the number of FIFOs in the expansion and TWCLK is the WCLK period. Note that extra cycles should be added for the possibility that the tsKEW1 specification is not met between RCLK and transfer clock, or WCLK and transfer clock, for the OR[1:2] flag.

The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in data moving, as quickly as possible, to the end of the chain and free locations to the beginning of the chain.

Depth Expansion Option #2 is depicted in Figure 34, Depth Expansion Option #2. One device will be active at a time by toggling the WCS pins. Data will be written into FIFO in Ping Pong fashion. First data is written into FIFO#1, second data is written into FIFO#2, third data is written into FIFO#1, fourth data is written into FIFO#2, and so on. Data can then be read out in the same manner on the read side by toggling the RCS1 and RCS2.

![Figure 33. Depth Expansion Option #1](image)

![Figure 34. Depth Expansion Option #2](image)
## ORDERING INFORMATION

![Diagram showing ordering information structure](image)

### ORDERING INFORMATION STRUCTURE

- **Device Type (XXXXX)**
- **Power (X)**
- **Speed (XX)**
- **Package (X)**
- **Process / Temperature Range (X)**

### Process / Temperature Range Options:

- **BLANK**
- **1**
- **G**
- **BB**
- **5**
- **6**
- **L**

#### Temperature Ranges:
- **Commercial (0°C to +70°C)**
- **Industrial (-40°C to +85°C)**

### Notes:

1. Industrial temperature range product for 6ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages please contact your sales office.

## DATASHEET DOCUMENT HISTORY

- **09/01/2005** pg. 1.
- **02/28/2006** pg. 10.
- **05/29/2006** pgs. 10, 21, and 23.
- **02/04/2009** pg. 48.
- **05/10/2016** pgs. 2, 3, 4, 7, 9, 19, 24, 46, 47, and 48
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   * **Standard**: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   * **High Quality**: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or damage to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

11. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2019 Renesas Electronics Corporation. All rights reserved.