3.3 VOLT CMOS ASYNCHRONOUS FIFO

512 x 9, 1,024 x 9,
2,048 x 9, 4,096 x 9,
8,192 x 9, 16,384 x 9

IDT72V01, IDT72V02
IDT72V03, IDT72V04
IDT72V05, IDT72V06

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES:
- 3.3V family uses less power than the 5 Volt 7201/7202/7203/7204/7205/7206 family
- 512 x 9 organization (72V01)
- 1,024 x 9 organization (72V02)
- 2,048 x 9 organization (72V03)
- 4,096 X 9 organization (72V04)
- 8,192 x 9 organization (72V05)
- 16,384 X 9 organization (72V06)
- Functionally compatible with 720x family
- Low-power consumption
  — Active: 180 mW (max.)
  — Power-down: 18 mW (max.)
- 15 ns access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- Status Flags: Empty, Half-Full, Full
- Auto-retransmit capability
- Available in 32-pin PLCC
- Industrial temperature range (-40°C to +85°C) is available
- Green parts available, see ordering information

DESCRIPTION:
The IDT72V01/72V02/72V03/72V04/72V05/72V06 are dual-port FIFO memories that operate at a power supply voltage (Vcc) between 3.0V and 3.6V. Their architecture, functional operation and pin assignments are identical to those of the IDT7201/7202/7203/7204/7205/7206. These devices load and empty data on a first-in/first-out basis. They use Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the devices through the use of the Write (W) and Read (R) pins. The devices have a maximum data access time as fast as 25 ns.

The devices use a 9-bit wide data array to allow for control and parity bits at the user’s option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking. They also feature a Retransmit (RT) capability that allows for reset of the read pointer to its initial position when RT is pulsed LOW to allow for retransmission from the beginning of data. A Half-Full Flag is available in the single device mode and width expansion modes.

These FIFOs are fabricated using high-speed CMOS technology. It has been designed for those applications requiring asynchronous and simultaneous read writes in multiprocessing and rate buffer applications.

FUNCTIONAL BLOCK DIAGRAM
COMMERCIAL AND INDUSTRIAL TEMPERATURE RANGES

2

COMMERCIAL  AND  INDUSTRIAL

TEMPERATURE  RANGES

IDT72V01/72V02/72V03/72V04/72V05/72V06 3.3V ASYNCHRONOUS FIFO

512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9, 8,192 x 9 and 16,384 x 9

PIN CONFIGURATION

INDEX

D2  5
D1  6
D0  7
X1  8
FF  9
Q0  10
Q1  11
NC  12
Q2  13

D6  29
D7  28
NC  27
FL/RT  26
RS  25
EF  24
XO/HF  23
Q7  22
Q6  21

PLCC (J32-1, order code: J)

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Com'l &amp; Ind'l</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTERM</td>
<td>Terminal Voltage with Respective to GND</td>
<td>–0.5 to +7.0</td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>–55 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>–50 to +50</td>
<td>mA</td>
</tr>
</tbody>
</table>

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>Supply Voltage</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>Vih(1)</td>
<td>Input High Voltage</td>
<td>2.0</td>
<td>—</td>
<td>VCC+0.5</td>
<td>V</td>
</tr>
<tr>
<td>Vil(2)</td>
<td>Input Low Voltage</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature</td>
<td>Commercial</td>
<td>0</td>
<td>—</td>
<td>70</td>
</tr>
<tr>
<td></td>
<td>Operating Temperature</td>
<td>Industrial</td>
<td>–40</td>
<td>—</td>
<td>85</td>
</tr>
</tbody>
</table>

NOTES:
1. For RT/RS/XI input, Vih = 2.6V (commercial).
2. For RT/RS/XI input, Vih = 2.8V (military).
3. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 3.3V ± 0.3V, TA = 0°C to +70°C; Industrial: Vcc = 3.3V ± 0.3V, TA = –40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>IDT72V01</th>
<th>IDT72V02</th>
<th>IDT72V03</th>
<th>IDT72V04</th>
<th>IDT72V05</th>
<th>IDT72V06</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>ta = 15, 25, 35 ns</td>
<td>ta = 15, 25, 35 ns</td>
<td>ta = 15, 25, 35 ns</td>
<td>ta = 15, 25, 35 ns</td>
<td>ta = 15, 25, 35 ns</td>
<td>ta = 15, 25, 35 ns</td>
</tr>
<tr>
<td>IL(2)</td>
<td>Input Leakage Current (Any Input)</td>
<td>–1</td>
<td>1</td>
<td>–1</td>
<td>1</td>
<td>–1</td>
<td>1</td>
</tr>
<tr>
<td>ICO(3)</td>
<td>Output Leakage Current</td>
<td>–10</td>
<td>10</td>
<td>–10</td>
<td>10</td>
<td>–10</td>
<td>10</td>
</tr>
<tr>
<td>Vih(1)</td>
<td>Output Logic “1” Voltage (IOH = –2mA)</td>
<td>2.4</td>
<td>—</td>
<td>2.4</td>
<td>—</td>
<td>2.4</td>
<td>—</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Logic “0” Voltage (IOL = 8mA)</td>
<td>—</td>
<td>0.4</td>
<td>—</td>
<td>0.4</td>
<td>—</td>
<td>0.4</td>
</tr>
<tr>
<td>ICC(4)</td>
<td>Active Power Supply Current</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>75</td>
<td>—</td>
<td>75</td>
</tr>
<tr>
<td>ICC(2)</td>
<td>Standby Current (R=WR=RS=FL/RT=Vih)</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>5</td>
</tr>
</tbody>
</table>

NOTES:
1. Industrial temperature range product for the 25ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Measurements with 0.4 ≤ Vin ≤ VCC.
3. Ri ≥ Vih, 0.4 ≤ Vout ≤ VCC.
4. Tested with outputs open (IOUT = 0).
5. Tested at f = 20 MHz.
6. All inputs = VCC - 0.2V or GND + 0.2V.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter(1)</th>
<th>Condition</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td>Vin = 0V</td>
<td>8</td>
<td>pF</td>
</tr>
<tr>
<td>COUT</td>
<td>Output Capacitance</td>
<td>VOUT = 0V</td>
<td>8</td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTE:
1. Characterized values, not currently tested.

© 2019 Renesas Electronics Corporation
### AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 3.3V ± 0.3V, TA = 0°C to +70°C; Industrial: Vcc = 3.3V ± 0.3V, TA = –40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Commercial and Industrial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>IDT72V01L15</td>
<td>IDT72V01L25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V02L15</td>
<td>IDT72V02L25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V03L15</td>
<td>IDT72V03L25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V04L15</td>
<td>IDT72V04L25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V05L15</td>
<td>IDT72V05L25</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V06L15</td>
<td>IDT72V06L25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>fS</td>
<td>Shift Frequency</td>
<td>—</td>
<td>40</td>
<td>—</td>
<td>28.5</td>
<td>—</td>
<td>22.2</td>
<td>MHz</td>
</tr>
<tr>
<td>tRC</td>
<td>Read Cycle Time</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tA</td>
<td>Access Time</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>ns</td>
</tr>
<tr>
<td>tRR</td>
<td>Read Recovery Time</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRW</td>
<td>Read Pulse Width</td>
<td>15</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tLZ</td>
<td>Read Pulse Low to Data Bus at Low Z(3)</td>
<td>3</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>3</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tHZ</td>
<td>Read Pulse High to Data Bus at Low Z(4)</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tDV</td>
<td>Data Valid from Read Pulse High</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>5</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tHZH</td>
<td>Read Pulse High to Data Bus at High Z(5)</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>18</td>
<td>—</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>tWC</td>
<td>Write Cycle Time</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tWP</td>
<td>Write Pulse Width</td>
<td>15</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tWR</td>
<td>Write Recovery Time</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tDS</td>
<td>Data Setup Time</td>
<td>11</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>18</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tDH</td>
<td>Data Hold Time</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRS</td>
<td>Reset Cycle Time</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRSW</td>
<td>Reset Pulse Width</td>
<td>15</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRSS</td>
<td>Reset Setup Time</td>
<td>15</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRSSR</td>
<td>Reset Recovery Time</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRSC</td>
<td>Reset to Empty Flag Low</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRFH</td>
<td>Reset to Half-Full and Full Flag High</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRTF</td>
<td>Retransmit Low to Flags Valid</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRE</td>
<td>Read Low to Empty Flag Low</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRF</td>
<td>Read High to Full Flag High</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRP</td>
<td>Read Pulse Width after EF High</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRW</td>
<td>Read Pulse High to Empty Flag High</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRL</td>
<td>Write Low to Full Flag Low</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRF</td>
<td>Write Low to Half-Full Flag Low</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRF</td>
<td>Write High to Full Flag High</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRW</td>
<td>Write Pulse Width after FF High</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tXOL</td>
<td>Read/Write to XO Low</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tXOH</td>
<td>Read/Write to XO High</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>45</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tXIP</td>
<td>Pulse Width(3)</td>
<td>15</td>
<td>—</td>
<td>25</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tXIR</td>
<td>Recovery Time</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tXIS</td>
<td>Setup Time</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>10</td>
<td>—</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Timings referenced as in AC Test Conditions.
2. Industrial temperature range product for the 25ns speed grade is available as a standard device. All other speed grades are available by special order.
3. Pulse widths less than minimum value are not allowed.
4. Values guaranteed by design, not currently tested.
5. Only applies to read data flow-through mode.

### AC TEST CONDITIONS

<table>
<thead>
<tr>
<th>Input Pulse Levels</th>
<th>GND to 3.0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Rise/Fall Times</td>
<td>5ns</td>
</tr>
<tr>
<td>Input Timing Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Reference Levels</td>
<td>1.5V</td>
</tr>
<tr>
<td>Output Load</td>
<td>See Figure 1</td>
</tr>
</tbody>
</table>

*Includes scope and jig capacitances.

---

**Figure 1. Output Load**

---

© 2019 Renesas Electronics Corporation
SIGNAL DESCRIPTIONS

INPUTS:
DATA IN (D0 – D8)
Data inputs for 9-bit wide data.

CONTROLS:
RESET (RS)
Reset is accomplished whenever the Reset (RS) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the Read Enable (R) and Write Enable (W) inputs must be in the HIGH state during the window shown in Figure 2, (i.e., tRSS before the rising edge of RS) and should not change until tRSR after the rising edge of RS. Half-Full Flag (HF) will be reset to HIGH after Reset (RS).

WRITE ENABLE (W)
A write cycle is initiated on the falling edge of this input if the Full Flag (FF) is not set. Data setup and hold times must be adhered to with respect to the rising edge of the Write Enable (W). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag (HF) will be set to LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag (HF) is then reset by the rising edge of the read operation.

To prevent data overflow, the Full Flag (FF) will go LOW, inhibiting further write operations. Upon the completion of a valid read operation, the Full Flag (FF) will go HIGH after tRFF, allowing a valid write to begin. When the FIFO is full, the internal write pointer is blocked from W, so external changes in W will not affect the FIFO when it is full.

READ ENABLE (R)
A read cycle is initiated on the falling edge of the Read Enable (R) provided the Empty Flag (EF) is not set. The data is accessed on a First-In/First-Out basis, independent of any ongoing write operations. After Read Enable (R) goes HIGH, the Data Outputs (Q0 – Q8) will return to a high impedance condition until the next Read operation. When all data has been read from the FIFO, the Empty Flag (EF) will go LOW, allowing the “final” read cycle but inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the Empty Flag (EF) will go HIGH after tWER and a valid Read can then begin. When the FIFO is empty, the internal read pointer is blocked from R so external changes in R will not affect the FIFO when it is empty.

FIRST LOAD/RETRANSMIT (FL/RT)
This is a dual-purpose input. In the Depth Expansion Mode, this pin is grounded to indicate that it is the first loaded (see Operating Modes). In the Single Device Mode, this pin acts as the retransmit input. The Single Device Mode is initiated by grounding the Expansion In (XI).

These FIFOs can be made to retransmit data when the Retransmit Enable control (RT) input is pulsed LOW. A retransmit operation will set the internal read pointer to the first location and will not affect the write pointer. Read Enable (R) and Write Enable (W) must be in the HIGH state during retransmit. This feature is useful when less than 512/1,024/2,048/4,096/8,192/16,384 writes are performed between resets. The retransmit feature is not compatible with the Depth Expansion Mode and will affect the Half-Full Flag (HF), depending on the relative locations of the read and write pointers.

EXPANSION IN (XI)
This input is a dual-purpose pin. Expansion In (XI) is grounded to indicate an operation in the single device mode. Expansion In (XI) is connected to Expansion Out (XO) of the previous device in the Depth Expansion or Daisy Chain Mode.

OUTPUTS:
FULL FLAG (FF)
The Full Flag (FF) will go LOW, inhibiting further write operation, when the write pointer is one location less than the read pointer, indicating that the device is full. If the read pointer is not moved after Reset (RS), the Full Flag (FF) will go LOW after 512/1,024/2,048/4,096/8,192/16,384 writes to the IDT72V01/72V02/72V03/72V04/72V05/72V06.

EMPTY FLAG (EF)
The Empty Flag (EF) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that the device is empty.

EXPANSION OUT/HALF-FULL FLAG (XO/HF)
This is a dual-purpose output. In the single device mode, when Expansion In (XI) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled and at the falling edge of the next write operation, the Half-Full Flag (HF) will be set LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag (HF) is then reset by using rising edge of the read operation.

In the Depth Expansion Mode, Expansion In (XI) is connected to Expansion Out (XO) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse to the next device when the previous device reaches the last location of memory.

DATA OUTPUTS (Q0 – Q8)
Data outputs for 9-bit wide data. This data is in a high impedance condition whenever Read (R) is in a HIGH state.
**Figure 2. Reset**

**Figure 3. Asynchronous Write and Read Operation**

**Figure 4. Full Flag From Last Write to First Read**
Figure 5. Empty Flag From Last Read to First Write

Figure 6. Retransmit

Figure 7. Minimum Timing for an Empty Flag Coincident Read Pulse

Figure 8. Minimum Timing for a Full Flag Coincident Write Pulse
**Figure 9. Half-Full Flag Timing**

**Figure 10. Expansion Out**

**Figure 11. Expansion In**
OPERATING MODES:

Care must be taken to assure that the appropriate flag is monitored by each system (i.e. FF is monitored on the device where W is used; EF is monitored on the device where R is used). For additional information, refer to Tech Note 8: Operating FIFOs on Full and Empty Boundary Conditions and Tech Note 6: Designing with FIFOs.

SINGLE DEVICE MODE

A single IDT72V01/72V02/72V03/72V04/72V05/72V06 may be used when the application requirements are for 512/1,024/2,048/4,096/8,192/16,384 words or less. These devices are in a Single Device Configuration when the Expansion In (XI) control input is grounded (see Figure 12).

These FIFOs can easily be adapted to applications when the requirements are for greater than 512/1,024/2,048/4,096/8,192/16,384 words. Figure 14 demonstrates Depth Expansion using three IDT72V01/72V02/72V03/72V04/72V05/72V06s. Any depth can be attained by adding additional IDT72V01/72V02/72V03/72V04/72V05/72V06s. These devices operate in the Depth Expansion mode when the following conditions are met:

1. The first device must be designated by grounding the First Load (FL) control input.
2. All other devices must have FL in the HIGH state.
3. The Expansion Out (XO) pin of each device must be tied to the Expansion In (XI) pin of the next device. See Figure 14.
4. External logic is needed to generate a composite Full Flag (FF) and Empty Flag (EF). This requires the ORing of all EFs and ORing of all FFs (i.e. all must be set to generate the correct composite FF or EF). See Figure 14.
5. The Retransmit (RT) function and Half-Full Flag (HF) are not available in the Depth Expansion Mode.

For additional information, refer to Tech Note 9: Cascading FIFOs or FIFO Modules.

USAGE MODES:

WIDTH EXPANSION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags (EF, FF and HF) can be detected from any one device. Figure 13 demonstrates an 18-bit word width by using two IDT72V01/72V02/72V03/72V04/72V05/72V06s. Any word width can be attained by adding additional IDT72V01/72V02/72V03/72V04/72V05/72V06s (Figure 13).

BIDIRECTIONAL OPERATION

Applications which require data buffering between two systems (each system capable of Read and Write operations) can be achieved by pairing IDT72V01/72V02/72V03/72V04/72V05/72V06s as shown in Figure 16. Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH

Two types of flow-through modes are permitted, a read flow-through and write flow-through mode. For the read flow-through mode (Figure 17), the FIFO permits a reading of a single word after writing one word of data into an empty FIFO. The data is enabled on the bus in (tWEF + tA) ns after the rising edge of W, called the first write edge, and it remains on the bus until the R line is raised from LOW-to-HIGH, after which the bus would go into a three-state mode after tRHZ ns. The EF line would have a pulse showing temporary deassertion and then would be asserted.

In the write flow-through mode (Figure 18), the FIFO permits the writing of a single word of data immediately after reading one word of data from a full FIFO. The R line causes the FF to be deasserted but the W line being LOW causes it to be asserted again in anticipation of a new data word. On the rising edge of W, the new word is loaded in the FIFO. The W line must be toggled when FF is not asserted to write new data in the FIFO and to increment the write pointer.
Figure 12. Block Diagram of Single 512 x 9, 1,024 x 9, 2,048 x 9, 4,096 x 9, 8,192 x 9 and 16,384 x 9 FIFO

Figure 13. Block Diagram of 512 x 18, 1,024 x 18, 2,048 x 18, 4,096 x 18, 8,192 x 18 and 16,384 x 18 FIFO Memory Used in Width Expansion Mode

TABLE 1 — RESET AND RETRANSMIT

Single Device Configuration/Width Expansion Mode

<table>
<thead>
<tr>
<th>Mode</th>
<th>Inputs</th>
<th>Internal Status</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RS</td>
<td>RT</td>
<td>XI</td>
</tr>
<tr>
<td>Reset</td>
<td>0</td>
<td>X</td>
<td>0</td>
</tr>
<tr>
<td>Retransmit</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Read/Write</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

NOTE:
1. Pointer will increment if flag is HIGH

© 2019 Renesas Electronics Corporation
### TABLE 2 — RESET AND FIRST LOAD TRUTH TABLE

<table>
<thead>
<tr>
<th>Mode</th>
<th>Inputs</th>
<th>Internal Status</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RS</td>
<td>FL</td>
<td>XI</td>
</tr>
<tr>
<td>Reset First Device</td>
<td>0</td>
<td>0</td>
<td>(1)</td>
</tr>
<tr>
<td>Reset All Other Devices</td>
<td>0</td>
<td>1</td>
<td>(1)</td>
</tr>
<tr>
<td>Read/Write</td>
<td>1</td>
<td>X</td>
<td>(1)</td>
</tr>
</tbody>
</table>

**NOTE:**
1. XI is connected to XO of previous device. See Figure 14. RS = Reset Input, FL/RT = First Load/Retransmit, EF = Empty Flag Output, FF = Full Flag Output, XI = Expansion Input, HF = Half-Full Flag Output.

---

![Figure 14. Block Diagram of 1,536 x 9, 3,072 x 9, 6,144 x 9, 12,288 x 9, 24,576 x 9 and 49,152 x 9 FIFO Memory (Depth Expansion)](image)

**Figure 14.** Block Diagram of 1,536 x 9, 3,072 x 9, 6,144 x 9, 12,288 x 9, 24,576 x 9 and 49,152 x 9 FIFO Memory (Depth Expansion)

---

**NOTES:**
1. For depth expansion block see section on Depth Expansion and Figure 14.
2. For Flag detection see section on Width Expansion and Figure 13.

![Figure 15. Compound FIFO Expansion](image)

**Figure 15.** Compound FIFO Expansion
**Figure 16. Bidirectional FIFO Mode**

**Figure 17. Read Data Flow-Through Mode**

**Figure 18. Write Data Flow-Through Mode**
ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Power</th>
<th>Speed</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>XXXX</td>
<td>X</td>
<td>XXX</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

Process/Temperature Range

- Blank
- 8 Tube or Tray
- Tape and Reel
- Blank
- I Industrial (−40°C to +85°C)
- G Green
- J Plastic Leaded Chip Carrier (PLCC, J32-1)
- 15 Commercial Only
- 25 Commercial Only
- 35 Commercial Only
- L Low Power
- 72V01 512 x 9 FIFO
- 72V02 1,024 x 9 FIFO
- 72V03 2,048 x 9 FIFO
- 72V04 4,096 x 9 FIFO
- 72V05 8,192 x 9 FIFO
- 72V06 16,384 x 9 FIFO

NOTES:
1. Industrial temperature range product for the 25ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages contact your local sales office.

LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   *Standard*: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   *High Quality*: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failures or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.idt.com/go/support

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2019 Renesas Electronics Corporation. All rights reserved.