RENESAS

3.3 VOLT CMOS SyncFIFO™ 256 x 18, 512 x 18, 1,024 x 18, 2,048 x 18, and 4,096 x 18

IDT72V205, IDT72V215, IDT72V225, IDT72V235, IDT72V245

LEAD FINISH (SnPb) ARE IN EOL PROCESS - LAST TIME BUY EXPIRES JUNE 15, 2018

FEATURES:

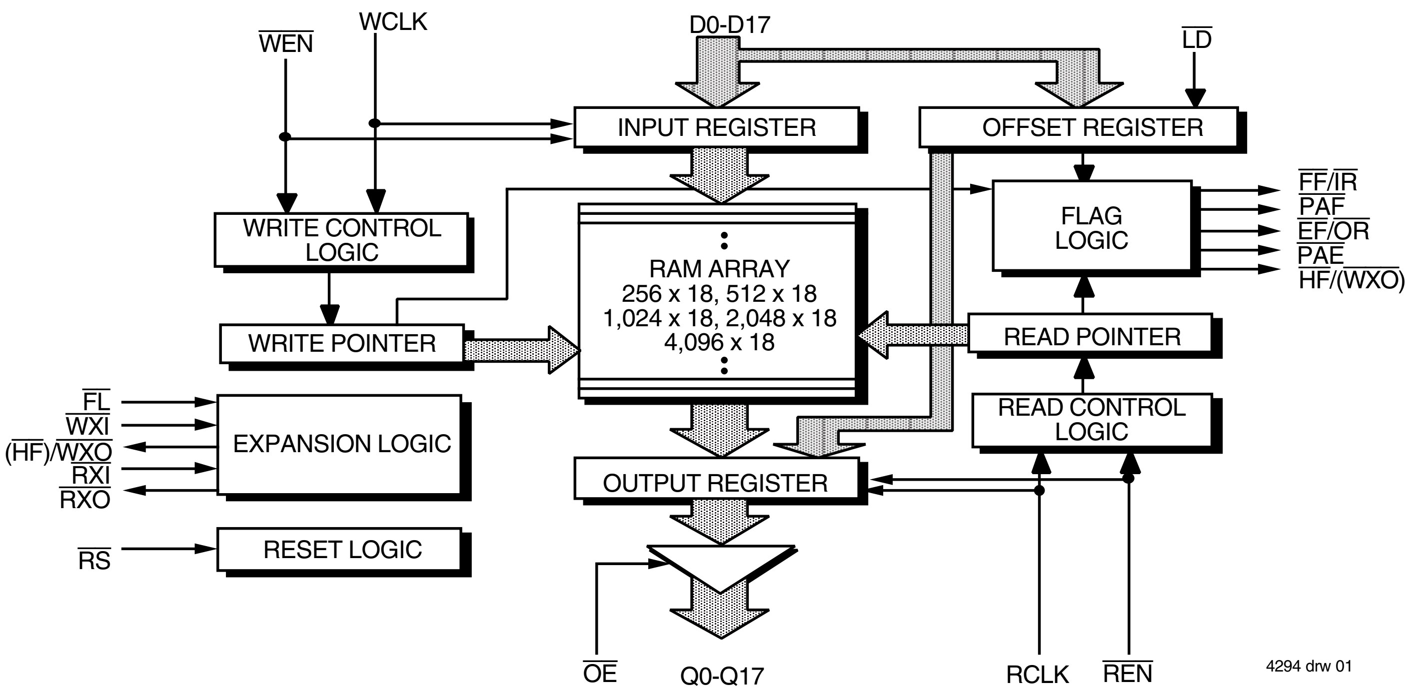
- **256 x 18-bit organization array (IDT72V205)**
- **512 x 18-bit organization array (IDT72V215)**
- **1,024 x 18-bit organization array (IDT72V225)**
- **2,048 x 18-bit organization array (IDT72V235)**
- **4,096 x 18-bit organization array (IDT72V245)**
- **10 ns read/write cycle time**
- **5V input tolerant**
- **IDT Standard or First Word Fall Through timing**
- **Single or double register-buffered Empty and Full flags**
- **Easily expandable in depth and width**
- **Asynchronous or coincident Read and Write Clocks**
- **Asynchronous or synchronous programmable Almost-Empty and Almost-Full flags with default settings**
- **Half-Full flag capability**
- **Output enable puts output data bus in high-impedance state**
- **High-performance submicron CMOS technology**
- **Available in a 64-lead thin quad flatpack (TQFP/STQFP)**
- **Industrial temperature range (–40°C to +85°C) is available**
- **Green parts available, see ordering information**

DESCRIPTION:

The IDT72V205/72V215/72V225/72V235/72V245 are functionally compatible versions of the IDT72205LB/72215LB/72225LB/72235LB/72245LB, designed to run off a 3.3V supply for exceptionally low power consumption. These devices are very high-speed, low-power First-In, First-Out (FIFO) memories with clocked read and write controls. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, Local Area Networks (LANs), and interprocessor communication.

These FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and an input enable pin (WEN). Data is read into the synchronous FIFO on every clock when WEN is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin (REN). The Read Clock(RCLK) can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual-clock operation. An Output Enable pin (OE) is provided on the read port for three-state control of the output.

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION (CONTINUED)

The synchronous FIFOs have two fixed flags, Empty Flag/Output Ready ($\overline{EF}$/$\overline{OR}$) and Full Flag/Input Ready ($\overline{FF}$/$\overline{IR}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the Load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

There are two possible timing modes of operation with these devices: IDT Standard mode and First Word Fall-Through (FWFT) mode.

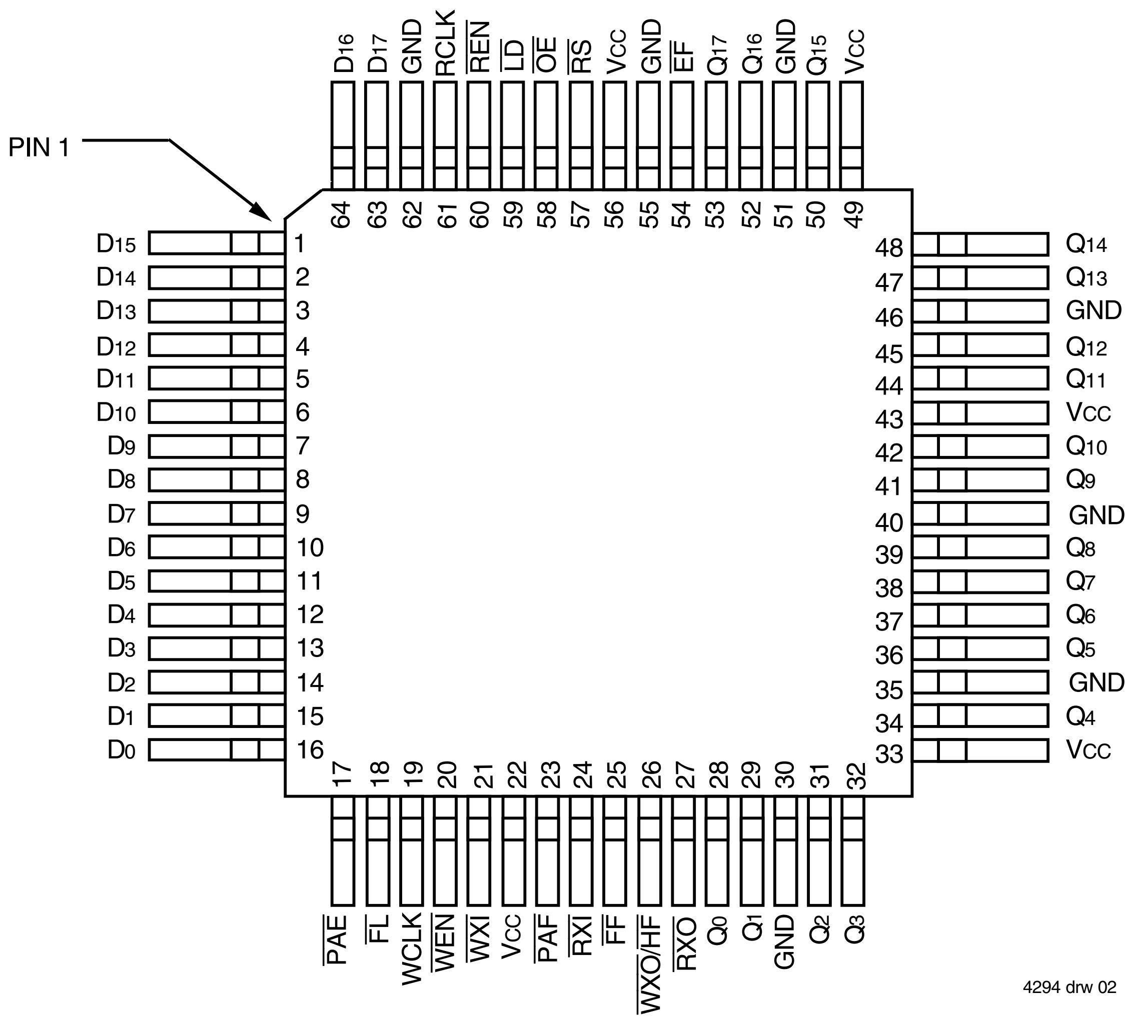
In IDT Standard Mode, the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating $\overline{REN}$ and enabling a rising RCLK edge, will shift the word from internal memory to the data output lines.

In FWFT mode, the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A $\overline{REN}$ does not have to be asserted for accessing the first word.

These devices are depth expandable using a Daisy-Chain technique or First Word Fall Through mode (FWFT). The $\overline{XI}$ and $\overline{XO}$ pins are used to expand the FIFOs. In depth expansion configuration, First Load ($\overline{FL}$) is grounded on the first device and set to HIGH for all other devices in the Daisy Chain.

The IDT72V205/72V215/72V225/72V235/72V245 are fabricated using high-speed submicron CMOS technology.

PIN CONFIGURATIONS



TQFP (PN64-1, order code: PF)
STQFP (PP64-1, order code: TF)
TOP VIEW

PIN DESCRIPTION

Symbol	Name	I/O	Description
D0–D17	Data Inputs	I	Data inputs for an 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on a LOW-to-HIGH transition of WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	When $\overline{REN}$ is LOW, data is read from the FIFO on a LOW-to-HIGH transition of RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high-impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D0–D11 is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q0–Q11 is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ together with $\overline{WXI}$ and $\overline{RXI}$ determine if the mode is IDT Standard mode or First Word Fall Through (FWFT) mode, as well as whether the $\overline{PAE}$/$\overline{PAF}$ flags are synchronous or asynchronous. (See Table 1.) In the Daisy Chain Depth Expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to HIGH for all other devices in the Daisy Chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ together with $\overline{FL}$ and $\overline{RXI}$ determine if the mode is IDT Standard mode or FWFT mode, as well as whether the $\overline{PAE}$/$\overline{PAF}$ flags are synchronous or asynchronous. (See Table 1.) In the Daisy Chain Depth Expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ together with $\overline{FL}$ and $\overline{WXI}$, determine if the mode is IDT Standard mode or FWFT mode, as well as whether the $\overline{PAE}$/$\overline{PAF}$ flags are synchronous or asynchronous. (See Table 1.) In the Daisy Chain Depth Expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{FF}$/$\overline{IR}$	Full Flag/ Input Ready	O	In the IDT Standard mode, the $\overline{FF}$ function is selected. $\overline{FF}$ indicates whether or not the FIFO memory is full. In the FWFT mode, the $\overline{IR}$ function is selected. $\overline{IR}$ indicates whether or not there is space available for writing to the FIFO memory.
$\overline{EF}$/$\overline{OR}$	Empty Flag/ Output Ready	O	In the IDT Standard mode, the $\overline{EF}$ function is selected. $\overline{EF}$ indicates whether or not the FIFO memory is empty. In FWFT mode, the $\overline{OR}$ function is selected. $\overline{OR}$ indicates whether or not there is valid data available at the outputs.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost-empty based on the offset programmed into the FIFO. The default offset at reset is 31 from empty for IDT72V205, 63 from empty for IDT72V215, and 127 from empty for IDT72V225/ 72V235/72V245.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost-full based on the offset programmed into the FIFO. The default offset at reset is 31 from full for IDT72V205, 63 from full for IDT72V215, and 127 from full for IDT72V225/72V235/72V245.
$\overline{WXO}$/$\overline{HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q0–Q17	Data Outputs	O	Data outputs for an 18-bit bus.
VCC	Power		+3.3V power supply pins.
GND	Ground		Seven ground pins.

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Unit
VTERM[2]	Terminal Voltage with respect to GND	–0.5 to +5	V
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	–50 to +50	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VCC terminal only.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage Commercial/Industrial	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage Commercial/Industrial	2.0	—	5.5	V
VIL[1]	Input Low Voltage Commercial/Industrial	-0.5	—	0.8	V
TA	Operating Temperature Commercial	0	—	70	°C
TA	Operating Temperature Industrial	-40	—	85	°C

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 3.3V ± 0.3V, TA = 0°C to +70°C; Industrial: VCC = 3.3V ± 0.3V, TA = -40°C to +85°C)

Symbol	Parameter	IDT72V205 IDT72V215 IDT72V225 IDT72V235 IDT72V245 Commercial & Industrial[1] tCLK = 10, 15, 20 ns			Unit
		Min.	Typ.	Max.	
ILI[2]	Input Leakage Current (any input)	–1	—	1	µA
ILO[3]	Output Leakage Current	–10	—	10	µA
VOH	Output Logic "1" Voltage, IOH = –2 mA	2.4	—	—	V
VOL	Output Logic "0" Voltage, IOL = 8 mA	—	—	0.4	V
ICC1[4,5,6]	Active Power Supply Current	—	—	30	mA
ICC2[4,7]	Standby Current	—	—	5	mA

NOTES:
1. Industrial Temperature Range Product for the 15ns speed grade is available as a standard device.
2. Measurements with 0.4 ≤ VIN ≤ VCC.
3. $\overline{OE}$ ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
4. Tested with outputs disabled (IOUT = 0).
5. RCLK and WCLK toggle at 20 MHZ and data inputs switch at 10 MHz.
6. Typical ICC1 = 2.04 + 0.88*fS + 0.02*CL*fS (in mA).
   These equations are valid under the following conditions:
   VCC = 3.3V, TA = 25°C, fS = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fS/2, CL = capacitive load (in pF).
7. All Inputs = VCC - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN[2]	Input Capacitance	VIN = 0V	10	pF
COUT[1,2]	Output Capacitance	VOUT = 0V	10	pF

NOTES:
1. With output deselected, ($\overline{OE}$ ≥ VIH).
2. Characterized values, not currently tested.

AC ELECTRICAL CHARACTERISTICS

(Commercial: VCC = 3.3V ± 0.3V, TA = 0°C to +70°C; Industrial: VCC = 3.3V ± 0.3V, TA = -40°C to +85°C)

Symbol	Parameter	Commercial IDT72V205L10 IDT72V215L10 IDT72V225L10 IDT72V235L10 IDT72V245L10		Com'l & Ind'l[1] IDT72V205L15 IDT72V215L15 IDT72V225L15 IDT72V235L15 IDT72V245L15		Commercial IDT72V205L20 IDT72V215L20 IDT72V225L20 IDT72V235L20 IDT72V245L20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency	—	100	—	66.7	—	50	MHz
t_A	Data Access Time	2	6.5	2	10	2	12	ns
t_{CLK}	Clock Cycle Time	10	—	15	—	20	—	ns
t_{CLKH}	Clock HIGH Time	4.5	—	6	—	8	—	ns
t_{CLKL}	Clock LOW Time	4.5	—	6	—	8	—	ns
t_{DS}	Data Set-up Time	3	—	4	—	5	—	ns
t_{DH}	Data Hold Time	0.5	—	1	—	1	—	ns
t_{ENS}	Enable Set-up Time	3	—	4	—	5	—	ns
t_{ENH}	Enable Hold Time	0.5	—	1	—	1	—	ns
t_{RS}	Reset Pulse Width[2]	10	—	15	—	20	—	ns
t_{RSS}	Reset Set-up Time	8	—	10	—	12	—	ns
t_{RSR}	Reset Recovery Time	8	—	10	—	12	—	ns
t_{RSF}	Reset to Flag and Output Time	—	15	—	15	—	20	ns
t_{OLZ}	Output Enable to Output in Low-Z[3]	0	—	0	—	0	—	ns
t_{OE}	Output Enable to Output Valid	—	6	3	8	3	10	ns
t_{OHZ}	Output Enable to Output in High-Z[3]	1	6	3	8	3	10	ns
t_{WFF}	Write Clock to Full Flag	—	6.5	—	10	—	12	ns
t_{REF}	Read Clock to Empty Flag	—	6.5	—	10	—	12	ns
t_{PAFA}	Clock to Asynchronous Programmable Almost-Full Flag	—	17	—	20	—	22	ns
t_{PAFS}	Write Clock to Synchronous Programmable Almost-Full Flag	—	8	—	10	—	12	ns
t_{PAEA}	Clock to Asynchronous Programmable Almost-Empty Flag	—	17	—	20	—	22	ns
t_{PAES}	Read Clock to Synchronous Programmable Almost-Empty Flag	—	8	—	10	—	12	ns
t_{HF}	Clock to Half-Full Flag	—	17	—	20	—	22	ns
t_{XO}	Clock to Expansion Out	—	6.5	—	10	—	12	ns
t_{XI}	Expansion In Pulse Width	3	—	6.5	—	8	—	ns
t_{XIS}	Expansion In Set-Up Time	3	—	5	—	8	—	ns
t_{SKEW1}	Skew time between Read Clock & Write Clock for $\overline{FF}/\overline{IR}$ and $\overline{EF}/\overline{OR}$	5	—	6	—	8	—	ns
t_{SKEW2}[4]	Skew time between Read Clock & Write Clock for $\overline{PAE}$ and $\overline{PAF}$	14	—	18	—	20	—	ns

NOTES:
1. Industrial temperature range product for the 15ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.
4. t_{SKEW2} applies to synchronous $\overline{PAE}$ and synchronous $\overline{PAF}$ only.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

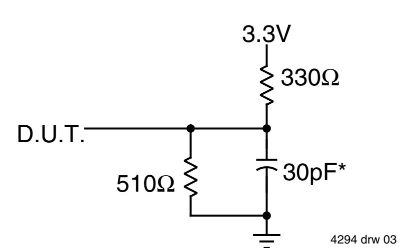


Figure 1. Output Load

* Includes jig and scope capacitances.

FUNCTIONAL DESCRIPTION

TIMING MODES: IDT STANDARD vs FIRST WORD FALL THROUGH (FWFT) MODE

The IDT72V205/72V215/72V225/72V235/72V245 support two different timing modes of operation. The selection of which mode will operate is determined during configuration at Reset (RS). During a RS operation, the First Load (FL), Read Expansion Input (RXI), and Write Expansion Input (WXI) pins are used to select the timing mode per the truth table shown in Table 3. In IDT Standard Mode, the first word written to an empty FIFO will not appear on the data output lines unless a specific read operation is performed. A read operation, which consists of activating Read Enable (REN) and enabling a rising Read Clock (RCLK) edge, will shift the word from internal memory to the data output lines. In FWFT mode, the first word written to an empty FIFO is clocked directly to the data output lines after three transitions of the RCLK signal. A REN does not have to be asserted for accessing the first word.

Various signals, both input and output signals operate differently depending on which timing mode is in effect.

IDT STANDARD MODE

In this mode, the status flags, FF, PAF, HF, PAE, and EF operate in the manner outlined in Table 1. To write data into to the FIFO, Write Enable (WEN) must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of the Write Clock (WCLK). After the first write is performed, the Empty Flag (EF) will go HIGH. Subsequent writes will continue to fill up the FIFO. The Programmable Almost-Empty flag (PAE) will go HIGH after n + 1 words have been loaded into the FIFO, where n is the empty offset value. The default setting for this value is stated in the footnote of Table 1. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

If one continued to write data into the FIFO, and we assumed no read operations were taking place, the Half-Full Flag (HF) would toggle to LOW once the 129th (72V205), 257th (72V215), 513th (72V225), 1,025th (72V235), and 2,049th (72V245) word respectively was written into the FIFO. Continuing to write data into the FIFO will cause the Programmable Almost-Full Flag (PAF) to go LOW. Again, if no reads are performed, the PAF will go LOW after (256-m) writes for the IDT72V205, (512-m) writes for the IDT72V215, (1,024-m) writes for the IDT72V225, (2,048-m) writes for the IDT72V235 and (4,096–m) writes for the IDT72V245. The offset "m" is the full offset value. This parameter is also user programmable. See section on Programmable Flag Offset Loading. If there is no full offset specified, the PAF will be LOW when the device is 31 away from completely full for IDT72V205, 63 away from completely full for IDT72V215, and 127 away from completely full for the IDT72V225/72V235/72V245.

When the FIFO is full, the Full Flag (FF) will go LOW, inhibiting further write operations. If no reads are performed after a reset, FF will go LOW after D writes to the FIFO. D = 256 writes for the IDT72V205, 512 for the IDT72V215, 1,024 for the IDT72V225, 2,048 for the IDT72V235 and 4,096 for the IDT72V245, respectively.

If the FIFO is full, the first read operation will cause FF to go HIGH. Subsequent read operations will cause PAF and the Half-Full Flag (HF) to go HIGH at the conditions described in Table 1. If further read operations occur, without write operations, the Programmable Almost-Empty Flag (PAE) will go LOW when there are n words in the FIFO, where n is the empty offset value. If there is no empty offset specified, the PAE will be LOW when the device is 31 away from completely empty for IDT72V205, 63 away from completely empty for IDT72V215, and 127 away from completely empty for IDT72V225/72V235/72V245. Continuing read operations will cause the FIFO to be empty. When the last word has been read from the FIFO, the EF will go LOW inhibiting further read operations. REN is ignored when the FIFO is empty.

FIRST WORD FALL THROUGH MODE (FWFT)

In this mode, the status flags, IR, PAF, HF, PAE, and OR operate in the manner outlined in Table 2. To write data into to the FIFO, WEN must be LOW. Data presented to the DATA IN lines will be clocked into the FIFO on subsequent transitions of WCLK. After the first write is performed, the Output Ready (OR) flag will go LOW. Subsequent writes will continue to fill up the FIFO. PAE will go HIGH after n + 2 words have been loaded into the FIFO, where n is the empty offset value. The default setting for this value is stated in the footnote of Table 2. This parameter is also user programmable. See section on Programmable Flag Offset Loading.

If one continued to write data into the FIFO, and we assumed no read operations were taking place, the HF would toggle to LOW once the 130th (72V205), 258th (72V215), 514th (72V225), 1,026th (72V235), and 2,050th (72V245) word respectively was written into the FIFO. Continuing to write data into the FIFO will cause the PAF to go LOW. Again, if no reads are performed, the PAF will go LOW after (257-m) writes for the IDT72V205, (513-m) writes for the IDT72V215, (1,025-m) writes for the IDT72V225, (2,049–m) writes for the IDT72V235 and (4,097–m) writes for the IDT72V245, where m is the full offset value. The default setting for this value is stated in the footnote of Table 2.

When the FIFO is full, the Input Ready (IR) flag will go HIGH, inhibiting further write operations. If no reads are performed after a reset, IR will go HIGH after D writes to the FIFO. D = 257 writes for the IDT72V205, 513 for the IDT72V215, 1,025 for the IDT72V225, 2,049 for the IDT72V235 and 4,097 for the IDT72V245. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

If the FIFO is full, the first read operation will cause the IR flag to go LOW. Subsequent read operations will cause the PAF and HF to go HIGH at the conditions described in Table 2. If further read operations occur, without write operations, the PAE will go LOW when there are n + 1 words in the FIFO, where n is the empty offset value. If there is no empty offset specified, the PAE will be LOW when the device is 32 away from completely empty for IDT72V205, 64 away from completely empty for IDT72V215, and 128 away from completely empty for IDT72V225/72V235/72V245. Continuing read operations will cause the FIFO to be empty. When the last word has been read from the FIFO, OR will go HIGH inhibiting further read operations. REN is ignored when the FIFO is empty.

PROGRAMMABLE FLAG LOADING

Full and Empty flag offset values can be user programmable. The IDT72V205/72V215/72V225/72V235/72V245 has internal registers for these offsets. Default settings are stated in the footnotes of Table 1 and Table 2. Offset values are loaded into the FIFO using the data input lines D_0-D_{11}. To load the offset registers, the Load (LD) pin and WEN pin must be held LOW. Data present on D_0-D_{11} will be transferred in to the Empty Offset register on the first LOW-to-HIGH transition of WCLK. By continuing to hold the LD and WEN pin low, data present on D_0-D_{11} will be transferred into the Full Offset register on the next transition of the WCLK. The third transition again writes to the Empty Offset register. Writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the LD pin HIGH, the FIFO is returned to normal read/write operation. When the LD pin and WEN are again set LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the data output lines Q0-Q11 when the LD pin is set LOW and REN is set LOW. Data can then be read on the next LOW-to-HIGH transition of RCLK. The first transition of RCLK will present the empty offset value to the data output lines. The next transition of RCLK will present the full offset value. Offset register content can be read out in the IDT Standard mode only. It cannot be read in the FWFT mode.

SYNCHRONOUS vs ASYNCHRONOUS PROGRAMMABLE FLAG TIMING SELECTION

The IDT72V205/72V215/72V225/72V235/72V245 can be configured during the "Configuration at Reset" cycle described in Table 3 with either asynchronous or synchronous timing for PAE and PAF flags.

If asynchronous PAE/PAF configuration is selected (as per Table 3), the PAE is asserted LOW on the LOW-to-HIGH transition of RCLK. PAE is reset to HIGH on the LOW-to-HIGH transition of WCLK. Similarly, the PAF is asserted LOW on the LOW-to-HIGH transition of WCLK and PAF is reset to HIGH on the LOW-to-HIGH transition of RCLK. For detail timing diagrams, see Figure 13 for asynchronous PAE timing and Figure 14 for asynchronous PAF timing.

If synchronous PAE/PAF configuration is selected , the PAE is asserted and updated on the rising edge of RCLK only and not WCLK. Similarly, PAF is asserted and updated on the rising edge of WCLK only and not RCLK. For detail timing diagrams, see Figure 22 for synchronous PAE timing and Figure 23 for synchronous PAF timing.

REGISTER-BUFFERED FLAG OUTPUT SELECTION

The IDT72V205/72V215/72V225/72V235/72V245 can be configured during the "Configuration at Reset" cycle described in Table 4 with single, double or triple register-buffered flag output signals. The various combinations available are described in Table 4 and Table 5. In general, going from single to double or triple buffered flag outputs removes the possibility of metastable flag indications on boundary states (i.e, empty or full conditions). The trade-off is the addition of clock cycle delays for the respective flag to be asserted. Not all combinations of register-buffered flag outputs are supported. Register-buffered outputs apply to the Empty Flag and Full Flag only. Partial flags are not effected. Table 4 and Table 5 summarize the options available.

TABLE 1 — STATUS FLAGS FOR IDT STANDARD MODE

Number of Words in FIFO									
IDT72V205	IDT72V215	IDT72V225	IDT72V235	IDT72V245	FF	PAF	HF	PAE	EF
0	0	0	0	0	H	H	H	L	L
1 to n(1)	1 to n(1)	1 to n(1)	1 to n(1)	1 to n(1)	H	H	H	L	H
(n + 1) to 128	(n + 1) to 256	(n + 1) to 512	(n + 1) to 1,024	(n + 1) to 2,048	H	H	H	H	H
129 to (256-(m+1))(2)	257 to (512-(m+1))(2)	513 to (1,024-(m+1))(2)	1,025 to (2,048-(m+1))(2)	2,049 to (4,096-(m+1))(2)	H	H	L	H	H
(256-m) to 255	(512-m) to 511	(1,024-m) to 1,023	(2,048-m) to 2,047	(4,096-m) to 4,095	H	L	L	H	H
256	512	1,024	2,048	4,096	L	L	L	H	H

NOTES:
1. n = Empty Offset (Default Values : IDT72V205 n = 31, IDT72V215 n = 63, IDT72V225/72V235/72V245 n = 127)
2. m = Full Offset (Default Values : IDT72V205 m = 31, IDT72V215 m = 63, IDT72V225/72V235/72V245 m = 127)

TABLE 2 — STATUS FLAGS FOR FWFT MODE

Number of Words in FIFO									
IDT72V205	IDT72V215	IDT72V225	IDT72V235	IDT72V245	IR	PAF	HF	PAE	OR
0	0	0	0	0	L	H	H	L	H
1 to (n + 1)(1)	1 to (n + 1)(1)	1 to (n + 1)(1)	1 to (n + 1)(1)	1 to (n + 1)(1)	L	H	H	L	L
(n + 2) to 129	(n + 2) to 257	(n + 2) to 513	(n + 2) to 1,025	(n + 2) to 2,049	L	H	H	H	L
130 to (257-(m+1))(2)	258 to (513-(m+1))(2)	514 to (1,025-(m+1))(2)	1,026 to (2,049-(m+1))(2)	2,050 to (4,097-(m+1))(2)	L	H	L	H	L
(257-m) to 256	(513-m) to 512	(1,025-m) to 1,024	(2,049-m) to 2,048	(4,097-m) to 4,096	L	L	L	H	L
257	513	1,025	2,049	4,097	H	L	L	H	L

NOTES:
1. n = Empty Offset (Default Values : IDT72V205 n = 31, IDT72V215 n = 63, IDT72V225/72V235/72V245 n = 127)
2. m = Full Offset (Default Values : IDT72V205 m = 31, IDT72V215 m = 63, IDT72V225/72V235/72V245 m = 127)

TABLE 3 — TRUTH TABLE FOR CONFIGURATION AT RESET

$\overline{FL}$	$\overline{RXI}$	$\overline{WXI}$	$\overline{EF}/\overline{OR}$	$\overline{FF}/\overline{IR}$	$\overline{PAE}$, $\overline{PAF}$	FIFO Timing Mode
0	0	0	Single register-buffered Empty Flag	Single register-buffered Full Flag	Asynchronous	Standard
0	0	1	Triple register-buffered Output Ready Flag	Double register-buffered Input Ready Flag	Asynchronous	FWFT
0	1	0	Double register-buffered Empty Flag	Double register-buffered Full Flag	Asynchronous	Standard
0(1)	1	1	Single register-buffered Empty Flag	Single register-buffered Full Flag	Asynchronous	Standard
1	0	0	Single register-buffered Empty Flag	Single register-buffered Full Flag	Synchronous	Standard
1	0	1	Triple register-buffered Output Ready Flag	Double register-buffered Input Ready Flag	Synchronous	FWFT
1	1	0	Double register-buffered Empty Flag	Double register-buffered Full Flag	Synchronous	Standard
1(2)	1	1	Single register-buffered Empty Flag	Single register-buffered Full Flag	Synchronous	Standard

NOTES:

1. In a daisy-chain depth expansion, $\overline{FL}$ is held LOW for the "first load device". The $\overline{RXI}$ and $\overline{WXI}$ inputs are driven by the corresponding $\overline{RXO}$ and $\overline{WXO}$ outputs of the preceding device.
2. In a daisy-chain depth expansion, $\overline{FL}$ is held HIGH for members of the expansion other than the "first load device". The $\overline{RXI}$ and $\overline{WXI}$ inputs are driven by the corresponding $\overline{RXO}$ and $\overline{WXO}$ outputs of the preceding device.

TABLE 4 — REGISTER-BUFFERED FLAG OUTPUT OPTIONS — IDT STANDARD MODE

Empty Flag ($\overline{EF}$) Buffered Output	Full Flag ($\overline{FF}$) Buffered Output	Partial Flags Timing Mode	Programming at Reset			Flag Timing Diagrams
			$\overline{FL}$	$\overline{RXI}$	$\overline{WXI}$	
Single	Single	Asynch	0	0	0	Figure 9, 10
Single	Single	Sync	1	0	0	Figure 9, 10
Double	Double	Asynch	0	1	0	Figure 24, 26
Double	Double	Synch	1	1	0	Figure 24, 26

TABLE 5 — REGISTER-BUFFERED FLAG OUTPUT OPTIONS — FWFT MODE

Output Ready ($\overline{OR}$)	Input Ready ($\overline{IR}$)	Partial Flags	Programming at Reset			Flag Timing Diagrams
			$\overline{FL}$	$\overline{RXI}$	$\overline{WXI}$	
Triple	Double	Asynch	0	0	1	Figure 27
Triple	Double	Sync	1	0	1	Figure 20, 21

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})

Data inputs for 18-bit wide data.

CONTROLS:

RESET (RS)

Reset is accomplished whenever the Reset (RS) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Half-Full Flag (HF) and Programmable Almost-Full Flag (PAF) will be reset to HIGH after tRSF. The Programmable Almost-Empty Flag (PAE) will be reset to LOW after tRSF. The Full Flag (FF) will reset to HIGH. The Empty Flag (EF) will reset to LOW in IDT Standard mode but will reset to HIGH in FWFT mode. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

WRITE CLOCK (WCLK)

A write cycle is initiated on the LOW-to-HIGH transition of the Write Clock (WCLK). Data setup and hold times must be met with respect to the LOW-to-HIGH transition of WCLK.

The Write and Read Clocks can be asynchronous or coincident.

WRITE ENABLE (WEN)

When the WEN input is LOW, data may be loaded into the FIFO RAM array on the rising edge of every WCLK cycle if the device is not full. Data is stored in the RAM array sequentially and independently of any ongoing read operation.

When WEN is HIGH, no new data is written in the RAM array on each WCLK cycle.

To prevent data overflow in the IDT Standard Mode, FF will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, FF will go HIGH allowing a write to occur. The FF flag is updated on the rising edge of WCLK.

To prevent data overflow in the FWFT mode, IR will go HIGH, inhibiting further write operations. Upon the completion of a valid read cycle, IR will go LOW allowing a write to occur. The IR flag is updated on the rising edge of WCLK.

WEN is ignored when the FIFO is full in either FWFT or IDT Standard mode.

READ CLOCK (RCLK)

Data can be read on the outputs on the LOW-to-HIGH transition of the Read Clock (RCLK), when Output Enable (OE) is set LOW.

The Write and Read Clocks can be asynchronous or coincident.

READ ENABLE (REN)

When Read Enable is LOW, data is loaded from the RAM array into the output register on the rising edge of every RCLK cycle if the device is not empty.

When the REN input is HIGH, the output register holds the previous data and no new data is loaded into the output register. The data outputs Q_0-Q_n maintain the previous data value.

In the IDT Standard mode, every word accessed at Q_n, including the first word written to an empty FIFO, must be requested using REN. When the last word has been read from the FIFO, the Empty Flag (EF) will go LOW, inhibiting further read operations. REN is ignored when the FIFO is empty. Once a write is performed, EF will go HIGH allowing a read to occur. The EF flag is updated on the rising edge of RCLK.

In the FWFT mode, the first word written to an empty FIFO automatically goes to the outputs Q_n, on the third valid LOW to HIGH transition of RCLK + tSKEW after the first write. REN does not need to be asserted LOW. In order to access all other words, a read must be executed using REN. The RCLK LOW to HIGH transition after the last word has been read from the FIFO, Output Ready (OR) will go HIGH with a true read (RCLK with REN = LOW), inhibiting further read operations. REN is ignored when the FIFO is empty.

OUTPUT ENABLE (OE)

When Output Enable (OE) is enabled (LOW), the parallel output buffers receive data from the output register. When OE is disabled (HIGH), the Q output data bus is in a high-impedance state.

LOAD (LD)

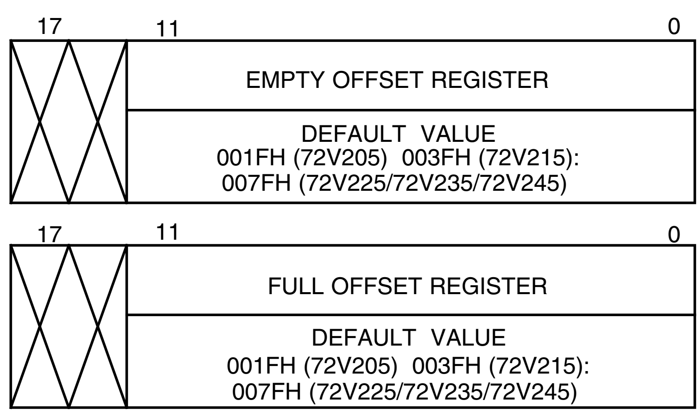
The IDT72V205/72V215/72V225/72V235/72V245 devices contain two 12-bit offset registers with data on the inputs, or read on the outputs. When the Load (LD) pin is set LOW and WEN is set LOW, data on the inputs D0-D11 is written into the Empty Offset register on the first LOW-to-HIGH transition of the Write Clock (WCLK). When the LD pin and WEN are held LOW then data is written into the Full Offset register on the second LOW-to-HIGH transition of WCLK. The third transition of WCLK again writes to the Empty Offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the LD pin HIGH, the FIFO is returned to normal read/write operation. When the LD pin is set LOW, and WEN is LOW, the next offset register in sequence is written.

LD	WEN	WCLK	Selection
0	0		Writing to offset registers: Empty Offset Full Offset
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

NOTE:
1. The same selection sequence applies to reading from the registers. REN is enabled and read is performed on the LOW-to-HIGH transition of RCLK.

Figure 2. Writing to Offset Registers



NOTE:
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

When the $\overline{LD}$ pin is LOW and $\overline{WEN}$ is HIGH, the WCLK input is disabled; then a signal at this input can neither increment the write offset register pointer, nor execute a write.

The contents of the offset registers can be read on the output lines when the $\overline{LD}$ pin is set LOW and $\overline{REN}$ is set LOW; then, data can be read on the LOW-to-HIGH transition of the Read Clock (RCLK). The act of reading the control registers employs a dedicated read offset register pointer. (The read and write pointers operate independently). Offset register content can be read out in the IDT Standard mode only. It is inhibited in the FWFT mode.

A read and a write should not be performed simultaneously to the offset registers.

FIRST LOAD ($\overline{FL}$)

For the single device mode, see Table 3 for additional information. In the Daisy Chain Depth Expansion configuration, $\overline{FL}$ is grounded to indicate it is the first device loaded and is set to HIGH for all other devices in the Daisy Chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXI}$)

This is a dual purpose pin. For single device mode, see Table 3 for additional information. $\overline{WXI}$ is connected to Write Expansion Out ($\overline{WXO}$) of the previous device in the Daisy Chain Depth Expansion mode.

READ EXPANSION INPUT ($\overline{RXI}$)

This is a dual purpose pin. For single device mode, see Table 3 for additional information. $\overline{RXI}$ is connected to Read Expansion Out ($\overline{RXO}$) of the previous device in the Daisy Chain Depth Expansion mode.

OUTPUTS:

FULL FLAG/INPUT READY ($\overline{FF}/\overline{IR}$)

This is a dual purpose pin. In IDT Standard mode, the Full Flag ($\overline{FF}$) function is selected. When the FIFO is full, $\overline{FF}$ will go LOW, inhibiting further write operations. When $\overline{FF}$ is HIGH, the FIFO is not full. If no reads are performed after a reset, $\overline{FF}$ will go LOW after D writes to the FIFO. D = 256 writes for the IDT72V205, 512 for the IDT72V215, 1,024 for the IDT72V225, 2,048 for the IDT72V235 and 4,096 for the IDT72V245.

In FWFT mode, the Input Ready ($\overline{IR}$) function is selected. $\overline{IR}$ goes LOW when memory space is available for writing in data. When there is no longer any free space left, $\overline{IR}$ goes HIGH, inhibiting further write operations.

$\overline{IR}$ will go HIGH after D writes to the FIFO. D = 257 writes for the IDT72V205, 513 for the IDT72V215, 1,025 for the IDT72V225, 2,049 for the IDT72V235 and 4,097 for the IDT72V245. Note that the additional word in FWFT mode is due to the capacity of the memory plus output register.

$\overline{FF}/\overline{IR}$ is synchronous and updated on the rising edge of WCLK.

EMPTY FLAG/OUTPUT READY ($\overline{EF}/\overline{OR}$)

This is a dual purpose pin. In the IDT Standard mode, the Empty Flag ($\overline{EF}$) function is selected. When the FIFO is empty, $\overline{EF}$ will go LOW, inhibiting further read operations. When $\overline{EF}$ is HIGH, the FIFO is not empty.

In FWFT mode, the Output Ready ($\overline{OR}$) function is selected. $\overline{OR}$ goes LOW at the same time that the first word written to an empty FIFO appears valid on the outputs. $\overline{OR}$ stays LOW after the RCLK LOW to HIGH transition that shifts the last word from the FIFO memory to the outputs. $\overline{OR}$ goes HIGH only with a true read (RCLK with $\overline{REN}$ = LOW). The previous data stays at the outputs, indicating the last word was read. Further data reads are inhibited until $\overline{OR}$ goes LOW again.

$\overline{EF}/\overline{OR}$ is synchronous and updated on the rising edge of RCLK.

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when FIFO reaches the almost-full condition. In IDT Standard mode, if no reads are performed after Reset ($\overline{RS}$), the $\overline{PAF}$ will go LOW after (256-m) writes for the IDT72V205, (512-m) writes for the IDT72V215, (1,024-m) writes for the IDT72V225, (2,048–m) writes for the IDT72V235 and (4,096–m) writes for the IDT72V245. The offset "m" is defined in the Full Offset register.

In FWFT mode, if no reads are performed, $\overline{PAF}$ will go LOW after 257-m for the IDT72V205, 513-m for the IDT72V215, 1,025 for the IDT72V225, 2,049 for the IDT72V235 and 4,097 for the IDT72V245. The default values for m are noted in Table 1 and 2.

If asynchronous $\overline{PAF}$ configuration is selected, the $\overline{PAF}$ is asserted LOW on the LOW-to-HIGH transition of the Write Clock (WCLK). $\overline{PAF}$ is reset to HIGH on the LOW-to-HIGH transition of the Read Clock (RCLK). If synchronous $\overline{PAF}$ configuration is selected (see Table 3), the $\overline{PAF}$ is updated on the rising edge of WCLK.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The $\overline{PAE}$ flag will go LOW when the FIFO reaches the almost-empty condition. In IDT Standard mode, $\overline{PAE}$ will go LOW when there are n words or less in the FIFO. In FWFT mode, the $\overline{PAE}$ will go LOW when there are n + 1 words or less in the FIFO. The offset "n" is defined as the empty offset. The default values for n are noted in Table 1 and 2.

If there is no empty offset specified, the Programmable Almost-Empty Flag ($\overline{PAE}$) will be LOW when the device is 31 away from completely empty for IDT72V205, 63 away from completely empty for IDT72V215, and 127 away from completely empty for IDT72V225/72V235/72V245.

If asynchronous $\overline{PAE}$ configuration is selected, the $\overline{PAE}$ is asserted LOW on the LOW-to-HIGH transition of the Read Clock (RCLK). $\overline{PAE}$ is reset to HIGH on the LOW-to-HIGH transition of the Write Clock (WCLK). If synchronous $\overline{PAE}$ configuration is selected (see Table 3), the $\overline{PAE}$ is updated on the rising edge of RCLK.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when Write Expansion In ($\overline{WXI}$) and/or Read Expansion In ($\overline{RXI}$) are grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the LOW-to-HIGH transition of the next write cycle, the Half-Full Flag goes LOW and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to HIGH by the LOW-to-HIGH transition of the Read Clock (RCLK). The $\overline{HF}$ is asynchronous.

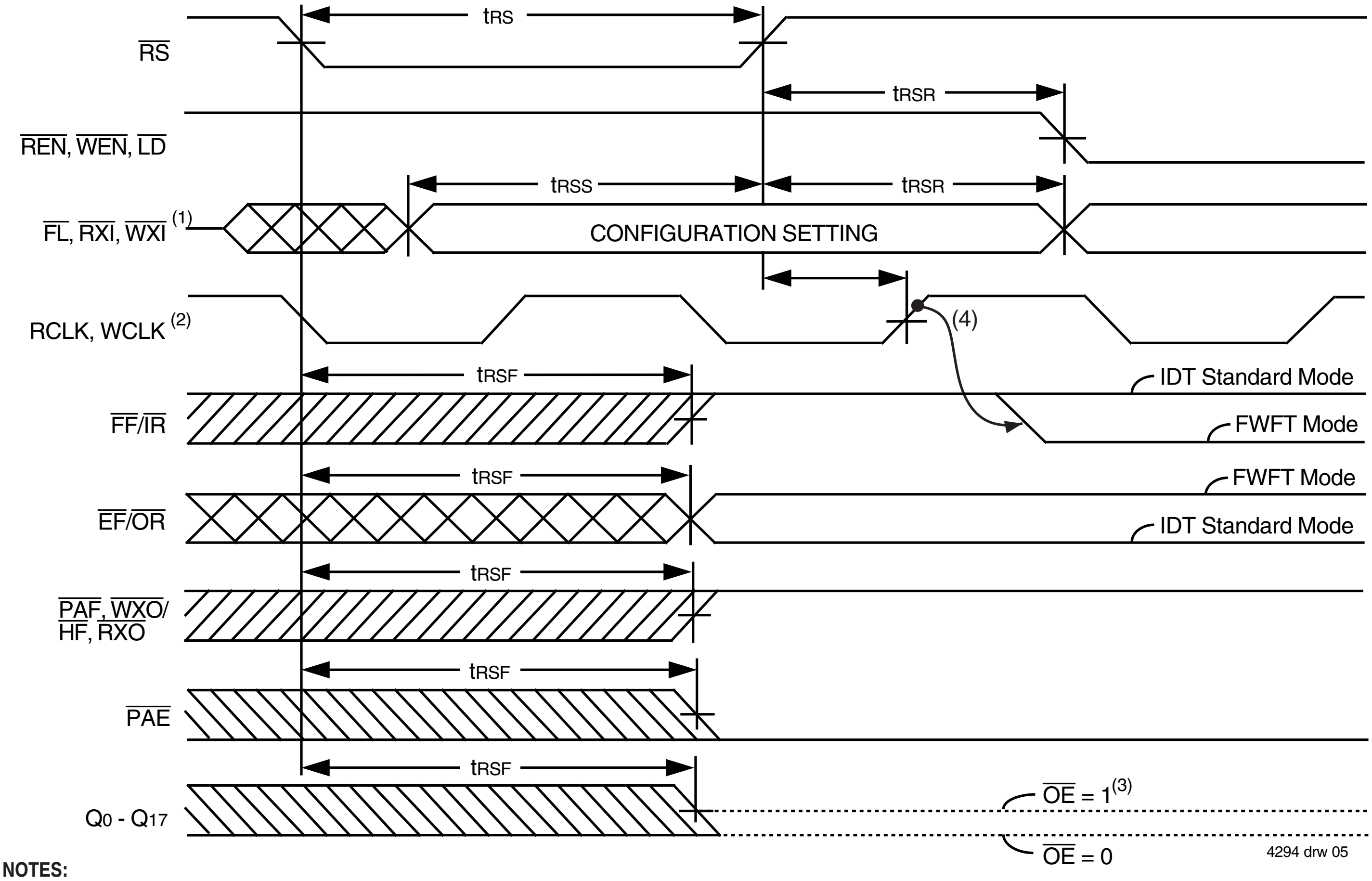
In the Daisy Chain Depth Expansion mode, $\overline{WXI}$ is connected to $\overline{WXO}$ of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device writes to the last location of memory.

READ EXPANSION OUT ($\overline{RXO}$)

In the Daisy Chain Depth Expansion configuration, Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

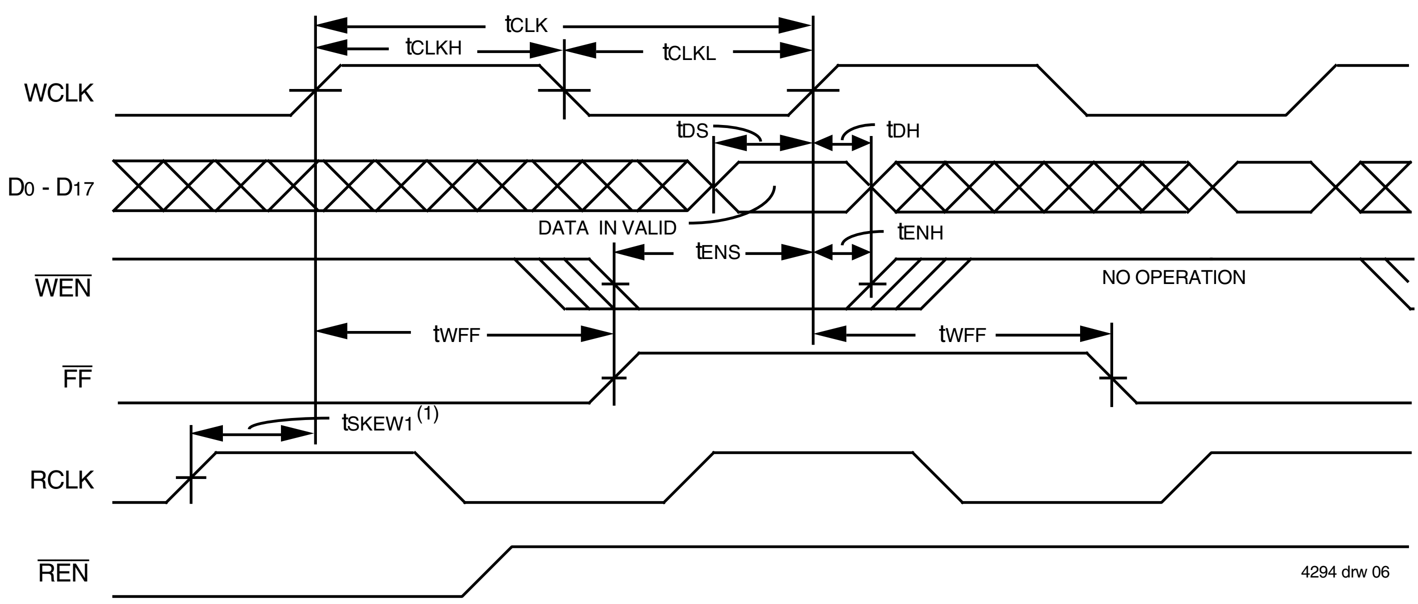
DATA OUTPUTS (Q0-Q17)

Q_0-Q_{17} are data outputs for 18-bit wide data.



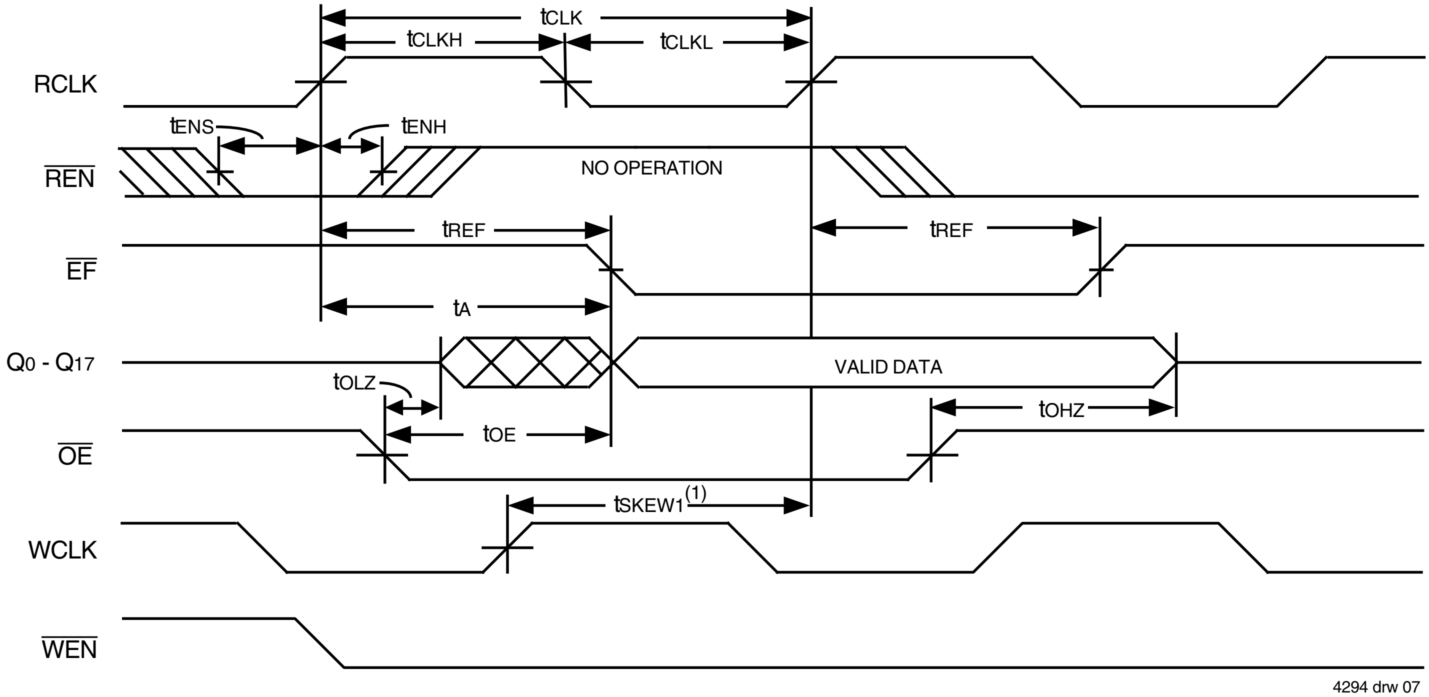
NOTES:
1. Single device mode (FL, RXI, WXI) = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0). FL, RXI, WXI should be static (tied to VCC or GND).
2. The clocks (RCLK, WCLK) can be free-running asynchronously or coincidentally.
3. After reset, the outputs will be LOW if OE = 0 and tri-state if OE = 1.
4. In FWFT mode IR goes LOW based on the WCLK edge after Reset.

Figure 5. Reset Timing[2]



NOTES:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that FF will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then FF may not change state until the next WCLK edge.
2. Select this mode by setting (FL, RXI, WXI) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during Reset.

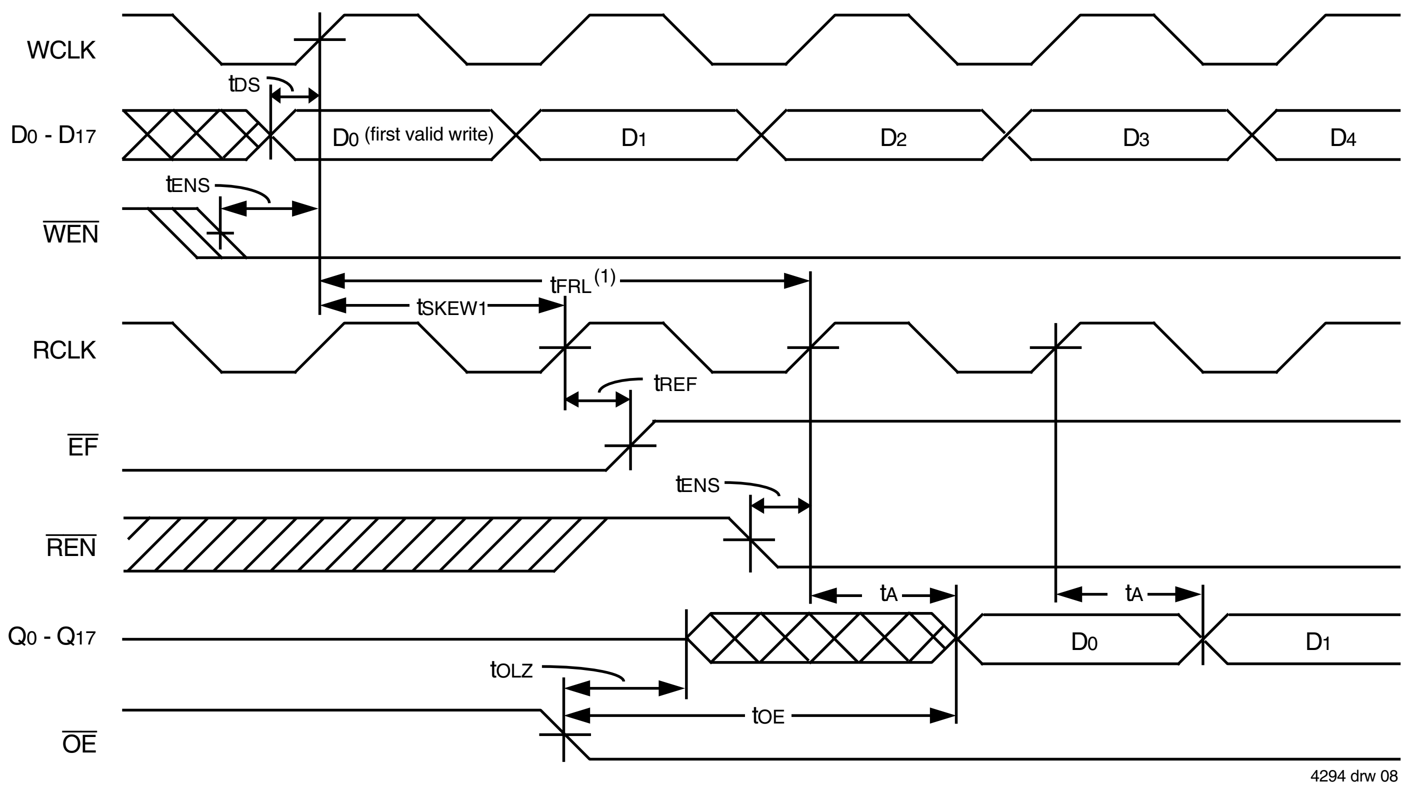
Figure 6. Write Cycle Timing with Single Register-Buffered FF (IDT Standard Mode)



NOTES:

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that EF will go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW1, then EF may not change state until the next RCLK edge.
2. Select this mode by setting (FL, RXI, WXI) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during Reset.

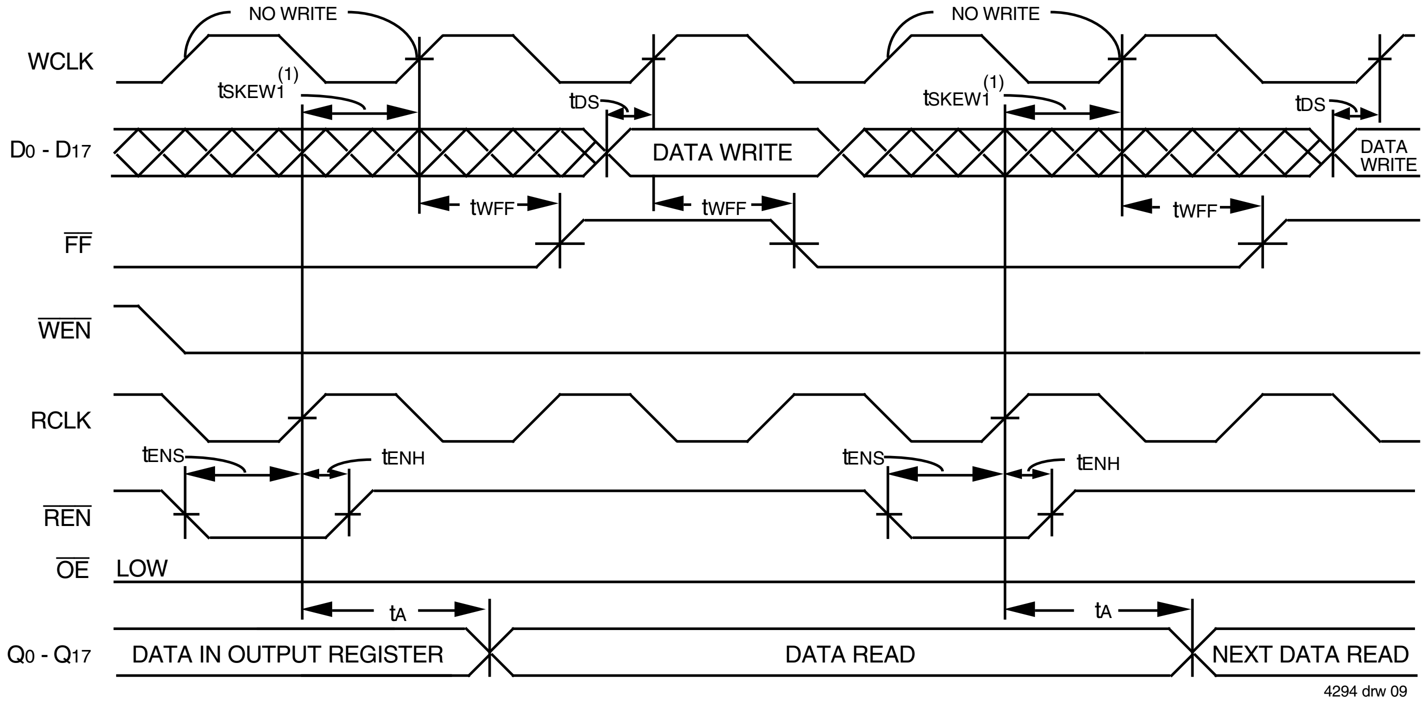
Figure 7. Read Cycle Timing with Single Register-Buffered EF (IDT Standard Mode)



NOTES:

1. When tSKEW1 minimum specification, tFRL (maximum) = tCLK + tSKEW1. When tSKEW1 < minimum specification, tFRL (maximum) = either 2*tCLK + tSKEW1 or tCLK + tSKEW1. The Latency Timing applies only at the Empty Boundary (EF = LOW).
2. The first word is available the cycle after EF goes HIGH, always.
3. Select this mode by setting (FL, RXI, WXI) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during Reset.

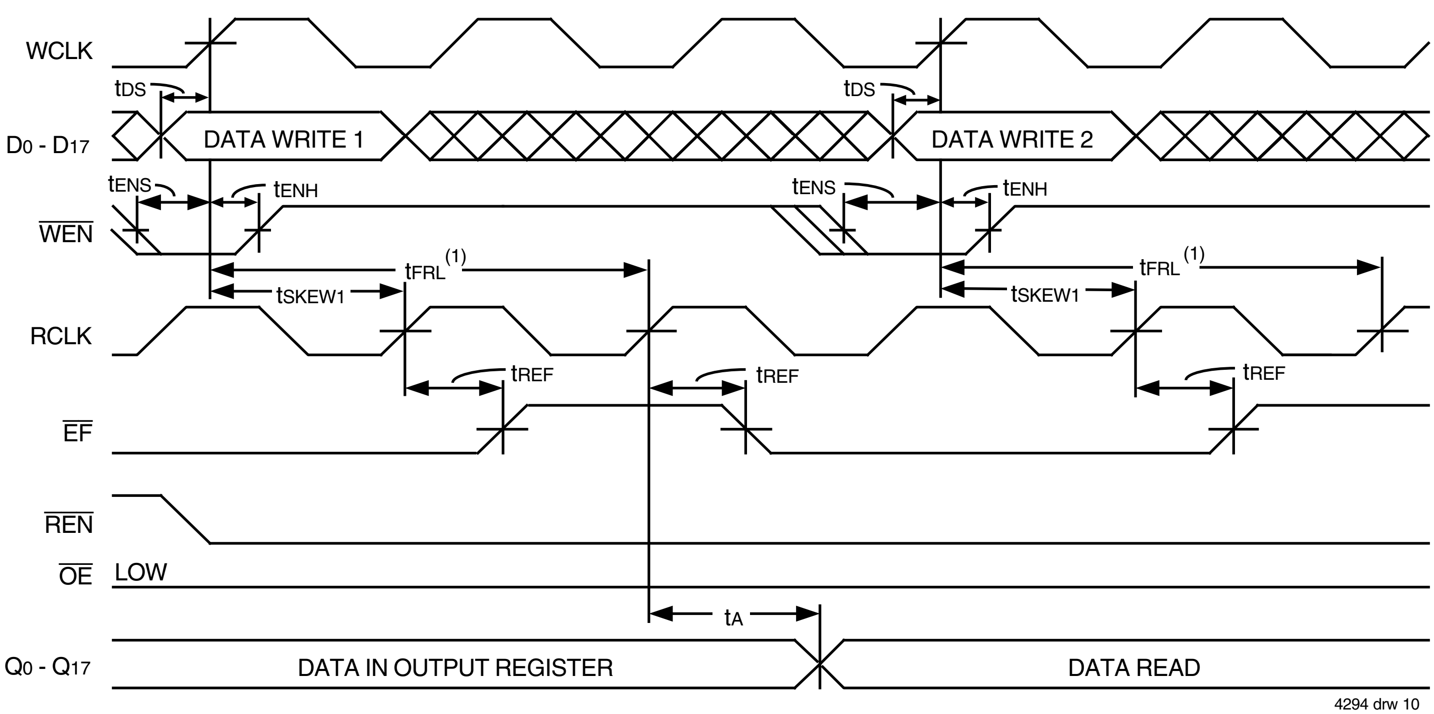
Figure 8. First Data Word Latency with Single Register-Buffered EF (IDT Standard Mode)



NOTES:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{\text{FF}}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{\text{FF}}$ may not change state until the next WCLK edge.
2. Select this mode by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during Reset.

Figure 9. Single Register-Buffered Full Flag Timing (IDT Standard Mode)



NOTES:

1. When t_{SKEW1} minimum specification, t_{FRL} (maximum) = t_{CLK} + t_{SKEW1}. When t_{SKEW1} < minimum specification, t_{FRL} (maximum) = either 2 * t_{CLK} + t_{SKEW1}, or t_{CLK} + t_{SKEW1}. The Latency Timing apply only at the Empty Boundary ($\overline{\text{EF}}$ = LOW).
2. Select this mode by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (0,0,0), (0,1,1), (1,0,0) or (1,1,1) during Reset.

Figure 10. Single Register-Buffered Empty Flag Timing (IDT Standard Mode)

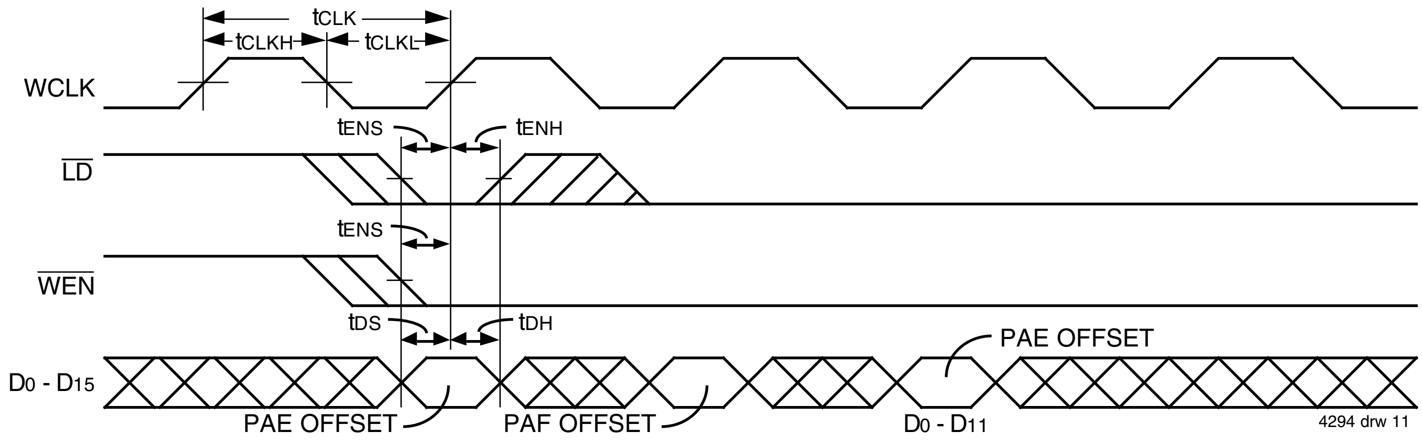


Figure 11. Write Programmable Registers (IDT Standard and FWFT Modes)

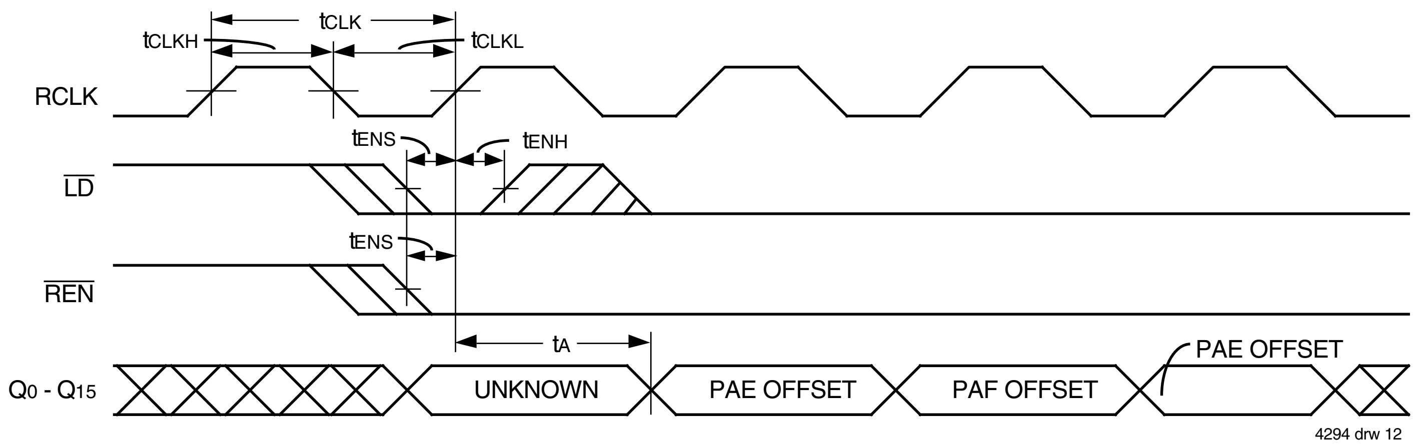
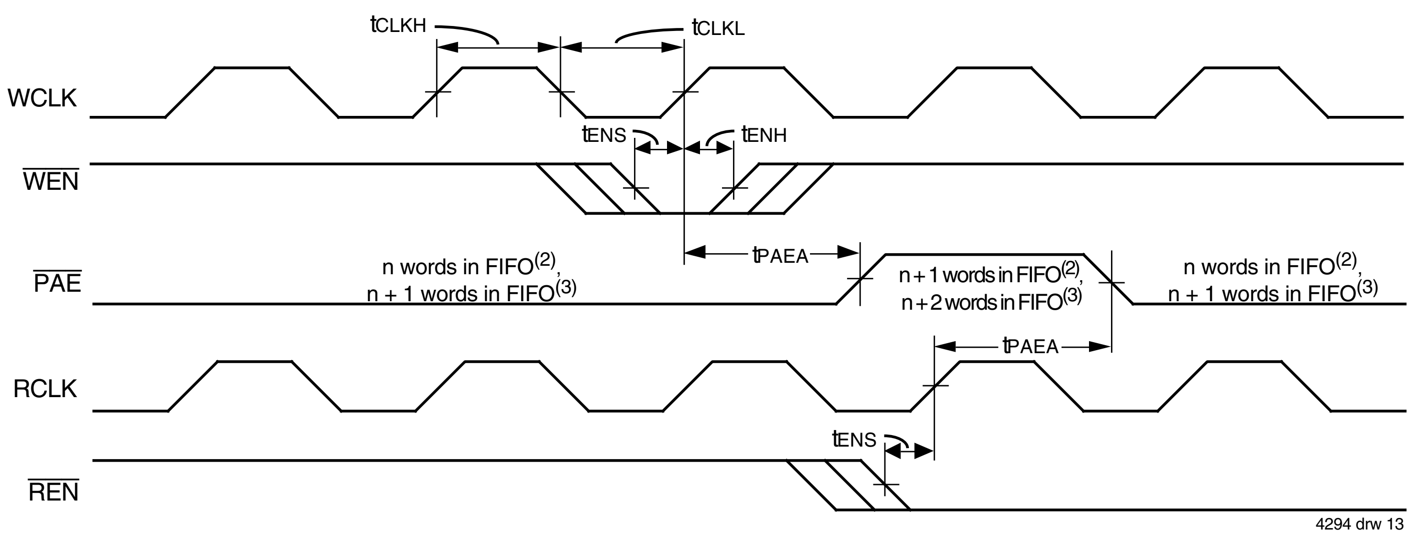
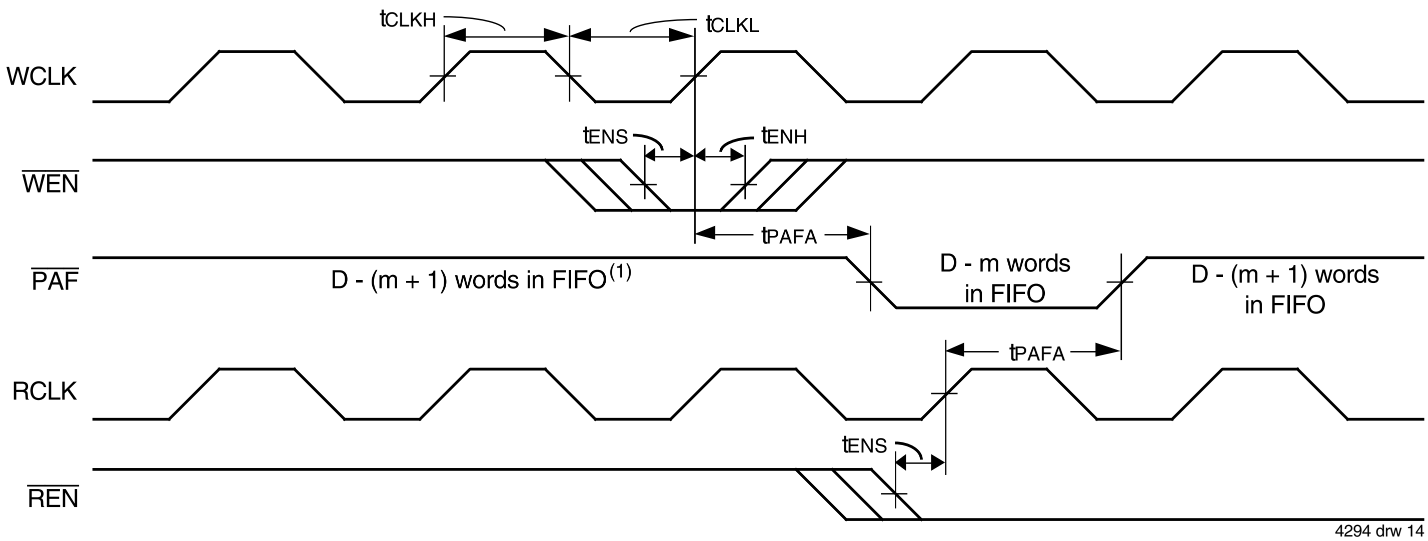


Figure 12. Read Programmable Registers (IDT Standard Mode)



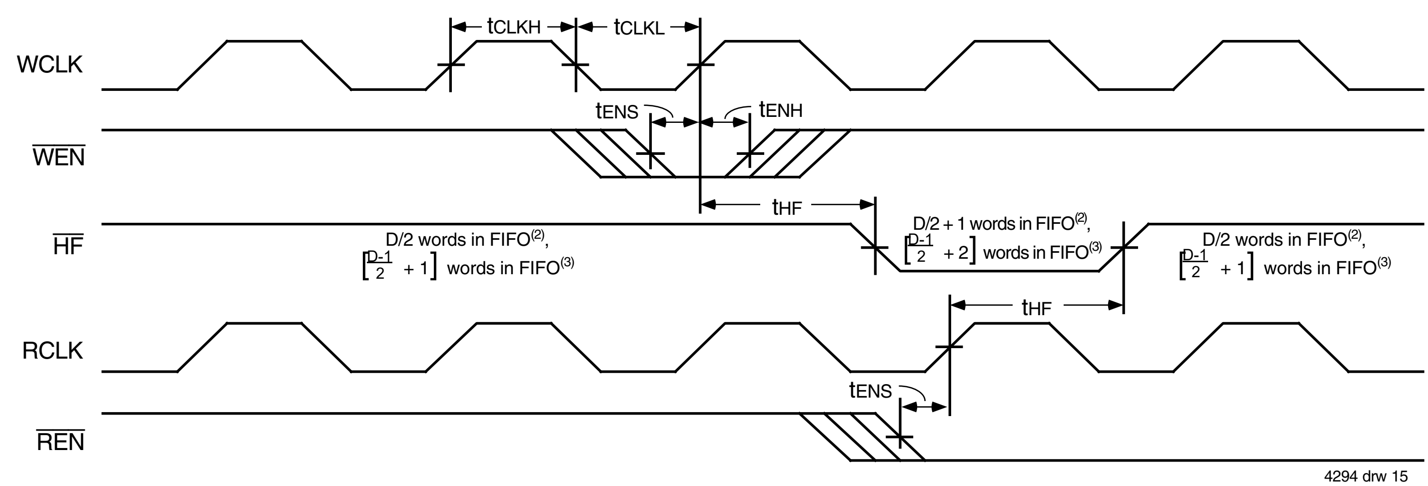
NOTES:
1. n = PAE offset.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. PAE is asserted LOW on RCLK transition and reset to HIGH on WCLK transition.
5. Select this mode by setting (FL, RXI, WXI) = (0,0,0), (0,0,1), (0,1,0), (0,1,1) or (1,1,1) during Reset.

Figure 13. Asynchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)



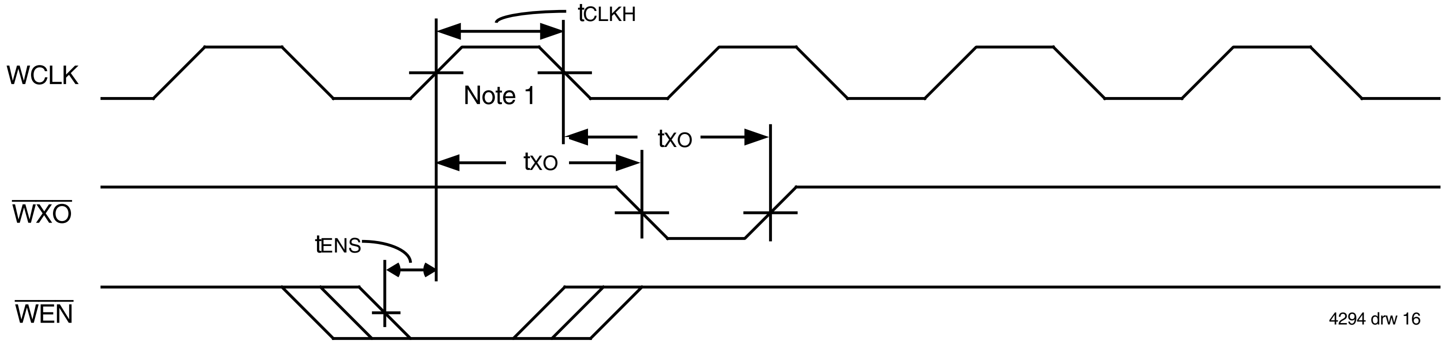
NOTES:
1. m = $\overline{\text{PAF}}$ offset.
2. D = maximum FIFO Depth.
   In IDT Standard Mode: D = 256 for the IDT72V205, 512 for the IDT72V215, 1,024 for the IDT72V225, 2,048 for the IDT72V235 and 4,096 for the IDT72V245.
   In FWFT Mode: D = 257 for the IDT72V205, 513 for the IDT72V215, 1,025 for the IDT72V225, 2,049 for the IDT72V235 and 4,097 for the IDT72V245.
3. $\overline{\text{PAF}}$ is asserted to LOW on WCLK transition and reset to HIGH on RCLK transition.
4. Select this mode by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (0,0,0), (0,0,1), (0,1,0), (0,1,1) or (1,1,1) during Reset.

Figure 14. Asynchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)



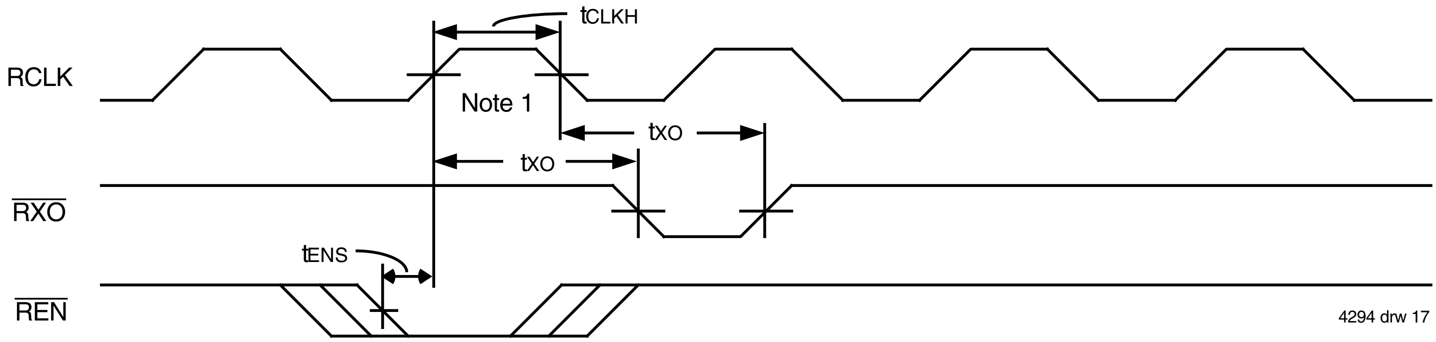
NOTES:
1. D = maximum FIFO Depth.
   In IDT Standard Mode: D = 256 for the IDT72V205, 512 for the IDT72V215, 1,024 for the IDT72V225, 2,048 for the IDT72V235 and 4,096 for the IDT72V245.
   In FWFT Mode: D = 257 for the IDT72V205, 513 for the IDT72V215, 1,025 for the IDT72V225, 2,049 for the IDT72V235 and 4,097 for the IDT72V245.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. Select this mode by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0) during Reset.

Figure 15. Half-Full Flag Timing (IDT Standard and FWFT Modes)



NOTE:
1. Write to Last Physical Location.

Figure 16. Write Expansion Out Timing



NOTE:
1. Read from Last Physical Location.

Figure 17. Read Expansion Out Timing

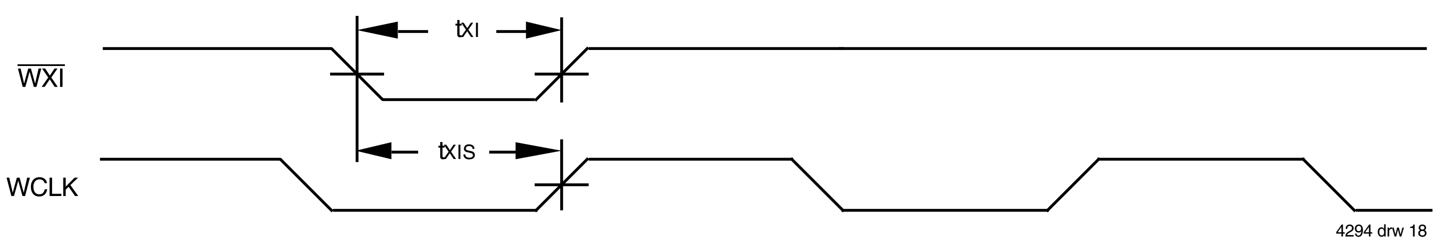


Figure 18. Write Expansion In Timing

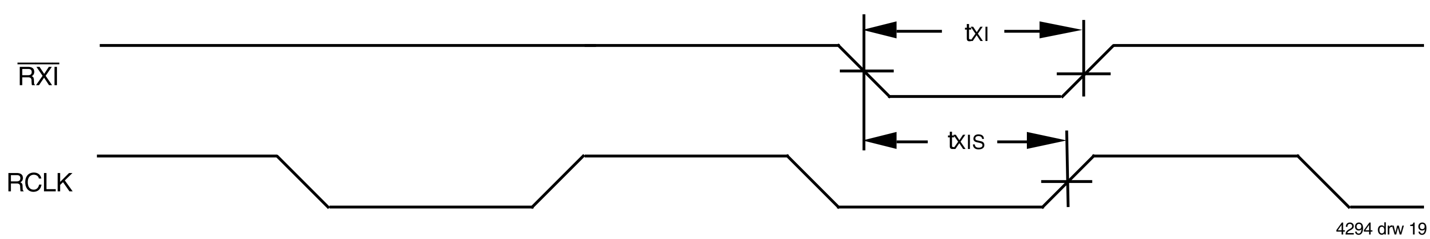
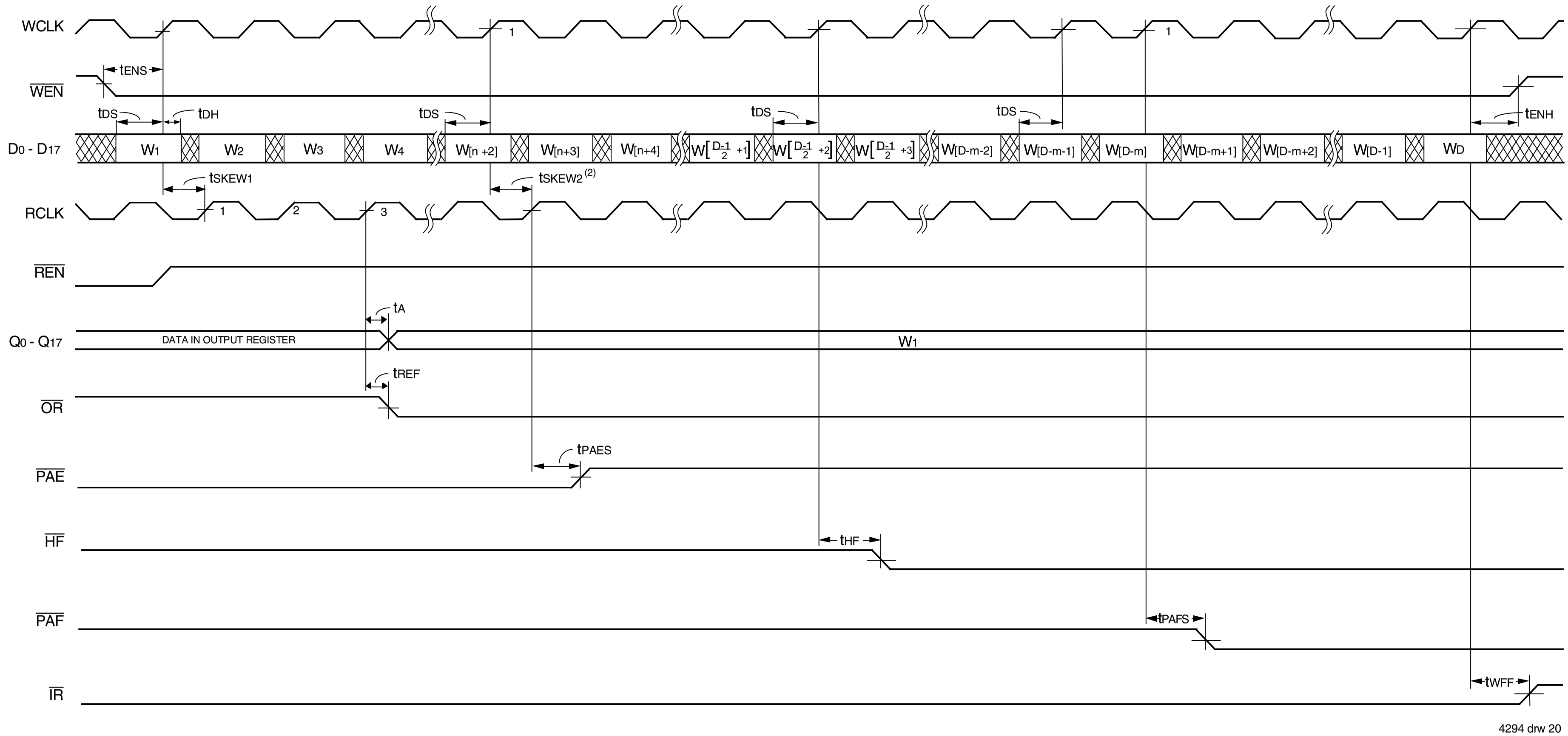


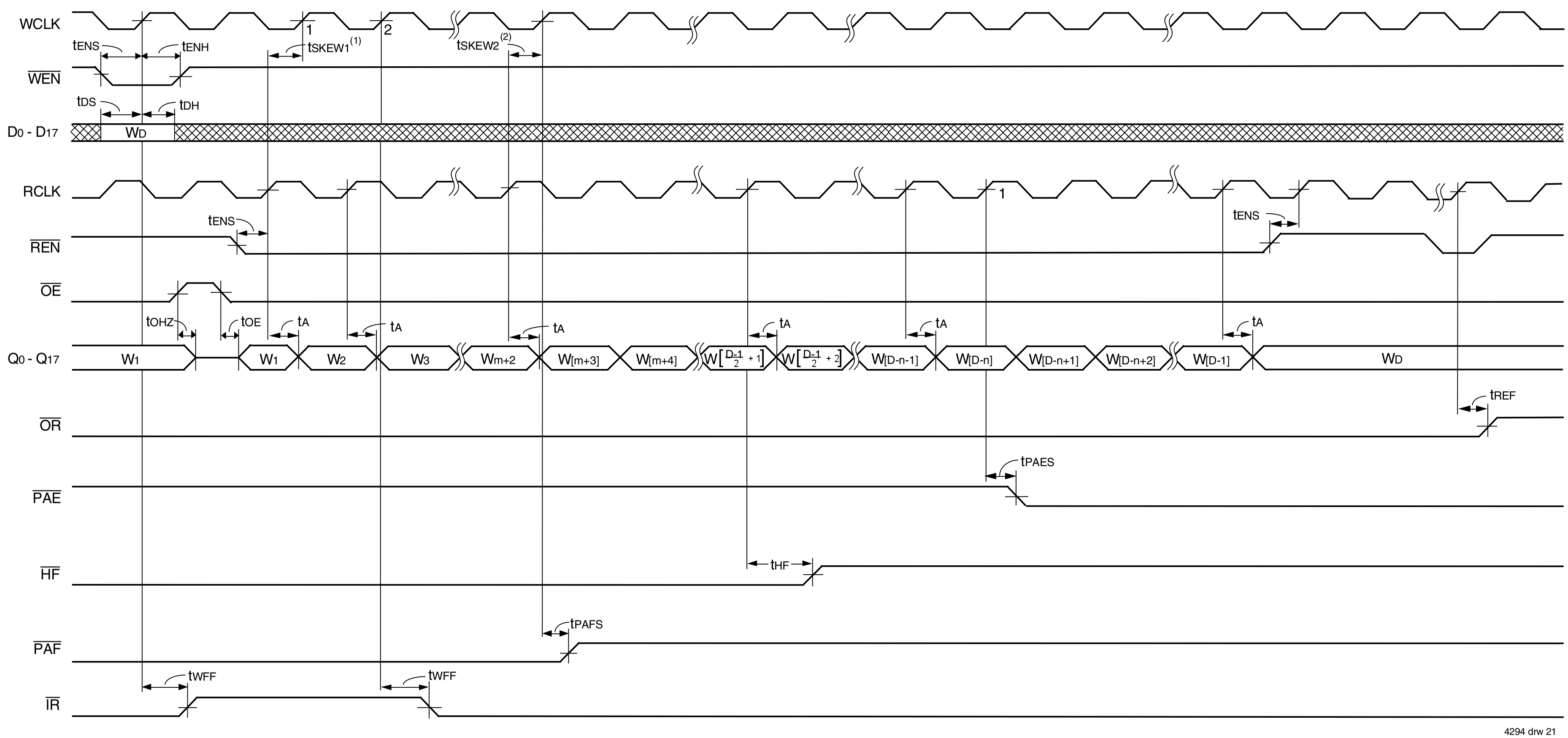
Figure 19. Read Expansion In Timing



NOTES:

1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{OR}$ to go LOW after two RCLK cycles plus tREF. If the time between the rising edge of WLCK and the rising edge of RCLK is less than tSKEW1, then the $\overline{OR}$ deassertion may be delayed one extra RCLK cycle.
2. tSKEW2 is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW2, then the $\overline{PAE}$ deassertion may be delayed one extra RCLK cycle.
3. $\overline{LD}$ = HIGH, $\overline{OE}$ = LOW
4. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth = 257 words for the IDT72V205, 513 words for the IDT72V215, 1,025 words for the IDT72V225, 2,049 words for the IDT72V235 and 4,097 words for the IDT72V245.
5. Select this mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (1,0,1) during Reset.

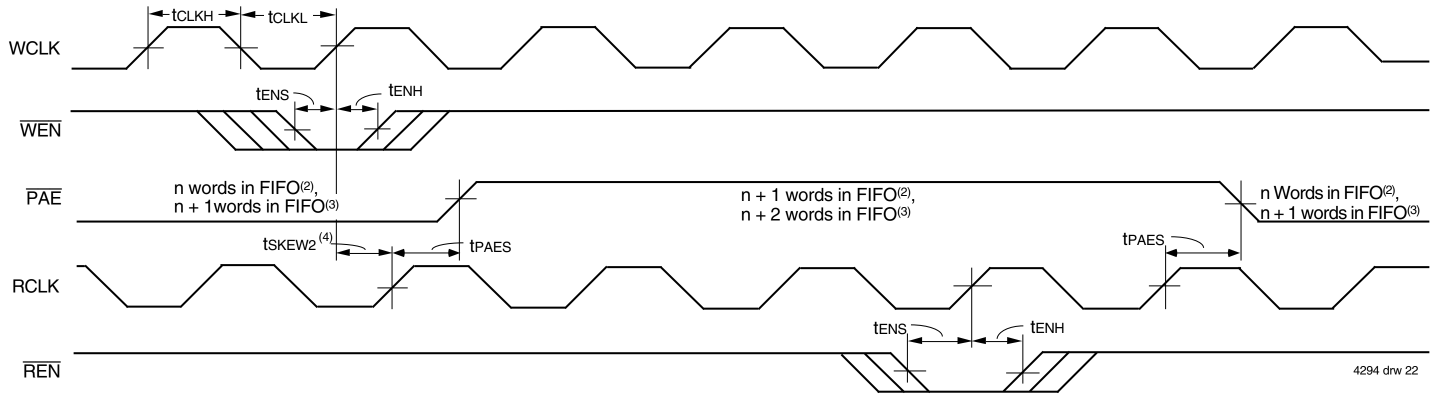
Figure 20. Write Timing with Synchronous Programmable Flags (FWFT Mode)



NOTES:

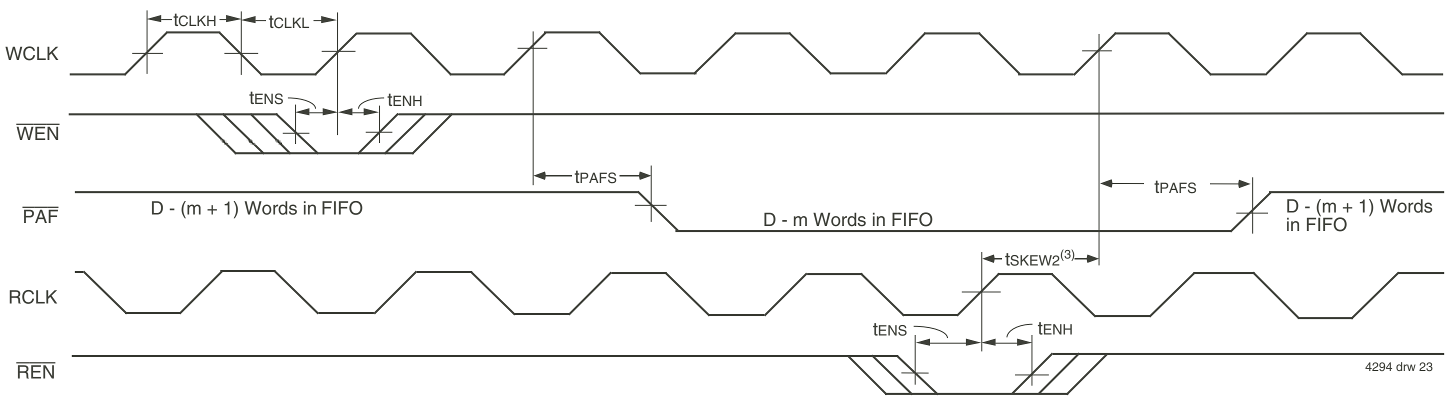
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{IR}$ will go LOW after one WCLK plus tWFF. If the time between the rising edge of RLCK and the rising edge of WCLK is less than tSKEW1, then the $\overline{IR}$ assertion may be delayed an extra WCLK cycle.
2. tSKEW2 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW2, then the $\overline{PAF}$ deassertion time may be delayed an extra WCLK cycle.
3. $\overline{LD}$ = HIGH
4. n = $\overline{PAE}$ offset, m = $\overline{PAF}$ offset, D = maximum FIFO depth = 257 words for the IDT72V205, 513 words for the IDT72V215, 1,025 words for the IDT72V225, 2,049 words for IDT72V235 and 4,097 words for IDT72V245.
5. Select this mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (1,0,1) during Reset.

Figure 21. Read Timing with Synchronous Programmable Flags (FWFT Mode)



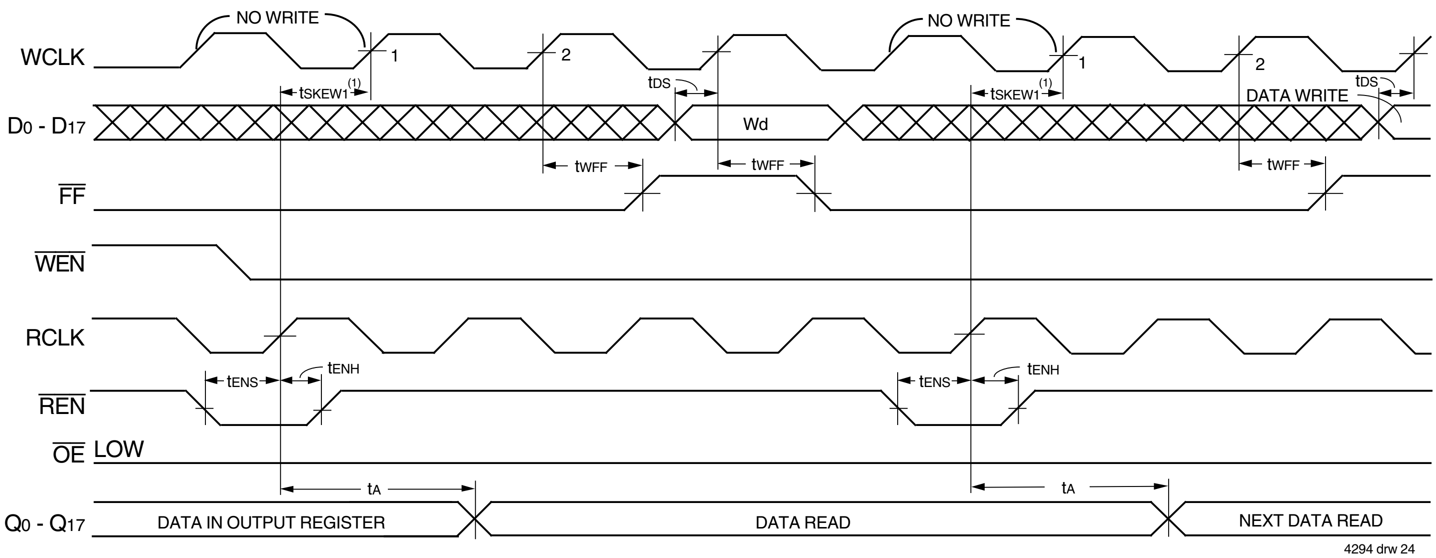
NOTES:
1. n = $\overline{\text{PAE}}$ offset.
2. For IDT Standard Mode.
3. For FWFT Mode.
4. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{\text{PAE}}$ to go HIGH during the current clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then the $\overline{\text{PAE}}$ deassertion may be delayed one extra RCLK cycle.
5. $\overline{\text{PAE}}$ is asserted and updated on the rising edge of RCLK only.
6. Select this mode by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (1,0,0), (1,0,1), or (1,1,0) during Reset.

Figure 22. Synchronous Programmable Almost-Empty Flag Timing (IDT Standard and FWFT Modes)



NOTES:
1. m = $\overline{\text{PAF}}$ offset.
2. D = maximum FIFO Depth.
   In IDT Standard Mode: D = 256 for the IDT72V205, 512 for the IDT72V215, 1,024 for the IDT72V225, 2,048 for the IDT72V235 and 4,096 for the IDT72V245.
   In FWFT Mode: D = 257 for the IDT72V205, 513 for the IDT72V215, 1,025 for the IDT72V225, 2,049 for the IDT72V235 and 4,097 for the IDT72V245.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{\text{PAF}}$ to go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then the $\overline{\text{PAF}}$ deassertion time may be delayed an extra WCLK cycle.
4. $\overline{\text{PAF}}$ is asserted and updated on the rising edge of WCLK only.
5. Select this mode by setting ($\overline{\text{FL}}$, $\overline{\text{RXI}}$, $\overline{\text{WXI}}$) = (1,0,0), (1,0,1), or (1,1,0) during Reset.

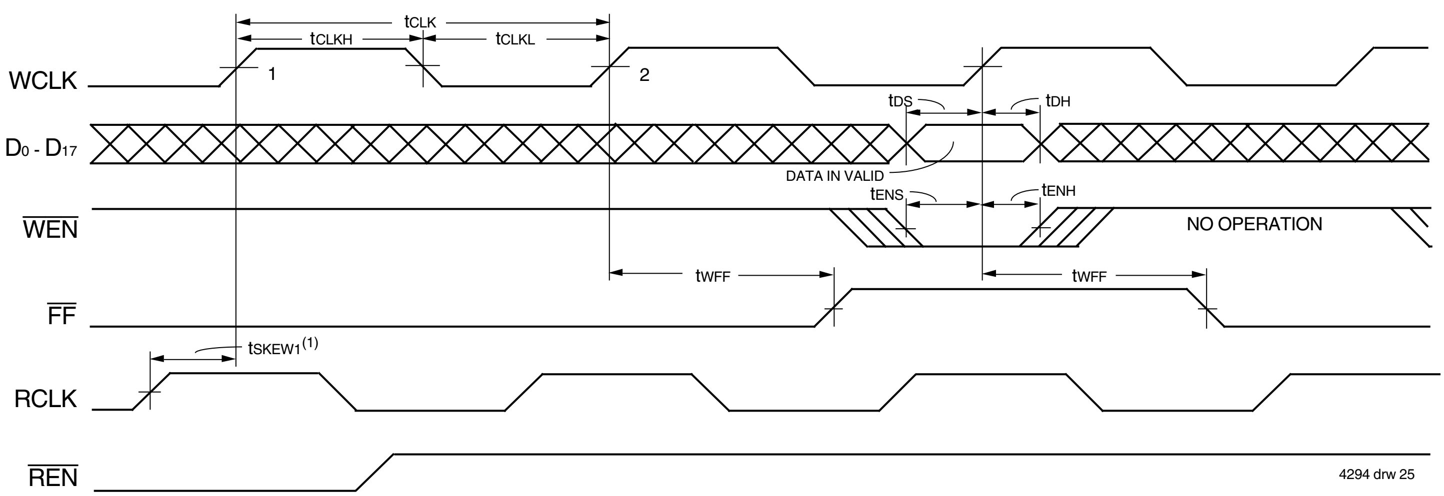
Figure 23. Synchronous Programmable Almost-Full Flag Timing (IDT Standard and FWFT Modes)



NOTES:

1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH after one WCLK cycle plus tWFF. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then the $\overline{FF}$ deassertion time may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH.
3. Select this mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,1,0) or (1,1,0) during Reset.

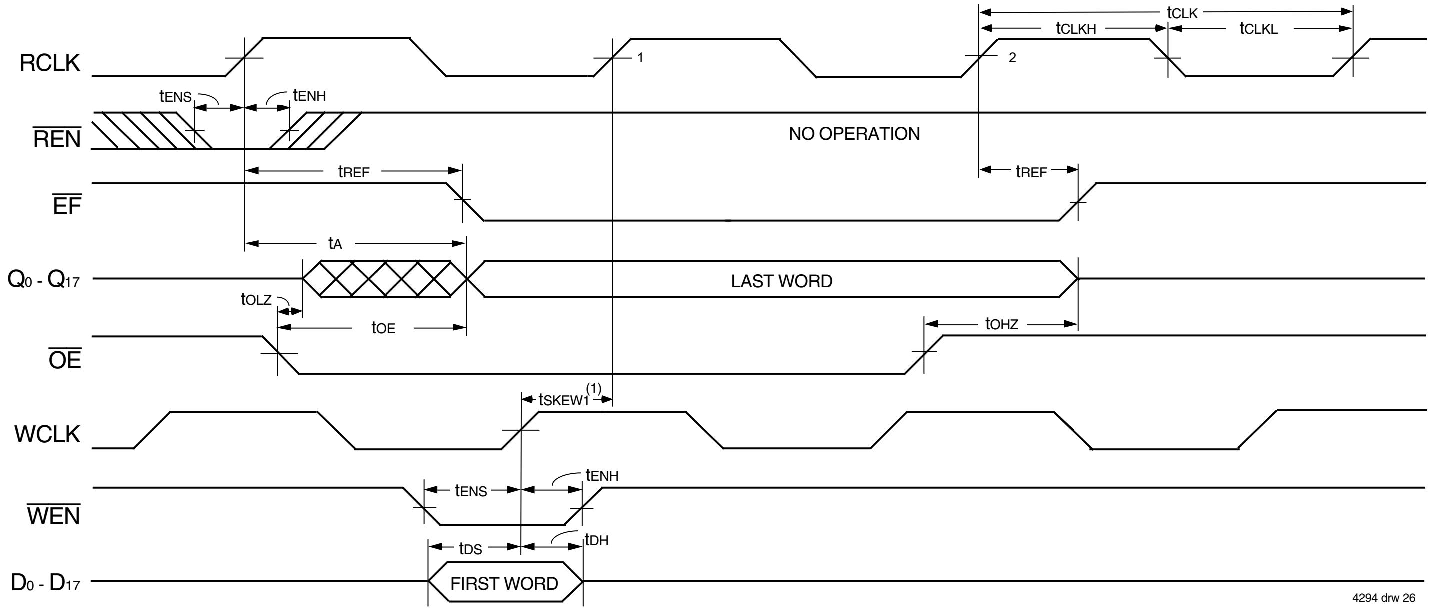
Figure 24. Double Register-Buffered Full Flag Timing (IDT Standard Mode)



NOTES:

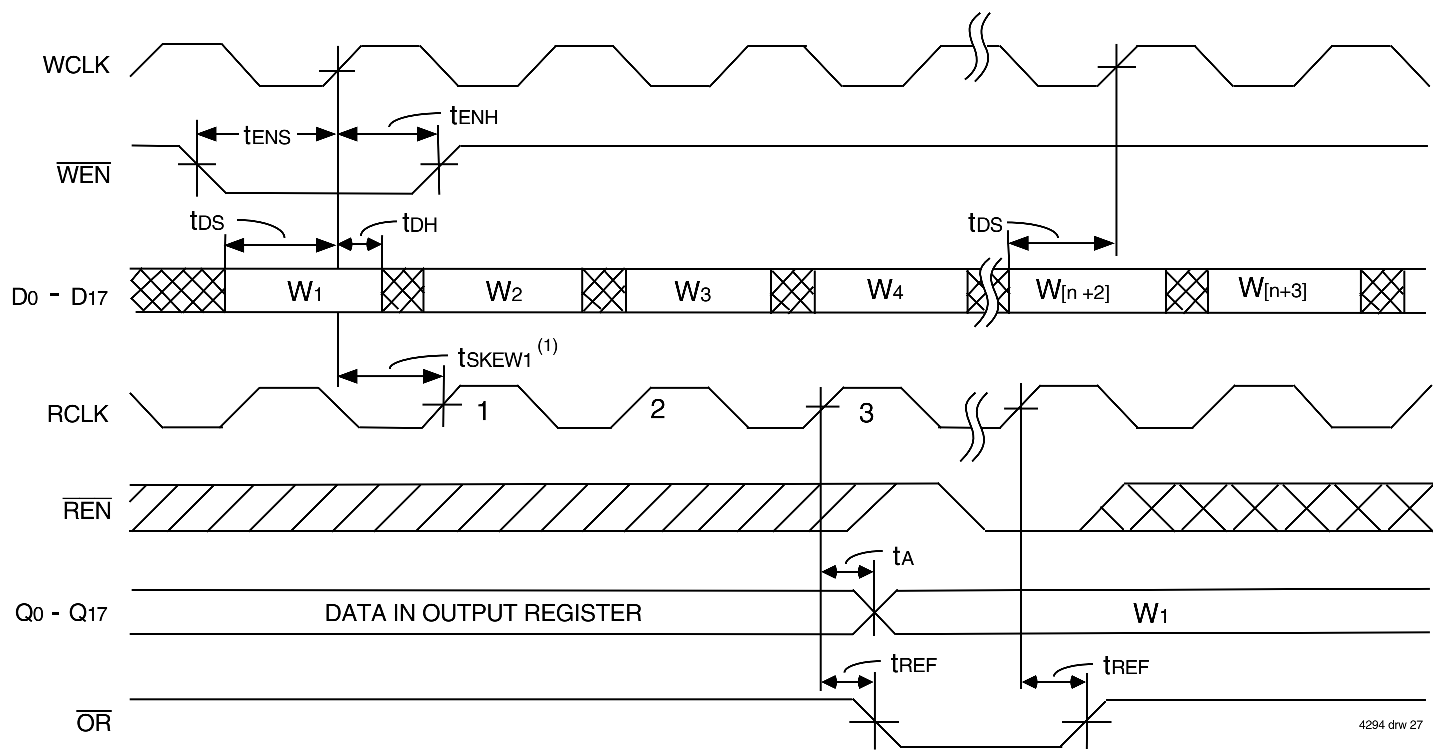
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH after one WCLK cycle plus tRFF. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1. then the $\overline{FF}$ deassertion may be delayed an extra WCLK cycle.
2. $\overline{LD}$ = HIGH.
3. Select this mode by setting ($\overline{FL}$, $\overline{RXI}$, $\overline{WXI}$) = (0,1,0) or (1,1,0) during Reset.

Figure 25. Write Cycle Timing with Double Register-Buffered $\overline{FF}$ (IDT Standard Mode)



NOTES:
1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that EF will go HIGH after one RCLK cycle plus tREF. If the time between the rising edge of WCLK and the rising edge of RCLK is less than tSKEW1. then the EF deassertion may be delayed an extra RCLK cycle.
2. LD = HIGH
3. Select this mode by setting (FL, RXI, WXI) = (0,1,0) or (1,1,0) during Reset.

Figure 26. Read Cycle Timing with Double Register-Buffered EF (IDT Standard Timing)



NOTES:
1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge for OR to go HIGH during the current cycle. If the time between the rising edge of WLCK and the rising edge of RCLK is less than tSKEW1, then the OR deassertion may be delayed one extra RCLK cycle.
2. LD = HIGH, OE = LOW
3. Select this mode by setting (FL, RXI, WXI) = (0,0,1) or (1,0,1) during Reset.

Figure 27. OR Flag Timing and First Word Fall Through when FIFO is Empty (FWFT mode)

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72V205/72V215/72V225/72V235/72V245 may be used when the application requirements are for 256/512/1,024/2,048/4,096 words or less. These FIFOs are in a single Device Configuration when the First Load (FL), Write Expansion In (WXI) and Read Expansion In (RXI) control inputs are configured as (FL, RXI, WXI = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0) during reset (Figure 28).

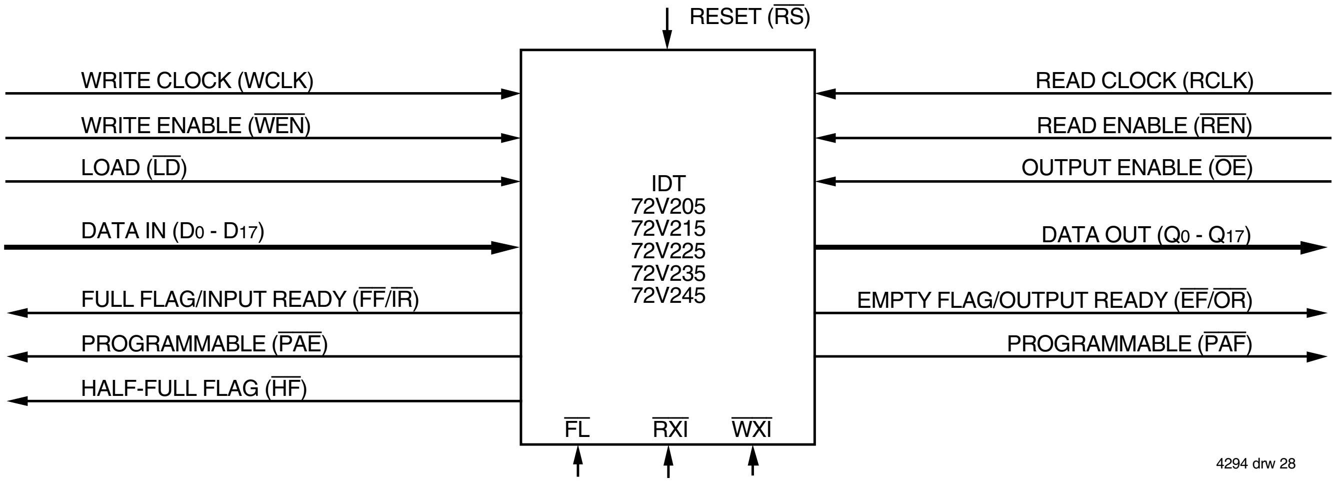
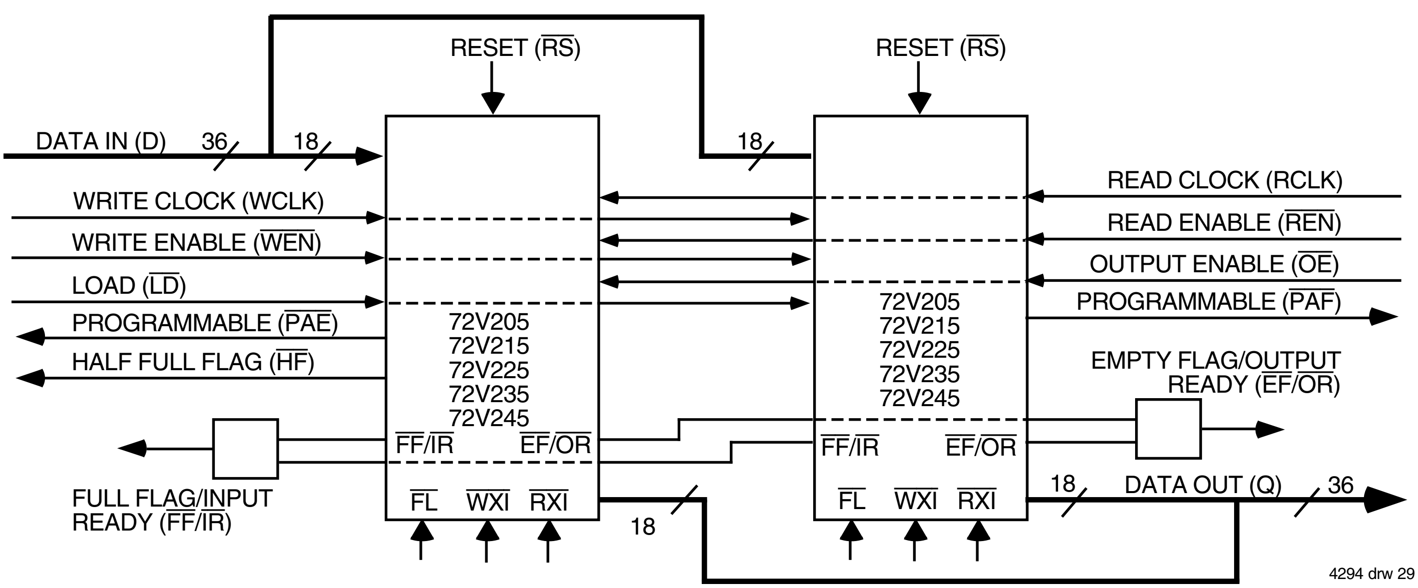


Figure 28. Block Diagram of Single 256 x 18, 512 x 18, 1,024 x 18, 2,048 x 18, 4,096 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting together the control signals of multiple devices. Status flags can be detected from any one device. The exceptions are the Empty Flag/Output Ready and Full Flag/Input Ready. Because of variations in skew between RCLK and WCLK, it is possible for flag assertion and deassertion to vary by one cycle between FIFOs. To avoid problems the user must create composite flags by gating the Empty Flags/Output Ready of every FIFO, and separately gating all Full Flags/Input Ready. Figure 29 demonstrates a 36-word width by using two IDT72V205/72V215/72V225/72V235/72V245s. Any word width can be attained by adding additional IDT72V205/72V215/72V225/72V235/72V245s. These FIFOs are in a single Device Configuration when the First Load (FL), Write Expansion In (WXI) and Read Expansion In (RXI) control inputs are configured as (FL, RXI, WXI = (0,0,0), (0,0,1), (0,1,0), (1,0,0), (1,0,1) or (1,1,0) during reset (Figure 29). Please see the Application Note AN-83.



NOTE:
1. Do not connect any output control signals directly together.

Figure 29. Block Diagram of 256 x 36, 512 x 36, 1,024 x 36, 2,048 x 36, 4,096 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

DEPTH EXPANSION CONFIGURATION — DAISY CHAIN TECHNIQUE (WITH PROGRAMMABLE FLAGS)

These devices can easily be adapted to applications requiring more than 256/512/1,024/2,048/4,096 words of buffering. Figure 30 shows Depth Expansion using three IDT72V205/72V215/72V225/72V235/72V245s. Maximum depth is limited only by signal loading.

Follow these steps:

1. The first device must be designated by grounding the First Load ($\overline{\text{FL}}$) control input.
2. All other devices must have $\overline{\text{FL}}$ in the HIGH state.
3. The Write Expansion Out ($\overline{\text{WXO}}$) pin of each device must be tied to the Write Expansion In ($\overline{\text{WXI}}$) pin of the next device. See Figure 30.
4. The Read Expansion Out ($\overline{\text{RXO}}$) pin of each device must be tied to the Read Expansion In ($\overline{\text{RXI}}$) pin of the next device. See Figure 30.
5. All Load ($\overline{\text{LD}}$) pins are tied together.
6. The Half-Full Flag ($\overline{\text{HF}}$) is not available in this Depth Expansion Configuration.
7. $\overline{\text{EF}}$, $\overline{\text{FF}}$, $\overline{\text{PAE}}$, and $\overline{\text{PAF}}$ are created with composite flags by ORing together every respective flags for monitoring. The composite $\overline{\text{PAE}}$ and $\overline{\text{PAF}}$ flags are not precise.
8. In Daisy Chain mode, the flag outputs are single register-buffered and the partial flags are in asynchronous timing mode.

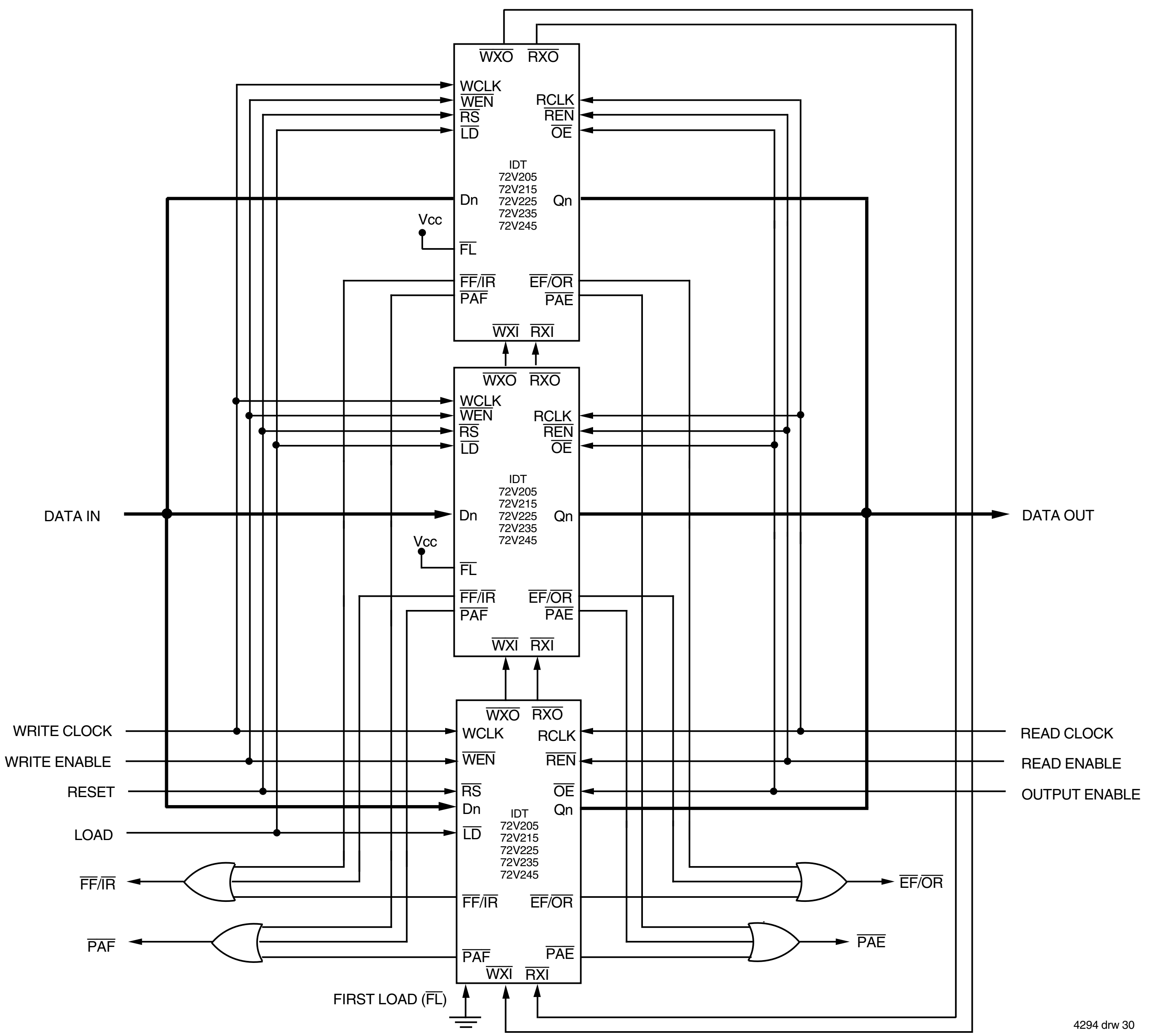


Figure 30. Block Diagram of 768 x 18, 1,536 x 18, 3,072 x 18, 6,144 x 18, 12,288 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

DEPTH EXPANSION CONFIGURATION (FWFT MODE)

In FWFT mode, the FIFOs can be connected in series (the data outputs of one FIFO connected to the data inputs of the next) with no external logic necessary. The resulting configuration provides a total depth equivalent to the sum of the depths associated with each single FIFO. Figure 31 shows a depth expansion using two IDT72V205/72V215/72V225/72V235/72V245 devices.

Care should be taken to select FWFT mode during Master Reset for all FIFOs in the depth expansion configuration. The first word written to an empty configuration will pass from one FIFO to the next ("ripple down") until it finally appears at the outputs of the last FIFO in the chain–no read operation is necessary but the RCLK of each FIFO must be free-running. Each time the data word appears at the outputs of one FIFO, that device's $\overline{OR}$ line goes LOW, enabling a write to the next FIFO in line.

For an empty expansion configuration, the amount of time it takes for $\overline{OR}$ of the last FIFO in the chain to go LOW (i.e. valid data to appear on the last FIFO's outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO:

$$(N - 1)*(4*\text{transfer clock}) + 3*T_{RCLK}$$

where N is the number of FIFOs in the expansion and T_{RCLK} is the RCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between WCLK and transfer clock, or RCLK and transfer clock, for the $\overline{OR}$ flag.

The "ripple down" delay is only noticeable for the first word written to an empty depth expansion configuration. There will be no delay evident for subsequent words written to the configuration.

The first free location created by reading from a full depth expansion configuration will "bubble up" from the last FIFO to the previous one until it finally moves into the first FIFO of the chain. Each time a free location is created in one FIFO of the chain, that FIFO's $\overline{IR}$ line goes LOW, enabling the preceding FIFO to write a word to fill it.

For a full expansion configuration, the amount of time it takes for $\overline{IR}$ of the first FIFO in the chain to go LOW after a word has been read from the last FIFO is the sum of the delays for each individual FIFO:

$$(N - 1)*(3*\text{transfer clock}) + 2\,T_{WCLK}$$

where N is the number of FIFOs in the expansion and T_{WCLK} is the WCLK period. Note that extra cycles should be added for the possibility that the t_{SKEW1} specification is not met between RCLK and transfer clock, or WCLK and transfer clock, for the $\overline{IR}$ flag.

The Transfer Clock line should be tied to either WCLK or RCLK, whichever is faster. Both these actions result in data moving, as quickly as possible, to the end of the chain and free locations to the beginning of the chain.

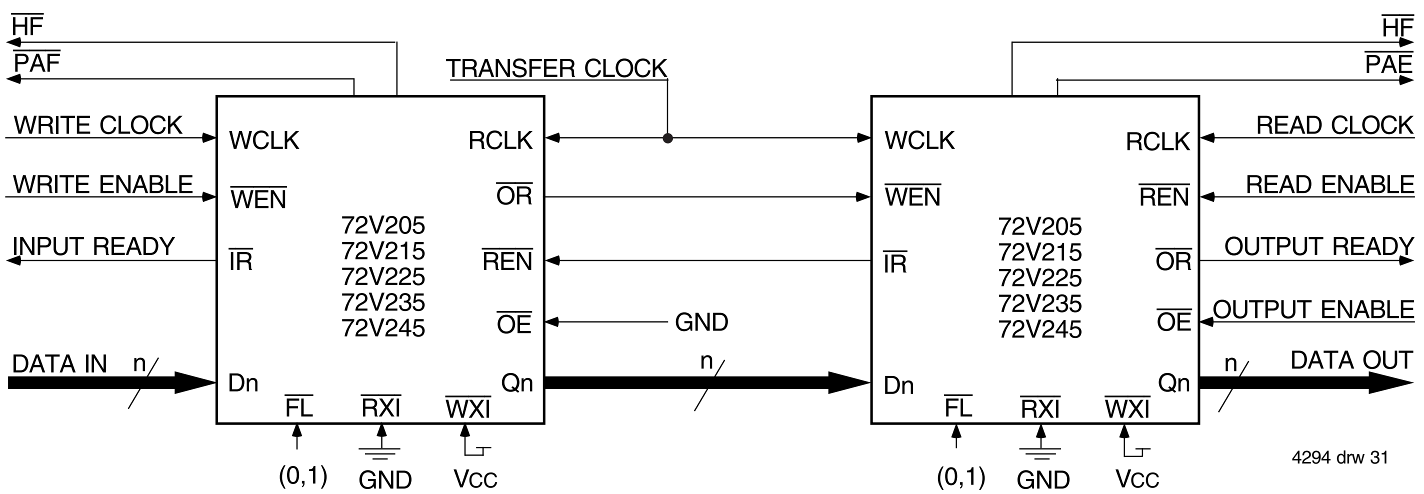
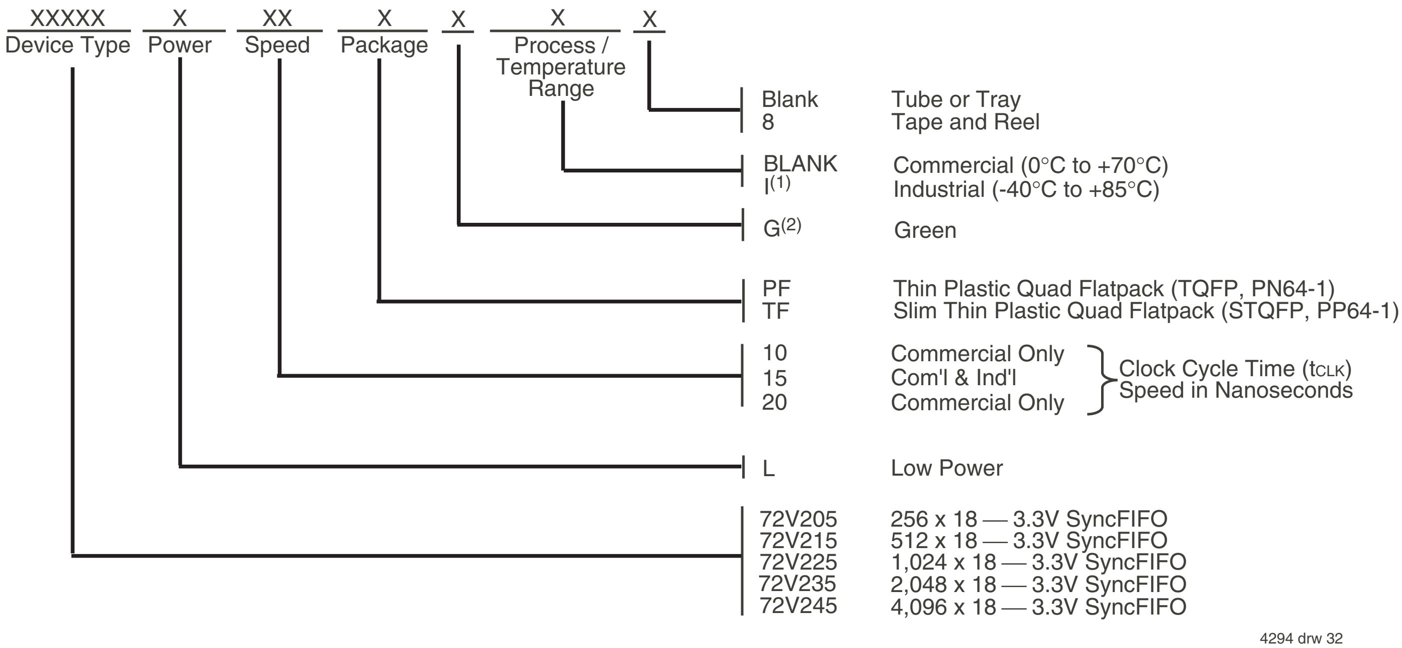


Figure 31. Block Diagram of 512 x 18, 1,024 x 18, 2,048 x 18, 4,096 x 18, 8,192 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



NOTES:
1. Industrial temperature range product for the 15ns speed grade is available as a standard device. All other speed grades are available by special order.
2. Green parts are available. For specific speeds and packages contact your sales office.
LEAD FINISH (SNPB) PARTS ARE IN EOL PROCESS. PRODUCT DISCONTINUATION NOTICE - PDN# SP-17-02

DATASHEET DOCUMENT HISTORY

05/02/2001	pgs. 4, 5 and 25.
01/11/2002	pg. 4.
02/01/2002	pg. 4.
02/22/2006	pgs. 1 and 25.
10/22/2008	pg. 25.
03/21/2013	pg. 2 and 25.
03/19/2018	Product Discontinuation Notice - PDN# SP-17-02 Last time buy expires June 15, 2018.

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