3.3 VOLT CMOS SyncFIFOTM WITH BUS-MATCHING

IDT72V3623
IDT72V3643

FEATURES:

• Memory storage capacity:
  IDT72V3623–256 x 36
  IDT72V3643–1,024 x 36
• Clock frequencies up to 100 MHz (6.5 ns access time)
• Clocked FIFO buffering data from Port A to Port B
• IDT Standard timing (using EF and FF) or First Word Fall Through Timing (using OR and IR flag functions)
• Programmable Almost-Empty and Almost-Full flags; each has three default offsets (8, 16 and 64)
• Serial or parallel programming of partial flags
• Port B bus sizing of 36 bits (long word), 18 bits (word) and 9 bits (byte)
• Big- or Little-Endian format for word and byte bus sizes

• Reset clears data and configures FIFO, Partial Reset clears data but retains configuration settings
• Mailbox bypass registers for each FIFO
• Free-running CLKA and CLKB may be asynchronous or coincident (simultaneous reading and writing of data on a single clock edge is permitted)
• Easily expandable in width and depth
• Auto power down minimizes power dissipation
• Available in a space-saving 128-pin Thin Quad Flatpack (TQFP)
• Pin and functionally compatible versions of the 5V operating IDT723623/723643
• Industrial temperature range (–40°C to +85°C) is available
• Green parts available, see ordering information

FUNCTIONAL BLOCK DIAGRAM
DESCRIPTION:

The IDT72V3623/72V3643 are pin and functionally compatible versions of the IDT723623/723643, designed to run off a 3.3V supply for exceptionally low power consumption. These devices are monolithic, high-speed, low-power, CMOS unidirectional Synchronous (clocked) FIFO memory which supports clock frequencies up to 100 MHz and has read access times as fast as 6.5 ns. The 256/1,024 x 36 dual-port SRAM FIFO buffers data from Port A to Port B. FIFO data on Port B can output in 36-bit, 18-bit, or 9-bit formats with a choice of Big- or Little-Endian configurations.

These devices are synchronous (clocked) FIFOs, meaning each port employs a synchronous interface. All data transfers through a port are gated synchronously with the clock.

Note:
1. NC – no internal connection

PIN CONFIGURATION

TQFP (PK128, order code: PF)
TOP VIEW

NOTE:

1. NC – no internal connection

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Communication between each port may bypass the FIFO via two mailbox registers. The mailbox registers’ width matches the selected Port B bus width. Each mailbox register has a flag (MBF1 and MBF2) to signal when new mail has been stored.

Two kinds of reset are available on these FIFOs: Reset and Partial Reset. Reset initializes the read and write pointers to the first location of the memory array and selects serial flag programming, parallel flag programming, or one of three possible default flag offset settings, 8, 16 or 64.

Partial Reset also sets the read and write pointers to the first location of the memory. Unlike Reset, any settings existing prior to Partial Reset (i.e., programming method and partial flag default offsets) are retained. Partial Reset is useful since it permits flushing of the FIFO memory without changing any configuration settings.

These devices have two modes of operation: In the IDT Standard mode, the first word written to an empty FIFO is deposited into the memory array. A read operation is required to access that word (along with all other words residing in memory). In the First Word Fall Through mode (FWFT), the first word written to an empty FIFO appears automatically on the outputs, no read operation required (Nevertheless, accessing subsequent words does necessitate a formal read request). The state of the BE/FWFT pin during Reset determines the mode in use.

The FIFO has a combined Empty/Output Ready Flag (EF/OR) and a combined Full/Input Ready Flag (FF/IR). The EF and FF functions are selected in the IDT Standard mode. EF indicates whether or not the FIFO memory is empty. FF shows whether the memory is full or not. The IR and OR functions are selected in the First Word Fall Through mode. IR indicates whether or not the FIFO has available memory locations. OR shows whether the FIFO has data available for reading or not. It marks the presence of valid data on the outputs.

The FIFO has a programmable Almost-Empty flag (AE) and a programmable Almost-Full flag (AF). AE indicates when a selected number of words remain in the FIFO memory. AF indicates when the FIFO contains more than a selected number of words. FF/IR and AF are two-stage synchronized to the port clock that writes data into its array. EF/OR and AE are two-stage synchronized to the port clock that reads data from its array. Programmable offsets for AE and AF are loaded in parallel using Port A or in serial via the SD input. The Serial Programming Mode pin (SPM) makes this selection. Three default offset settings are also provided. The AE threshold can be set at 8, 16 or 64 locations from the empty boundary and the AF threshold can be set at 8, 16 or 64 locations from the full boundary. All these choices are made using the FS0 and FS1 inputs during Reset.

Two or more devices may be used in parallel to create wider data paths. In First Word Fall Through mode, more than one device may be connected in series to create greater word depths. The addition of external components is unnecessary.

If, at any time, the FIFO is not actively performing a function, the chip will automatically power down. During the power down state, supply current consumption (ICC) is at a minimum. Initiating any operation (by activating control inputs) will immediately take the device out of the Power Down state.

The IDT72V3623/72V3643 are characterized for operation from 0°C to 70°C. Industrial temperature range (-40°C to +85°C) is available by special order. They are fabricated using high speed, submicron CMOS technology.
## PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A0-A35</td>
<td>Port A Data</td>
<td>I/O</td>
<td>36-bit bidirectional data port for side A.</td>
</tr>
<tr>
<td>AE</td>
<td>Almost-Empty Flag (Port B)</td>
<td>O</td>
<td>Programmable Almost-Empty flag synchronized to CLKB. It is LOW when the number of words in the FIFO is less than or equal to the value in the Almost-Empty B offset register, X.</td>
</tr>
<tr>
<td>AF</td>
<td>Almost-Full Flag (Port A)</td>
<td>O</td>
<td>Programmable Almost-Full flag synchronized to CLKA. It is LOW when the number of empty locations in the FIFO is less than or equal to the value in the Almost-Full A offset register, Y.</td>
</tr>
<tr>
<td>B0-B35</td>
<td>Port B Data</td>
<td>I/O</td>
<td>36-bit bidirectional data port for side B.</td>
</tr>
<tr>
<td>BE/FWFT</td>
<td>Big-Endian/First Word Fall Through</td>
<td>I</td>
<td>This is a dual purpose pin. During Master Reset, a HIGH on BE will select Big-Endian operation. In this case, depending on the bus size, the most significant byte or word written to Port A is read from Port B first. After Master Reset, this pin selects the timing mode. A HIGH on FWFT selects the Standard mode, a LOW selects First Word Fall Through mode. Once the timing mode has been selected, the level on FWFT must be static throughout device operation.</td>
</tr>
<tr>
<td>BM</td>
<td>Bus-Match Select (Port B)</td>
<td>I</td>
<td>A HIGH on this pin enables either byte or word bus width on Port B, depending on the state of SIZE. A LOW selects long word operation. BM works with SIZE and BE to select the bus size and endian arrangement for Port B. The level of BM must be static throughout device operation.</td>
</tr>
<tr>
<td>CLKA</td>
<td>Port A Clock</td>
<td>I</td>
<td>CLKA is a continuous clock that synchronizes all data transfers through Port A and can be asynchronous or coincident to CLKB. FF/IR and AF are synchronized to the LOW-to-HIGH transition of CLKA.</td>
</tr>
<tr>
<td>CLKB</td>
<td>Port B Clock</td>
<td>I</td>
<td>CLKB is a continuous clock that synchronizes all data transfers through Port B and can be asynchronous or coincident to CLKA. FF/IR and AE are synchronized to the LOW-to-HIGH transition of CLKB.</td>
</tr>
<tr>
<td>CSA</td>
<td>Port A Chip Select</td>
<td>I</td>
<td>CSA must be LOW to enable to LOW-to-HIGH transition of CLKA to read or write on Port A. The A0-A35 outputs are in the high-impedance state when CSA is HIGH.</td>
</tr>
<tr>
<td>CSB</td>
<td>Port B Chip Select</td>
<td>I</td>
<td>CSB must be LOW to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B. The B0-B35 outputs are in the high-impedance state when CSB is HIGH.</td>
</tr>
<tr>
<td>EF/OR</td>
<td>Empty/Output Ready Flag (Port B)</td>
<td>O</td>
<td>This is a dual function pin. In the IDT Standard mode, the EF function is selected. EF indicates whether or not the FIFO memory is empty. In the FWFT mode, the OR function is selected. OR indicates the presence of valid data on the B0-B35 outputs, available for reading. EF/OR is synchronized to the LOW-to-HIGH transition of CLKB.</td>
</tr>
<tr>
<td>ENA</td>
<td>Port A Enable</td>
<td>I</td>
<td>ENA must be HIGH to enable a LOW-to-HIGH transition of CLKA to read or write data on Port A.</td>
</tr>
<tr>
<td>ENB</td>
<td>Port B Enable</td>
<td>I</td>
<td>ENB must be HIGH to enable a LOW-to-HIGH transition of CLKB to read or write data on Port B.</td>
</tr>
<tr>
<td>FF/IR</td>
<td>Full/Input Ready Flag (Port A)</td>
<td>O</td>
<td>This is a dual function pin. In the IDT Standard mode, the FF function is selected. FF indicates whether or not the FIFO memory is full. In the FWFT mode, the IR function is selected. IR indicates whether or not there is space available for writing to the FIFO memory. FF/IR is synchronized to the LOW-to-HIGH transition of CLKA.</td>
</tr>
<tr>
<td>FS1/SEN</td>
<td>Flag Offset Select 1/Serial Enable</td>
<td>I</td>
<td>FS1/SEN and FS0/SD are dual-purpose inputs used for flag offset register programming. During Reset, FS1/SEN and FS0/SD, together with SPM, select the flag offset programming method. Three offset register programming methods are available: automatically load one of three preset values (8, 16, or 64), parallel load from Port A, and serial load.</td>
</tr>
<tr>
<td>FS0/SD</td>
<td>Flag Offset Serial Data</td>
<td>I</td>
<td>When serial load is selected for flag offset register programming, FS1/SEN is used as an enable synchronous to the LOW-to-HIGH transition of CLKA. When FS1/SEN is LOW, a rising edge on CLKA load the bit present on FS0/SD into the X and Y registers. The number of bit writes required to program the offset registers is 16 for the IDT72V3623 and 20 for the IDT72V3643. The first bit write stores the Y-register MSB and the last bit write stores the X-register LSB.</td>
</tr>
</tbody>
</table>
## PIN DESCRIPTIONS (CONTINUED)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBA</td>
<td>Port A Mailbox Select</td>
<td>I</td>
<td>A HIGH level on MBA chooses a mailbox register for a Port A read or write operation.</td>
</tr>
<tr>
<td>MBB</td>
<td>Port B Mailbox Select</td>
<td>I</td>
<td>A HIGH level on MBB chooses a mailbox register for a Port B read or write operation. When the B0-B35 outputs are active, a HIGH level on MBB selects data from the mail1 register for output and a LOW level selects FIFO data for output.</td>
</tr>
<tr>
<td>MBF1</td>
<td>Mail1 Register Flag</td>
<td>O</td>
<td>MBF1 is set LOW by a LOW-to-HIGH transition of CLKA that writes data to the mail1 register. Writes to the mail1 register are inhibited while MBF1 is LOW. MBF1 is set HIGH by a LOW-to-HIGH transition of CLKB when a Port B read is selected and MBB is HIGH. MBF1 is set HIGH following either a Reset (RS1) or Partial Reset (PRS).</td>
</tr>
<tr>
<td>MBF2</td>
<td>Mail2 Register Flag</td>
<td>O</td>
<td>MBF2 is set LOW by a LOW-to-HIGH transition of CLKB that writes data to the mail2 register. Writes to the mail2 register are inhibited while MBF2 is LOW. MBF2 is set HIGH by a LOW-to-HIGH transition of CLKA when a Port A read is selected and MBA is HIGH. MBF2 is set HIGH following either a Reset (RS2) or Partial Reset (PRS).</td>
</tr>
<tr>
<td>RST, RS2</td>
<td>Resets</td>
<td>I</td>
<td>A LOW on both pins initializes the FIFO read and write pointers to the first location of memory and sets the Port B output register to all zeroes. A LOW-to-HIGH transition on RST selects the programming method (serial or parallel) and one of three programmable flag default offsets. It also configures Port B for bus size and endian arrangement. Four LOW-to-HIGH transitions of CLKA and four LOW-to-HIGH transitions of CLKB must occur while RST is LOW.</td>
</tr>
<tr>
<td>PRS</td>
<td>Partial Reset</td>
<td>I</td>
<td>A LOW on this pin initializes the FIFO read and write pointers to the first location of memory and sets the Port B output register to all zeroes. During Partial Reset, the currently selected bus size, endian arrangement, programming method (serial or parallel), and programmable flag settings are all retained.</td>
</tr>
<tr>
<td>SIZE</td>
<td>Bus Size Select (Port B)</td>
<td>I</td>
<td>A HIGH on this pin when BM is HIGH selects byte bus (9-bit) size on Port B. A LOW on this pin when BM is HIGH selects word (18-bit) bus size. SIZE works with BM and BE to select the bus size and endian arrangement for Port B. The level of SIZE must be static throughout device operation.</td>
</tr>
<tr>
<td>SPM</td>
<td>Serial Programming Mode</td>
<td>I</td>
<td>A LOW on this pin selects serial programming of partial flag offsets. A HIGH on this pin selects parallel programming or default offsets (8, 16, or 64).</td>
</tr>
<tr>
<td>W/RA</td>
<td>Port A Write/ Read Select</td>
<td>I</td>
<td>A HIGH selects a write operation and a LOW selects a read operation on Port A for a LOW-to-HIGH transition of CLKA. The A0-A35 outputs are in the HIGH impedance state when W/RA is HIGH.</td>
</tr>
<tr>
<td>W/RB</td>
<td>Port B Write/ Read Select</td>
<td>I</td>
<td>A LOW selects a write operation and a HIGH selects a read operation on Port B for a LOW-to-HIGH transition of CLKB. The B0-B35 outputs are in the HIGH impedance state when W/RB is LOW.</td>
</tr>
</tbody>
</table>
### Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Commercial</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply Voltage Range</td>
<td>–0.5 to +4.6</td>
<td>V</td>
</tr>
<tr>
<td>VI(^{(2)})</td>
<td>Input Voltage Range</td>
<td>–0.5 to VCC+0.5</td>
<td>V</td>
</tr>
<tr>
<td>VO(^{(2)})</td>
<td>Output Voltage Range</td>
<td>–0.5 to VCC+0.5</td>
<td>V</td>
</tr>
<tr>
<td>I(\text{I}K)</td>
<td>Input Clamp Current ((\text{VI &lt; 0 or VI &gt; VCC}))</td>
<td>±20</td>
<td>mA</td>
</tr>
<tr>
<td>I(\text{O}K)</td>
<td>Output Clamp Current ((\text{VO = &lt; 0 or VO &gt; VCC}))</td>
<td>±50</td>
<td>mA</td>
</tr>
<tr>
<td>I(\text{O}UT)</td>
<td>Continuous Output Current ((\text{VO = 0 to VCC}))</td>
<td>±50</td>
<td>mA</td>
</tr>
<tr>
<td>I(\text{O}UT)</td>
<td>Continuous Current Through VCC or GND</td>
<td>±400</td>
<td>mA</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature Range</td>
<td>–65 to 150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded provided the input and output current ratings are observed.

### Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC(^{(2)})</td>
<td>Supply Voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>High-Level Input Voltage</td>
<td>2</td>
<td>—</td>
<td>VCC+0.5</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Low-Level Input Voltage</td>
<td>—</td>
<td>—</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>IOH</td>
<td>High-Level Output Current</td>
<td>—</td>
<td>—</td>
<td>–4</td>
<td>mA</td>
</tr>
<tr>
<td>IOL</td>
<td>Low-Level Output Current</td>
<td>—</td>
<td>—</td>
<td>8</td>
<td>mA</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature</td>
<td>0</td>
<td>—</td>
<td>70</td>
<td>°C</td>
</tr>
</tbody>
</table>

**NOTE:**
1. For 10ns (100 MHz operation), VCC = 3.3V ±0.15V; TA = 0° to +70°C; JEDEC JESD8-A compliant.

### Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless otherwise noted)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>IDT72V3623</th>
<th>Commercial</th>
<th>t(\text{CLK} = 10)(^{(1)}), 15ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOH</td>
<td>Output Logic &quot;1&quot; Voltage</td>
<td>(\text{VCC = 3.0V, IOH = –4 mA})</td>
<td>2.4</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Logic &quot;0&quot; Voltage</td>
<td>(\text{VCC = 3.0V, IOL = 8 mA})</td>
<td>—</td>
<td>—</td>
<td>0.5</td>
</tr>
<tr>
<td>ILI</td>
<td>Input Leakage Current (Any Input)</td>
<td>(\text{VCC = 3.6V, VI = VCC or 0})</td>
<td>—</td>
<td>—</td>
<td>±10</td>
</tr>
<tr>
<td>ILO</td>
<td>Output Leakage Current</td>
<td>(\text{VCC = 3.6V, VO = VCC or 0})</td>
<td>—</td>
<td>—</td>
<td>±10</td>
</tr>
<tr>
<td>ICC2(^{(2)})</td>
<td>Standby Current (with CLKA and CLKB running)</td>
<td>(\text{VCC = 3.6V, VI = VCC - 0.2V or 0})</td>
<td>—</td>
<td>—</td>
<td>5</td>
</tr>
<tr>
<td>ICC3(^{(2)})</td>
<td>Standby Current (no clocks running)</td>
<td>(\text{VCC = 3.6V, VI = VCC - 0.2V or 0})</td>
<td>—</td>
<td>—</td>
<td>1</td>
</tr>
<tr>
<td>CIN(^{(4)})</td>
<td>Input Capacitance</td>
<td>(\text{VI = 0, f = 1 MHz})</td>
<td>4</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>COUT(^{(4)})</td>
<td>Output Capacitance</td>
<td>(\text{VO = 0, f = 1 MHz})</td>
<td>8</td>
<td>—</td>
<td>—</td>
</tr>
</tbody>
</table>

**NOTES:**
1. For 10ns speed grade only: VCC = 3.3V ±0.15V; TA = 0° to +70°C; JEDEC JESD8-A compliant.
2. All typical values are at VCC = 3.3V, TA = 25°C.
3. For additional ICC information, see Figure 1, Typical Characteristics: Supply Current (ICC) vs. Clock Frequency (fs).
4. Characterized values, not currently tested.
5. Industrial temperature range is available by special order.

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DETERMINING ACTIVE CURRENT CONSUMPTION AND POWER DISSIPATION

The $I_{CC}(f)$ current for the graph in Figure 1 was taken while simultaneously reading and writing a FIFO on the IDT72V3623/72V3643 with CLKA and CLKB set to $f_s$. All data inputs and data outputs change state during each clock cycle to consume the highest supply current. Data outputs were disconnected to normalize the graph to a zero capacitance load. Once the capacitance load per data-output channel and the number of IDT72V3623/72V3643 inputs driven by TTL HIGH levels are known, the power dissipation can be calculated with the equation below.

CALCULATING POWER DISSIPATION

With $I_{CC}(f)$ taken from Figure 1, the maximum power dissipation ($P_T$) of these FIFOs may be calculated by:

$$P_T = V_{CC} \times I_{CC}(f) + \sum_{n} (C_L \times V_{CC}^2 \times f_0)$$

where:

- $N$ = number of used outputs (36-bit (long word), 18-bit (word) or 9-bit (byte) bus size)
- $C_L$ = output capacitance load
- $f_0$ = switching frequency of an output

Figure 1. Typical Characteristics: Supply Current ($I_{CC}$) vs. Clock Frequency ($f_s$)

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## TIMING REQUIREMENTS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE

Commercial: \( V_{cc} = 3.3V \pm 0.30V \); for 10ns (100 MHz) operation, \( V_{cc} = 3.3V \pm 0.15V \); \( T_A = 0^\circ C \) to +70\(^{\circ} C \); JEDEC JESD8-A compliant

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>IDT72V3623L10(1)</th>
<th>IDT72V3623L15(1)</th>
<th>IDT72V3643L10(1)</th>
<th>IDT72V3643L15</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_s )</td>
<td>Clock Frequency, CLKA or CLKB</td>
<td>—</td>
<td>100</td>
<td>—</td>
<td>66.7</td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{CLK} )</td>
<td>Clock Cycle Time, CLKA or CLKB</td>
<td>10</td>
<td>15</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{CLKH} )</td>
<td>Pulse Duration, CLKA or CLKB HIGH</td>
<td>4.5</td>
<td>6</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{CLKL} )</td>
<td>Pulse Duration, CLKA and CLKB LOW</td>
<td>4.5</td>
<td>6</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DS} )</td>
<td>Setup Time, A0-A35 before CLKA(^\uparrow) and B0-B35 before CLKB(^\uparrow)</td>
<td>3</td>
<td>4</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{ENS1} )</td>
<td>Setup Time, ( \overline{CSA} ), before CLKA(^\uparrow) and CLKB(^\uparrow)</td>
<td>4</td>
<td>4.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{ENS2} )</td>
<td>Setup Time, ENA, ( \overline{WRA} ) and MBA before CLKA(^\uparrow) and CLKB(^\uparrow)</td>
<td>3</td>
<td>4.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{RSTS} )</td>
<td>Setup Time, ( RS1 ) or ( PRS ) LOW before CLKA(^\uparrow) or CLKB(^\uparrow)(2)</td>
<td>5</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{FSS} )</td>
<td>Setup Time, FS0 and FS1 before ( RS1 ) HIGH</td>
<td>7.5</td>
<td>7.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{BES} )</td>
<td>Setup Time, BE/FWFT before ( RS1 ) HIGH</td>
<td>7.5</td>
<td>7.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SPMS} )</td>
<td>Setup Time, SPM before ( RS1 ) HIGH</td>
<td>7.5</td>
<td>7.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SDS} )</td>
<td>Setup Time, FS0/SD before CLKA(^\uparrow)</td>
<td>3</td>
<td>4</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SENS} )</td>
<td>Setup Time, FS1/( SEN ) before CLKA(^\uparrow)</td>
<td>3</td>
<td>4</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{FWS} )</td>
<td>Setup Time, FWFT before CLKA(^\uparrow)</td>
<td>0</td>
<td>—</td>
<td>0</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{DH} )</td>
<td>Hold Time, A0-A35 after CLKA(^\uparrow) and B0-B35 after CLKB(^\uparrow)</td>
<td>0.5</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{ENH} )</td>
<td>Hold Time, ( \overline{CSA} ), ( \overline{WRA} ), ENA, and MBA before CLKA(^\uparrow) and CLKB(^\uparrow)</td>
<td>0.5</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{RSTH} )</td>
<td>Hold Time, ( RS1 ) or ( PRS ) LOW after CLKA(^\uparrow) or CLKB(^\uparrow)(2)</td>
<td>4</td>
<td>4</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{FSH} )</td>
<td>Hold Time, FS0 and FS1 after ( RS1 ) HIGH</td>
<td>2</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{BEH} )</td>
<td>Hold Time, BE/FWFT after ( RS1 ) HIGH</td>
<td>2</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SPMH} )</td>
<td>Hold Time, SPM after ( RS1 ) HIGH</td>
<td>2</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SDH} )</td>
<td>Hold Time, FS0/SD after CLKA(^\uparrow)</td>
<td>0.5</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SENH} )</td>
<td>Hold Time, FS1/( SEN ) HIGH after CLKA(^\uparrow)</td>
<td>0.5</td>
<td>1</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SPH} )</td>
<td>Hold Time, FS1/( SEN ) HIGH after ( RS1 ) HIGH</td>
<td>2</td>
<td>2</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>( t_{SKEW1}(3) )</td>
<td>Skew Time between CLKA(^\uparrow) and CLKB(^\uparrow) for ( \overline{EF} )/OR and ( FF )/IR</td>
<td>7.5</td>
<td>7.5</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{SKEW2}(3,4) )</td>
<td>Skew Time between CLKA(^\uparrow) and CLKB(^\uparrow) for ( \overline{AE} ) and ( AF )</td>
<td>12</td>
<td>12</td>
<td>—</td>
<td>—</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. For 10ns speed grade only: \( V_{cc} = 3.3V \pm 0.15V \); \( T_A = 0^\circ C \) to +70\(^{\circ} C \); JEDEC JESD8-A compliant.
2. Requirement to count the clock edge as one of at least four needed to reset a FIFO.
3. Skew time is not a timing constraint for proper device operation and is only included to illustrate the timing relationship between CLKA cycle and CLKB cycle.
4. Design simulated, not tested.
5. Industrial temperature range is available by special order.
### SWITCHING CHARACTERISTICS OVER RECOMMENDED RANGES OF SUPPLY VOLTAGE AND OPERATING FREE-AIR TEMPERATURE, $CL = 30 \, \text{pF}$

Commercial: $V_{cc}=3.3V \pm 0.30V$; for 10ns (100 MHz) operation, $V_{cc}=3.3V \pm 0.15V$; $T_A = 0^\circ C$ to $+70^\circ C$; JEDEC JESD8-A compliant

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min.</th>
<th>Max.</th>
<th>Min.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$tA$</td>
<td>Access Time, $\uparrow$ $\text{CLKA}$ to $\uparrow$ $\text{A0-A35}$ and $\uparrow$ $\text{CLKB}$ to $\uparrow$ $\text{B0-B35}$</td>
<td>2</td>
<td>6.5</td>
<td>2</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$tWFF$</td>
<td>Propagation Delay Time, $\uparrow$ $\text{CLKA}$ to $\uparrow$ $\text{FF}$/$\text{IR}$</td>
<td>2</td>
<td>6.5</td>
<td>2</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>$tREF$</td>
<td>Propagation Delay Time, $\uparrow$ $\text{CLKB}$ to $\uparrow$ $\text{EF}$/$\text{OR}$</td>
<td>1</td>
<td>6.5</td>
<td>1</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>$tPAE$</td>
<td>Propagation Delay Time, $\uparrow$ $\text{CLKB}$ to $\uparrow$ $\text{AE}$</td>
<td>1</td>
<td>6.5</td>
<td>1</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>$tPAF$</td>
<td>Propagation Delay Time, $\uparrow$ $\text{CLKA}$ to $\uparrow$ $\text{AF}$</td>
<td>1</td>
<td>6.5</td>
<td>1</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>$tPMF$</td>
<td>Propagation Delay Time, $\uparrow$ $\text{CLKA}$ to $\text{MBF}_1$ LOW or $\text{MBF}_2$ LOW and $\uparrow$ $\text{CLKB}$ to $\text{MBF}_2$ LOW or $\text{MBF}_1$ HIGH</td>
<td>0</td>
<td>6.5</td>
<td>0</td>
<td>8</td>
<td>ns</td>
</tr>
<tr>
<td>$tPMR$</td>
<td>Propagation Delay Time, $\uparrow$ $\text{CLKA}$ to $\uparrow$ $\text{B0-B35}$ and $\uparrow$ $\text{CLKB}$ to $\uparrow$ $\text{A0-A35}$</td>
<td>2</td>
<td>8</td>
<td>2</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$tMDV$</td>
<td>Propagation Delay Time, $\text{MBA}$ to $\uparrow$ $\text{A0-A35}$ valid and MBB to $\uparrow$ $\text{B0-B35}$ Valid</td>
<td>2</td>
<td>6.5</td>
<td>2</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$tRSF$</td>
<td>Propagation Delay Time, $\text{RS}_1$ or $\text{PRS}_1$ LOW to $\text{AE}$ LOW, $\text{AF}$ HIGH, $\text{MBF}_1$ HIGH and $\text{MBF}_2$ HIGH</td>
<td>1</td>
<td>10</td>
<td>1</td>
<td>15</td>
<td>ns</td>
</tr>
<tr>
<td>$tEN$</td>
<td>Enable Time, $\overline{\text{CSA}}$ and $\overline{\text{W/RA}}$ LOW to $\text{A0-A35}$ Active and $\overline{\text{CSB}}$ LOW and $\overline{\text{W/RB}}$ HIGH to $\text{B0-B35}$ Active</td>
<td>2</td>
<td>6</td>
<td>2</td>
<td>10</td>
<td>ns</td>
</tr>
<tr>
<td>$tDIS$</td>
<td>Disable Time, $\overline{\text{CSA}}$ or $\overline{\text{W/RA}}$ HIGH to $\text{A0-A35}$ at high impedance and $\overline{\text{CSB}}$ HIGH or $\overline{\text{W/RB}}$ LOW to $\text{B0-B35}$ at high impedance</td>
<td>1</td>
<td>6</td>
<td>1</td>
<td>8</td>
<td>ns</td>
</tr>
</tbody>
</table>

**NOTES:**

1. For 10ns speed grade only: $V_{cc} = 3.3V \pm 0.15V$, $T_A = 0^\circ C$ to $+70^\circ C$; JEDEC JESD8-A compliant.
2. Writing data to the mail1 register when the $\text{B0-B35}$ outputs are active and MBB is HIGH.
3. Writing data to the mail2 register when the $\text{A0-A35}$ outputs are active and MBA is HIGH.
4. Industrial temperature range is available by special order.
SIGNAL DESCRIPTION

RESET (RS1, RS2)

After power up, a Reset operation must be performed by providing a LOW pulse to RS1 and RS2 simultaneously. Afterwards, the FIFO memory of the IDT72V3623/72V3643 undergoes a complete reset by taking its Reset (RS1 and RS2) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Reset inputs can switch asynchronously to the clocks. A Partial Reset initializes the internal read and write pointers and forces the Full/Input Ready flag (FF/IR) LOW, the Empty/Output Ready flag (EF/OR) LOW, the Almost-Empty flag (AE) LOW, and the Almost-Full flag (AF) HIGH. A Reset (RS1) also forces the Mailbox flag (MBF1) of the parallel mailbox register HIGH, and at the same time the RS2 and MBF2 operate likewise. After a Reset, the FIFO’s Full/Input Ready flag is set HIGH after two write clock cycles to begin normal operation.

A LOW-to-HIGH transition on the FIFO Reset (RS1) input latches the value of the Big-Endian (BE) input for determining the order by which bytes are transferred through Port B.

A LOW-to-HIGH transition on the FIFO Reset (RS1) input also latches the values of the Flag Select (FS0, FS1) and Serial Programming Mode (SPM) inputs for choosing the Almost-Full and Almost-Empty offset programming method (for details see Table 1, Flag Programming, and Almost-Empty and Almost-Full flag offset programming section). The relevant Reset timing diagram can be found in Figure 3.

PARTIAL RESET (PRS)

The FIFO memory of the IDT72V3623/72V3643 undergoes a limited reset by taking its Partial Reset (PRS) input LOW for at least four Port A clock (CLKA) and four Port B clock (CLKB) LOW-to-HIGH transitions. The Partial Reset input can switch asynchronously to the clocks. A Partial Reset initializes the internal read and write pointers and forces the Full/Input Ready flag (FF/IR) LOW, the Empty/Output Ready flag (EF/OR) LOW, the Almost-Empty flag (AE) LOW, and the Almost-Full flag (AF) HIGH. A Partial Reset also forces the Mailbox flag (MBF1, MBF2) of the parallel mailbox register HIGH. After a Partial Reset, the FIFO’s Full/Input Ready flag is set HIGH after two Write Clock cycles to begin normal operation. See Figure 4, Partial Reset (IDT Standard and FWFT Modes) for the relevant timing diagram.

Whatever flag offsets, programming method (parallel or serial), and timing mode (FWFT or IDT Standard mode) are currently selected at the time a Partial Reset is initiated, those settings will be remain unchanged upon completion of the reset operation. A Partial Reset may be useful in the case where reprogramming a FIFO following a Reset would be inconvenient.

BIG-ENDIAN/FIRST WORD FALL THROUGH (BE/FWFT)

— ENDIAN SELECTION

This is a dual purpose pin. At the time of Reset, the BE select function is active, permitting a choice of Big- or Little-Endian byte arrangement for data read from Port B. This selection determines the order by which bytes (or words) of data are transferred through this port. For the following illustrations, assume that a byte (or word) bus size has been selected for Port B. (Note that when Port B is configured for a long word size, the Big-Endian function has no application and the BE input is a “don’t care”.)

A HIGH on the BE/FWFT input when the Reset (RS1) input goes from LOW to HIGH will select a Big-Endian arrangement. In this case, the most significant byte (word) of the long word written to Port A will be read from Port B first; the least significant byte (word) of the long word written to Port A will be read from Port B last.

A LOW on the BE/FWFT input when the Reset (RS1) input goes from LOW to HIGH will select a Little-Endian arrangement. In this case, the least significant byte (word) of the long word written to Port A will be read from Port B first; the most significant byte (word) of the long word written to Port A will be read from Port B last.

— TIMING MODE SELECTION

After Reset, the FWFT select function is active, permitting a choice between two possible timing modes: IDT Standard mode or First Word Fall Through (FWFT) mode. Once the Reset (RS1) input is HIGH, a HIGH on the BE/FWFT input during the next LOW-to-HIGH transition of CLKA and CLKB will select IDT Standard mode. This mode uses the Empty Flag function (EF) to indicate whether or not there are any words present in the FIFO memory. It uses the Full Flag function (FF) to indicate whether or not the FIFO memory has any free space for writing. In IDT Standard mode, every word read from the FIFO, including the first, must be requested using a formal read operation.

Once the Reset (RS1) input is HIGH, a LOW on the BE/FWFT input during the next LOW-to-HIGH transition of CLKA and CLKB will select FWFT mode. This mode uses the Output Ready function (OR) to indicate whether or not there is valid data at the data outputs (B0-B35). It also uses the Input Ready function (IR) to indicate whether or not the FIFO memory has any free space for writing. In the FWFT mode, the first word written to an empty FIFO goes directly to data outputs, no read request necessary. Subsequent words must be accessed by performing a formal read operation.

Following Reset, the level applied to the BE/FWFT input to choose the desired timing mode must remain static throughout FIFO operation. Refer to Figure 3 (Reset) for a First Word Fall Through select timing diagram.

PROGRAMMING THE ALMOST-EMPTY AND ALMOST-FULL FLAGS

Two registers in the IDT72V3623/72V3643 are used to hold the offset values for the Almost-Empty and Almost-Full flags. The Almost-Empty flag (AE) Offset register is labeled X and Almost-Full flag (AF) Offset register is labeled Y. The offset registers can be loaded with preset values during the reset of the FIFO, programmed in parallel using the FIFO’s Port A data inputs, or programmed in serial using the Serial Data (SD) input (see Table 1). SPM, FS0/SD, and FS1/SEN function the same way in both IDT Standard and FWFT modes.

— PRESET VALUES

To load a FIFO’s Almost-Empty flag and Almost-Full flag Offset registers with one of the three preset values listed in Table 1, the Serial Program Mode (SPM) and at least one of the flag-select inputs must be HIGH during the LOW-to-HIGH transition of the Reset input (RS1). For example, to load the preset value of 64 into X and Y, SPM, FS0 and FS1 must be HIGH when RS1 returns HIGH. For the relevant preset value loading timing diagram, see Figure 3.

NOTE:

1. Either a HIGH or LOW can be applied to a “don’t care” input with no change to the logical operation of the FIFO. Nevertheless, inputs that are temporarily “don’t care” (along with unused inputs) must not be left open, rather they must be either HIGH or LOW.
TABLE 1 — FLAG PROGRAMMING

<table>
<thead>
<tr>
<th>SPM</th>
<th>FS1/SEN</th>
<th>FS0/SD</th>
<th>RS1</th>
<th>X AND Y REGISTERS(1)</th>
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</thead>
<tbody>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
<td>↑</td>
<td>64</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>L</td>
<td>↑</td>
<td>16</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>↑</td>
<td>8</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>↑</td>
<td>Parallel programming via Port A</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>L</td>
<td>↑</td>
<td>Serial Programming via SD</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>H</td>
<td>↑</td>
<td>reserved</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>H</td>
<td>↑</td>
<td>reserved</td>
</tr>
<tr>
<td>L</td>
<td>L</td>
<td>L</td>
<td>↑</td>
<td>reserved</td>
</tr>
</tbody>
</table>

NOTE:
1. X register holds the offset for $AE$; Y register holds the offset for $AF$.

— PARALLEL LOAD FROM PORT A
To program the X and Y registers from Port A, perform a Reset on with SPM HIGH and FS0 and FS1 LOW during the LOW-to-HIGH transition of RS1. After this reset is complete, the first two writes to the FIFO do not store data in RAM. The first two write cycles load the offset registers X and Y in the order Y, X. On the third write cycle the FIFO is ready to be loaded with data word. See Figure 5, Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT modes), for a detailed timing diagram. The Port A data inputs used by the offset registers are (A7-A0), (A8-A0), or (A9-A0) for the IDT72V3623 or IDT72V3643, respectively. The two registers are written in the order Y, X. On the third write cycle the FIFO is ready to be loaded with data word. See Figure 6, Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT modes).

FIFO WRITE/READ OPERATION
The state of the Port A data (A0-A35) lines is controlled by Port A Chip Select (CSA) and Port A Write/Read select (WR/RA). The A0-A35 lines are in the High-impedance state when either CSA or WR/RA is HIGH. The A0-A35 lines are active outputs when both CSA and WR/RA are LOW.

Data is loaded into the FIFO from the A0-A35 inputs on a LOW-to-HIGH transition of CLKA when CSA is LOW, WR/RA is HIGH, ENA is HIGH, MBA is LOW, and FF/IR is HIGH (see Table 2). FIFO writes on Port A are independent of any concurrent reads on Port B.

The Port B control signals are identical to those of Port A with the exception that the Port B Write/Read select (WR/ RB) is the inverse of the Port A Write/Read select (WR/RA). The state of the Port B data (B0-B35) lines is controlled by the Port B Chip Select (CSB) and Port B Write/Read select (WR/ RB). The B0-B35 lines are in the high-impedance state when either CSB is HIGH or WR/ RB is LOW. The B0-B35 lines are active outputs when CSB is LOW and WR/ RB is HIGH.

Data is read from the FIFO to the B0-B35 outputs by a LOW-to-HIGH transition of CLKB when CSB is LOW, WR/ RB is HIGH, ENB is HIGH, MBB is LOW, and EF/OR is HIGH (see Table 3). FIFO reads on Port B are independent of any concurrent writes on Port A.

The setup and hold time constraints to the port clocks for the port Chip Selects and Write/Read selects are only for enabling write and read operations and are not related to high-impedance control of the data outputs. If a port enable is LOW during a clock cycle, the port’s Chip Select and Write/Read select may change states during the setup and hold time window of the cycle.

When operating the FIFO in FWFT mode and the Output Ready flag is LOW, the next word written is automatically sent to the FIFO’s output register by the LOW-to-HIGH transition of the port clock that sets the Output Ready flag HIGH. When the Output Ready flag is HIGH, data residing in the FIFO’s memory array is clocked to the output register only when a read is selected using the port’s Chip Select, Write/Read select, Enable, and Mailbox select.

When operating the FIFO in IDT Standard mode, regardless of whether the Empty Flag is LOW or HIGH, data residing in the FIFO’s memory array is clocked to the output register only when a read is selected using the port's Chip Select, Write/Read select, Enable, and Mailbox select. Port A Write timing diagram can be found in Figure 7. Relevant Port B Read timing diagrams together with Bus-Matching and Endian select can be found in Figure 8, 9 and 10.

Synchronized FIFO Flags
Each FIFO is synchronized to its port clock through at least two flip-flop stages. This is done to improve flag-signal reliability by reducing the probability of metastable events when CLKA and CLKB operate asynchronously to one another. FF/IR and AE are synchronized to CLKA, EF/ OR and AF are synchronized to CLKB. Table 4 shows the relationship of each port flag to the number of words stored in memory.

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These are dual purpose flags. In the FWFT mode, the Output Ready (OR) function is selected. When the Output-Ready flag is HIGH, new data is present in the FIFO output register. When the Output Ready flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

In the IDT Standard mode, the Empty Flag (EF) function is selected. When the Empty Flag is HIGH, data is available in the FIFO’s memory for reading to the output register. When the Empty Flag is LOW, the previous data word is present in the FIFO output register and attempted FIFO reads are ignored.

The Empty/Output Ready flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). For both the FWFT and IDT Standard modes, the FIFO read pointer is incremented each time a new word is clocked to its output register. The state machine that controls an Output Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is empty, empty+1, or empty+2.

In FWFT mode, from the time a word is written to an empty FIFO, it can be shifted to the FIFO output register in a minimum of three cycles of the Output Ready flag synchronizing clock. Therefore, an Output Ready flag is LOW if a word in memory is the next data to be sent to the FIFO output register and attempted FIFO reads are ignored.
three cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Output Ready flag of the FIFO remains LOW until the third LOW-to-HIGH transition of the synchronizing clock occurs, simultaneously forcing the Output Ready flag HIGH and shifting the word to the FIFO output register.

In IDT Standard mode, from the time a word is written to a FIFO, the Empty Flag will indicate the presence of data available for reading in a minimum of two cycles of the Empty Flag synchronizing clock. Therefore, an Empty Flag is LOW if a word in memory is the next data to be sent to the FIFO output register and two cycles of the port Clock that reads data from the FIFO have not elapsed since the time the word was written. The Empty Flag of the FIFO remains LOW until the second LOW-to-HIGH transition of the synchronizing clock occurs, forcing the Empty Flag HIGH; only then can data be read.

A LOW-to-HIGH transition on an Empty/Output Ready flag synchronizing clock begins the first synchronization cycle of a write if the clock transition occurs at time tsKEW1 or greater after the write. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 11 and 12).

**FULL/INPUT READY FLAGS (FF/IR)**

This is a dual purpose flag. In FWFT mode, the Input Ready (IR) function is selected. In IDT Standard mode, the Full Flag (FF) function is selected. For both timing modes, when the Full/Input Ready flag is HIGH, a memory location is free in the FIFO to receive new data. No memory locations are free when the Full/Input Ready flag is LOW and attempted writes to the FIFO are ignored.

The Full/Input Ready flag of a FIFO is synchronized to the port clock that writes data to its array (CLKA). For both FWFT and IDT Standard modes, each time a word is written to a FIFO, its write pointer is incremented. The state machine that controls a Full/Ready flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is full, full-1, or full-2. From the time a word is read from a FIFO, its previous memory location is ready to be written to in a minimum of two cycles of the Full/Input Ready flag synchronizing clock. Therefore, an Full/Ready flag is LOW if less than two cycles of the Full/Input Ready flag synchronizing clock have elapsed since the next memory write location has been read. The second LOW-to-HIGH transition on the Full/Ready flag synchronizing clock after the read sets the Full/Input Ready flag HIGH.

A LOW-to-HIGH transition on a Full/Ready flag synchronizing clock begins the first synchronization cycle of a read if the clock transition occurs at time tsKEW1 or greater after the read. Otherwise, the subsequent clock cycle can be the first synchronization cycle (see Figures 13 and 14).

**ALMOST-EMPTY FLAG (AE)**

The Almost-Empty flag of a FIFO is synchronized to the port clock that reads data from its array (CLKB). The state machine that controls an Almost-Empty flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-empty, almost-empty+1, or almost-empty+2. The Almost-Empty state is defined by the contents of register X. These registers are loaded with preset values during a FIFO reset, programmed from Port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming section). An Almost-Empty flag is LOW when the number of words in its FIFO is greater than or equal to \((256-Y)\) or \((1,024-Y)\) for the IDT72V3623 or IDT72V3643 respectively. An Almost-Empty flag is HIGH when the number of words in its FIFO is less than or equal to \([256-(Y+1)]\) or \([1,024-(Y+1)]\) for the IDT72V3623 or IDT72V3643 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for its Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing \((X+1)\) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the \((X+1)\) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the \((X+1)\) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time tsKEW2 or greater after the write that fills the FIFO to \((X+1)\) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle. (See Figure 15).

**ALMOST-FULL FLAG (AF)**

The Almost-Full flag of a FIFO is synchronized to the port clock that writes data to its array. The state machine that controls an Almost-Full flag monitors a write pointer and read pointer comparator that indicates when the FIFO memory status is almost-full, almost-full-1, or almost-full-2. The Almost-Full state is defined by the contents of register Y. These registers are loaded with preset values during a FIFO reset or, programmed from Port A, or programmed serially (see Almost-Empty flag and Almost-Full flag offset programming section). An Almost-Full flag is LOW when the number of words in its FIFO is greater than or equal to \((256-Y)\) or \((1,024-Y)\) for the IDT72V3623 or IDT72V3643 respectively. An Almost-Full flag is HIGH when the number of words in its FIFO is less than or equal to \([256-(Y+1)]\) or \([1,024-(Y+1)]\) for the IDT72V3623 or IDT72V3643 respectively. Note that a data word present in the FIFO output register has been read from memory.

Two LOW-to-HIGH transitions of the Almost-Full flag synchronizing clock are required after a FIFO read for its Almost-Full flag to reflect the new level of fill. Therefore, the Almost-Empty flag of a FIFO containing \((X+1)\) or more words remains LOW if two cycles of its synchronizing clock have not elapsed since the write that filled the memory to the \((X+1)\) level. An Almost-Empty flag is set HIGH by the second LOW-to-HIGH transition of its synchronizing clock after the FIFO write that fills memory to the \((X+1)\) level. A LOW-to-HIGH transition of an Almost-Empty flag synchronizing clock begins the first synchronization cycle if it occurs at time tsKEW2 or greater after the write that fills the FIFO to \((X+1)\) words. Otherwise, the subsequent synchronizing clock cycle may be the first synchronization cycle. (See Figure 15).

**MAILBOX REGISTERS**

Two 36-bit bypass registers are on the IDT72V3623/72V3643 to pass command and control information between Port A and Port B without putting it in queue. The Mailbox select (MBA, MBB) inputs choose between a mail register and a FIFO for a port data transfer operation. The usable width of both the Mail1 and Mail2 Registers matches the selected bus size for Port B.

A LOW-to-HIGH transition on CLKA writes data to the Mail1 Register when a Port A write is selected by CSÅ, W/RÅ, and ENA with MBA HIGH. If the selected Port B bus size is 36 bits, the usable width of the Mail1 Register employs data lines A0-A35. If the selected Port B bus size is 18 bits, then the usable width of the Mail1 Register employs data lines A0-A17. (In this case, A18-A35 are don’t care inputs.) If the selected Port B bus size is 9 bits, then the usable width of the Mail1 Register employs data lines A0-A8. (In this case, A9-A35 are don’t care inputs.)

A LOW-to-HIGH transition on CLKB writes B0-B35 data to the Mail2 Register when a Port B write is selected by CSB, W/RB, and ENB with MBB HIGH. If the selected Port B bus size is 36 bits, the usable width of...
the Mail employs data lines B0-B35. If the selected Port B bus size is 18
bits, then the usable width of the Mail Register employs data lines B0-
B17. (In this case, B18-B35 are don’t care inputs.) If the selected Port B
bus size is 9 bits, then the usable width of the Mail Register employs data
lines B0-B8. (In this case, B9-B35 are don’t care inputs.)

Writing data to a mail register sets its corresponding flag (MBF1 or
MBF2) LOW. Attempted writes to a mail register are ignored while the
mail flag is LOW.

When data outputs of a port are active, the data on the bus comes from
the FIFO output register when the port Mailbox select input is LOW and from
the mail register when the port Mailbox select input is HIGH.

The Mail Register Flag (MBF1) is set HIGH by a LOW-to-HIGH transition
on CLKB when a Port B read is selected by CSB, W/RB, and ENB with
MBB HIGH. For a 36-bit bus size, 36 bits of mailbox data are placed on
B0-B35. For an 18-bit bus size, 18 bits of mailbox data are placed on B0-
B17. (In this case, B18-B35 are don’t care inputs.) For a 9-bit bus size, 9 bits
of mailbox data are placed on B0-B8. (In this case, B9-B35 are don’t care inputs.)

The Mail Register Flag (MBF2) is set HIGH by a LOW-to-HIGH transition
on CLKA when a Port A read is selected by CSA, W/RA, and ENA with
MBA HIGH.

For a 36-bit bus size, 36 bits of mailbox data are placed on A0-A35.
For an 18-bit bus size, 18 bits of mailbox data are placed on A0-A17. (In
this case, A18-A35 are don’t care inputs.) For a 9-bit bus size, 9 bits
of mailbox data are placed on A0-A8. (In this case, A9-A35 are don’t care inputs.)

The data in a mail register remains intact after it is read and changes
only when new data is written to the register. The Endian select feature
has no effect on mailbox data. For mail register and mail register flag
timing diagrams, see Figure 17 and 18.

BUS SIZING

The Port B bus can be configured in a 36-bit long word, 18-bit word,
or 9-bit byte format for data read from the FIFO. The levels applied to the
Port B Bus Size select (SIZE) and the Bus-Match select (BM) determine
the Port B bus size. These levels should be static throughout FIFO
operation. Both bus size selections are implemented at the completion of
Reset, by the time the Full/Input Ready flag is set HIGH, as shown in
Figure 2.

Two different methods for sequencing data transfer are available for
Port B when the bus size selection is either byte-or word-size. They are
referred to as Big-Endian (most significant byte first) and Little-Endian
(least significant byte first). The level applied to the Big-Endian select (BE)
input during the LOW-to-HIGH transition of RS1 selects the endian
method that will be active during FIFO operation. BE is a don’t care input
when the bus size selected for Port B is long word. The endian method
is implemented at the completion of Reset, by the time the Full/Input
Ready flag is set HIGH, as shown in Figure 2.

Only 36-bit long word data is written to or read from the FIFO
memory on the IDT72V3623/72V3643. Bus-matching operations are
done after data is read from the FIFO RAM. These bus-matching
operations are not available when transferring data via mailbox registers.
Furthermore, both the word- and byte-size bus selections limit the width
of the data bus that can be used for mail register operations. In this case,
only those byte lanes belonging to the selected word- or byte-size bus can
carry mailbox data. The remaining data outputs will be indeterminate.
The remaining data inputs will be don’t care inputs. For example, when
a word-size bus is selected, then mailbox data can be transmitted only
between A0-A17 and B0-B17. When a byte-size bus is selected, then
mailbox data can be transmitted only between A0-A8 and B0-B8. (See
Figures 17 and 18).

BUS-MATCHING FIFO READS

Data is read from the FIFO RAM in 36-bit long word increments. If
a long word bus size is implemented, the entire long word immediately
shifts to the FIFO output register. If byte or word size is implemented on
Port B, only the first one or two bytes appear on the selected portion of the
FIFO output register, with the rest of the long word stored in auxiliary
registers. In this case, subsequent FIFO reads output the rest of the long
word to the FIFO output register in the order shown by Figure 2.

When reading data from FIFO in byte or word format, the unused B0-B35
outputs are indeterminate.
Figure 2. Bus sizing
NOTES:
1. PRS must be HIGH during Reset.
2. If BE/FWFT is HIGH, then EF/OR will go LOW one CLKB cycle earlier than in this case where BE/FWFT is LOW.

Figure 3. Reset and Loading X and Y with a Preset Value of Eight (IDT Standard and FWFT Modes)

NOTES:
1. RST must be HIGH during Partial Reset.
2. If BE/FWFT is HIGH, then EF/OR will go LOW one CLKB cycle earlier than in this case where BE/FWFT is LOW.

Figure 4. Partial Reset (IDT Standard and FWFT Modes)
NOTE:
1. \( \text{CSA} = \text{LOW}, \ W/\text{RA} = \text{HIGH}, \ \text{MBA} = \text{LOW}. \)

**Figure 5. Parallel Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)**

NOTES:
1. It is not necessary to program offset register bits on consecutive clock cycles. FIFO write attempts are ignored until \( \text{FF}/\text{IR} \) is set HIGH.
2. Programmable offsets are written serially to the SD input in the order \( \text{AF} \) offset (\( Y \)) and \( \text{AE} \) offset (\( X \)).

**Figure 6. Serial Programming of the Almost-Full Flag and Almost-Empty Flag Offset Values after Reset (IDT Standard and FWFT Modes)**

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NOTE:
1. Written to FIFO.

Figure 7. Port A Write Cycle Timing for FIFO (IDT Standard and FWFT Modes)

DATA SIZE TABLE FOR FIFO LONG-WORD READS

<table>
<thead>
<tr>
<th>SIZE MODE (1) (SELECT AT RESET)</th>
<th>DATA WRITTEN TO FIFO</th>
<th>DATA READ FROM FIFO</th>
</tr>
</thead>
<tbody>
<tr>
<td>BM SIZE BE A35-A27 A26-A18 A17-A9 A8-A0 B35-B27 B26-B18 B17-B9 B8-B0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L X X A B C D A B C D</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE:
1. BE is selected at Reset. BM and SIZE must be static throughout device operation.

Figure 8. Port B Long-Word Read Cycle (IDT Standard and FWFT Modes)
DATA SIZE TABLE FOR WORD READS

<table>
<thead>
<tr>
<th>SIZE MODE (i)</th>
<th>DATA WRITTEN TO FIFO 1</th>
<th>READ NO.</th>
<th>DATA READ FROM FIFO</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BM SIZE BE A35-A27 A26-A18 A17-A9 A8-A0</td>
<td></td>
<td>B17-B9 B8-B0</td>
</tr>
<tr>
<td>H L H</td>
<td>A B C D</td>
<td>1</td>
<td>A B</td>
</tr>
<tr>
<td>H L L</td>
<td>A B C D</td>
<td>1</td>
<td>C D</td>
</tr>
</tbody>
</table>

NOTE:
1. BE is selected at Reset: BM and SIZE must be static throughout device operation.

Figure 9. Port B Word Read Cycle Timing (IDT Standard and FWFT Modes)
### DATA SIZE TABLE FOR BYTE READS

<table>
<thead>
<tr>
<th>SIZE MODE(1)</th>
<th>DATA WRITTEN TO FIFO</th>
<th>READ NO.</th>
<th>DATA READ FROM FIFO</th>
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</thead>
<tbody>
<tr>
<td>BE BM SIZE</td>
<td>A35-A27 A26-A18 A17-A9 A8-A0</td>
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<td>B8-B0</td>
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<tr>
<td>H H H</td>
<td>A B C D</td>
<td>1</td>
<td>A</td>
</tr>
<tr>
<td>H H L</td>
<td>A B C D</td>
<td>2 3 4</td>
<td>B C D</td>
</tr>
<tr>
<td>H H L</td>
<td>A B C D</td>
<td>1 2 3 4</td>
<td>D C B A</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Unused bytes B9-B17, B18-B26, and B27-B35 are indeterminate.

---

**Figure 10. Port B Byte Read Cycle Timing (IDT Standard and FWFT Modes)**

---

1. BE is selected at Reset: BM and SIZE must be static throughout device operation.
NOTES:
1. $t_{SKEW1}$ is the minimum time between a rising CLKA edge and a rising CLKB edge for OR to transition HIGH and to clock the next word to the FIFO output register in three CLKB cycles. If the time between the rising CLKA edge and rising CLKB edge is less than $t_{SKEW1}$, then the transition of OR HIGH and load of the first word to the output register may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, OR is set LOW by the last word or byte read from the FIFO, respectively.

*Figure 11. OR Flag Timing and First Data Word Fall Through when FIFO is Empty (FWFT Mode)*
Figure 12. EF Flag Timing and First Data Read when FIFO is Empty (IDT Standard Mode)

NOTES:
1. \( t_{sKEW1} \) is the minimum time between a rising CLKA edge and a rising CLKB edge for \( EF \) to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than \( t_{sKEW1} \), then the transition of \( EF \) HIGH may occur one CLKB cycle later than shown.
2. If Port B size is word or byte, \( EF \) is set LOW by the last word or byte read from the FIFO, respectively.
NOTES:
1. \( t_{SKEW1} \) is the minimum time between a rising CLKB edge and a rising CLKA edge for IR to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than \( t_{SKEW1} \), then IR may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, \( t_{SKEW1} \) is referenced to the rising CLKB edge that reads the last word or byte write of the long word, respectively.

*Figure 13. IR Flag Timing and First Available Write when FIFO is Full (FWFT Mode)*
NOTES:
1. tSKEW1 is the minimum time between a rising CLKB edge and a rising CLKA edge for FF to transition HIGH in the next CLKA cycle. If the time between the rising CLKB edge and rising CLKA edge is less than tSKEW1, then FF may transition HIGH one CLKA cycle later than shown.
2. If Port B size is word or byte, tSKEW1 is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.

Figure 14. FF Flag Timing and First Available Write when FIFO is Full (IDT Standard Mode)

NOTES:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for AE to transition HIGH in the next CLKB cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then AE may transition HIGH one CLKB cycle later than shown.
2. FIFO Write (CSA = LOW, W/RA = LOW, MBA = LOW), FIFO read (CSB = LOW, W/RB = HIGH, MBB = LOW). Data in the FIFO output register has been read from the FIFO.
3. If Port B size is word or byte, AE is set LOW by the last word or byte read from the FIFO, respectively.

Figure 15. Timing for AE when the FIFO is Almost-Empty (IDT Standard and FWFT Modes).
COMMERCIAL TEMPERATURE RANGE

Figure 17. Timing for Mail1 Register and MBF1 Flag (IDT Standard and FWFT Modes)

NOTE:
1. If Port B is configured for word size, data can be written to the Mail1 Register using A0-A17 (A18-A35 are don’t care inputs). In this first case B0-B17 will have valid data (B18-B35 will be indeterminate). If Port B is configured for byte size, data can be written to the Mail1 Register using A0-A8 (A9-A35 are don’t care inputs). In this second case, B0-B8 will have valid data (B9-B35 will be indeterminate).

Figure 16. Timing for AF when the FIFO is Almost-Full (IDT Standard and FWFT Modes)

NOTE:
1. tSKEW2 is the minimum time between a rising CLKA edge and a rising CLKB edge for AF to transition HIGH in the next CLKA cycle. If the time between the rising CLKA edge and rising CLKB edge is less than tSKEW2, then AF may transition HIGH one CLKA cycle later than shown.
2. FIFO Write (CSA = LOW, W/RA = HIGH, MBA = LOW), FIFO read (CSB = LOW, W/RB = HIGH, MBB = LOW). Data in the FIFO output register has been read from the FIFO.
3. D = Maximum FIFO Depth = 256 for the IDT72V3623, 1,024 for the IDT72V3643.
4. If Port B size is word or byte, tSKEW2 is referenced from the rising CLKB edge that reads the last word or byte of the long word, respectively.
NOTE:
1. If Port B is configured for word size, data can be written to the Mail2 Register using B0-B17 (B18-B35 are don't care inputs). In this first case A0-A17 will have valid data (A18-A35 will be indeterminate).

If Port B is configured for byte size, data can be written to the Mail2 Register using B0-B8 (B9-B35 are don't care inputs). In this second case, A0-A8 will have valid data (A9-A35 will be indeterminate).

Figure 18. Timing for Mail2 Register and MBF2 Flag (IDT Standard and FWFT Modes)

NOTES:
1. Mailbox feature is not supported in depth expansion applications. (MBA + MBM tie to GND)
2. Transfer clock should be set either to the Write Port Clock (CLKA) or the Read Port Clock (CLKB), whichever is faster.
3. The amount of time it takes for EF/IR of the first FIFO in the chain to go HIGH (i.e. valid data to appear on the last FIFO’s outputs) after a word has been written to the first FIFO is the sum of the delays for each individual FIFO: \( (N - 1) \times (4\times\text{transfer clock}) + 3 \times T_{\text{RCLK}} \), where \( N \) is the number of FIFOs in the expansion and \( T_{\text{RCLK}} \) is the CLKB period.
4. The amount of time it takes for FF/IR of the first FIFO in the chain to go HIGH after a word has been read from the last FIFO is the sum of the delays for each individual FIFO: \( (N - 1) \times (3\times\text{transfer clock}) + 2 \times T_{\text{WCLK}} \), where \( N \) is the number of FIFOs in the expansion and \( T_{\text{WCLK}} \) is the CLKA period.

Figure 19. Block Diagram of 256 x 36, 1,024 x 36 Synchronous FIFO Memory with Programmable Flags used in Depth Expansion Configuration
PARAMETER MEASUREMENT INFORMATION

NOTE:
1. Includes probe and jig capacitance.

Figure 20. Load Circuit and Voltage Waveforms.
### ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Device Type</th>
<th>Power</th>
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<th>Process/ Temperature Range</th>
<th>Notes</th>
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### NOTES:
1. Industrial temperature range is available by special order.
2. Green parts available. For specific speeds and packages contact your sales office.
3. LEAD FINISH (SnPb) parts are in EOL process. Product Discontinuation Notice - PDN# SP-17-02

Last time buy expires June 15, 2018.

03/22/2018 Product Discontinuation Notice - PDN# SP-17-02
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