FEATURES:

- The IDT72V801 is equivalent to two IDT72V201 256 x 9 FIFOs
- The IDT72V811 is equivalent to two IDT72V211 512 x 9 FIFOs
- The IDT72V821 is equivalent to two IDT72V221 1,024 x 9 FIFOs
- The IDT72V831 is equivalent to two IDT72V231 2,048 x 9 FIFOs
- The IDT72V841 is equivalent to two IDT72V241 4,096 x 9 FIFOs
- The IDT72V851 is equivalent to two IDT72V251 8,192 x 9 FIFOs
- Offers optimal combination of large capacity, high speed, design flexibility and small footprint
- Ideal for prioritization, bidirectional, and width expansion applications
- 10 ns read/write cycle time
- 5V input tolerant
- Separate control lines and data lines for each FIFO
- Separate Empty, Full, programmable Almost-Empty and Almost-Full flags for each FIFO
- Enable puts output data lines in high-impedance state
- Space-saving 64-pin plastic Thin Quad Flat Pack (TQFP/STQFP)
- Industrial temperature range (–40°C to +85°C) is available
- Green parts available, see ordering information

DESCRIPTION:

The IDT72V801/72V811/72V821/72V831/72V841/72V851/72V851 are dual synchronous (clocked) FIFOs. The device is functionally equivalent to two IDT72V201/72V211/72V221/72V231/72V241/72V251 FIFOs in a single package with all associated control, data, and flag lines assigned to separate pins.

FUNCTIONAL BLOCK DIAGRAM

Each of the two FIFOs (designated FIFO A and FIFO B) contained in the IDT72V801/72V811/72V821/72V831/72V841/72V851 has a 9-bit input data port (DA0 - DA8, DB0 - DB8) and a 9-bit output data port (QA0 - QA8, QB0 - QB8). Each input port is controlled by a free-running clock (WCLKA, WCLKB), and two Write Enable pins (WENA1, WENA2, WENB1, WENB2). Data is written into each of the two arrays on every rising clock edge of the Write Clock (WCLKA, WCLKB) when the appropriate Write Enable pins are asserted.

The output port of each FIFO bank is controlled by its associated clock pin (RCLKA, RCLKB) and two Read Enable pins (RENA1, RENA2, RENB1, RENB2). The Read Clock can be tied to the Write Clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An Output Enable pin (OEÄ, OEB) is provided on the read port of each FIFO for three-state output control.

Each of the two FIFOs has two fixed flags, Empty (EFA, EFB) and Full (FFA, FFB). Two programmable flags, Almost-Empty (PAEA, PAEB) and Almost-Full (PAFA, PAFB), are provided for each FIFO bank to improve memory utilization. If not programmed, the programmable flags default to Empty+7 for PAEA and PAFB, and Full-7 for PAFÄ and PAFB.

The IDT72V801/72V811/72V821/72V831/72V841/72V851 architecture lends itself to many flexible configurations such as:

- 2-level priority data buffering
- Bidirectional operation
- Width expansion
- Depth expansion

This FIFO is fabricated using IDT's high-performance submicron CMOS technology.

IDT and the IDT logo are registered trademarks of Integrated Device Technology, Inc. The TeraSync FIFO is a trademark of Integrated Device Technology, Inc.
PIN CONFIGURATION

TQFP (PN64, order code: PF)
STQFP (PP64, order code: TF)
TOP VIEW
PIN DESCRIPTIONS

The IDT72V801/72V811/72V821/72V831/72V841/72V851’s two FIFOs, referred to as FIFO A and FIFO B, are identical in every respect. The following description defines the input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0-D8</td>
<td>A Data Inputs</td>
<td>I</td>
<td>9-bit data inputs to RAM array A.</td>
</tr>
<tr>
<td>B0-B8</td>
<td>B Data Inputs</td>
<td>I</td>
<td>9-bit data inputs to RAM array B.</td>
</tr>
<tr>
<td>RSA, RSB</td>
<td>Reset</td>
<td>I</td>
<td>When RSA (RSB) is set LOW, the associated internal read and write pointers of array A (B) are set to the first location; FFA (FFB) and PAF (PAFB) go HIGH, and PAEA (PAEB) and EFA (EFB) go LOW. After power-up, a reset of both FIFOs A and B is required before an initial WRITE.</td>
</tr>
<tr>
<td>WCLKA, WCLKB</td>
<td>Write Clock</td>
<td>I</td>
<td>Data is written into the FIFO A (B) on a LOW-TO-HIGH transition of WCLKA (WCLKB) when the write enable(s) are asserted.</td>
</tr>
<tr>
<td>WENAT, WENBT</td>
<td>Write Enable 1</td>
<td>I</td>
<td>If FIFO A (B) is configured to have programmable flags, WENAT (WENBT) is the only write enable pin that can be used. When WENAT (WENBT) is LOW, data A (B) is written into the FIFO on every LOW-TO-HIGH transition WCLKA (WCLKB). If the FIFO is configured to have two write enables, WENAT (WENBT) must be LOW and WENA1 (WENB1) must be HIGH to write data into the FIFO. Data will not be written into the FIFO if FFA (FFB) is LOW.</td>
</tr>
<tr>
<td>WENA2/LDA, WENB2/LDB</td>
<td>Write Enable 2/Load</td>
<td>I</td>
<td>FIFO A (B) is configured at reset to have either two write enable or programmable flags. If LDA (LDB) is HIGH at reset, this pin operates as a second Write Enable. If WENA2/LDA (WENB2/LDB) is LOW at reset this pin operates as a control to load and read the programmable flag offsets for its respective array. If the FIFO is configured to have two write enables, WENAT (WENBT) must be LOW and WENA2 (WENB2) must be HIGH to write data into the FIFO A (B). Data will not be written into FIFO A (B) if FFA (FFB) is LOW. If the FIFO is configured to have programmable flags, LDA (LDB) is held LOW to write or read the programmable flag offsets.</td>
</tr>
<tr>
<td>QA0-QA8</td>
<td>A Data Outputs</td>
<td>O</td>
<td>9-bit data outputs from RAM array A.</td>
</tr>
<tr>
<td>QB0-QB8</td>
<td>B Data Outputs</td>
<td>O</td>
<td>9-bit data outputs from RAM array B.</td>
</tr>
<tr>
<td>RCLKA, RCLKB</td>
<td>Read Clock</td>
<td>I</td>
<td>Data is read from FIFO A (B) on a LOW-TO-HIGH transition of RCLKA (RCLKB) when RENA1 (RENB1) and RENA2 (RENB2) are asserted.</td>
</tr>
<tr>
<td>RENAT, RENBT</td>
<td>ReadEnable 1</td>
<td>I</td>
<td>When RENAT (RENB1) and RENA2 (RENB2) are LOW, data is read from FIFO A (B) on every LOW-TO-HIGH transition of RCLKA (RCLKB). Data will not be read from array A (B) if EFA (EFB) is LOW.</td>
</tr>
<tr>
<td>RENA2, RENB2</td>
<td>ReadEnable 2</td>
<td>I</td>
<td>When RENAT (RENB1) and RENA2 (RENB2) are LOW, data is read from the FIFO A (B) on every LOW-TO-HIGH transition of RCLKA (RCLKB). Data will not be read from array A (B) if the EFA (EFB) is LOW.</td>
</tr>
<tr>
<td>OEA</td>
<td>Output Enable</td>
<td>I</td>
<td>When OEA (OEB) is LOW, outputs DA0-DA8 (DB0-DB8) are active. If OEA (OEB) is HIGH, the OEB outputs DA0-DA8 (DB0-DB8) will be in a high-impedance state.</td>
</tr>
<tr>
<td>EFA, EFB</td>
<td>Empty Flag</td>
<td>O</td>
<td>When EFA (EFB) is LOW, FIFO A (B) is empty and further data reads from the output are inhibited. When EFA (EFB) is HIGH, FIFO A (B) is not empty. EFA (EFB) is synchronized to RCLKA (RCLKB).</td>
</tr>
<tr>
<td>PAEA, PAEB</td>
<td>Programmable Almost-Empty Flag</td>
<td>O</td>
<td>When PAEA (PAEB) is LOW, FIFO A (B) is Almost-Empty based on the offset programmed into the appropriate offset register. The default offset at reset is Empty+7. PAEA (PAEB) is synchronized to RCLKA (RCLKB).</td>
</tr>
<tr>
<td>PAFA, PAFB</td>
<td>Programmable Almost-Full Flag</td>
<td>O</td>
<td>When PAFA (PAFB) is LOW, FIFO A (B) is Almost-Full based on the offset programmed into the appropriate offset register. The default offset at reset is Full+7. PAFA (PAFB) is synchronized to WCLKA (WCLKB).</td>
</tr>
<tr>
<td>FFA, FFB</td>
<td>Full Flag</td>
<td>O</td>
<td>When FFA (FFB) is LOW, FIFO A (B) is full and further data writings into the input are inhibited. When FFA (FFB) is HIGH, FIFO A (B) is not full. FFA (FFB) is synchronized to WCLKA (WCLKB).</td>
</tr>
<tr>
<td>VCC</td>
<td>Power</td>
<td>+3.3V</td>
<td>Power supply pin.</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>0V</td>
<td>Ground pin.</td>
</tr>
</tbody>
</table>
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VTERM</td>
<td>Terminal Voltage with Respect to GND</td>
<td>–0.5</td>
<td>+5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage Temperature</td>
<td>–55</td>
<td>+125</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>IOUT</td>
<td>DC Output Current</td>
<td>–50</td>
<td>+50</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
<td>Supply Voltage (Com’l &amp; Ind’)</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>GND</td>
<td>Supply Voltage (Com’l &amp; Ind’)</td>
<td>0</td>
<td>0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VIH</td>
<td>Input High Voltage (Com’l &amp; Ind’)</td>
<td>2.0</td>
<td></td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage (Com’l &amp; Ind’)</td>
<td></td>
<td></td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>TA</td>
<td>Operating Temperature</td>
<td>0</td>
<td></td>
<td>70</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Commercial</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Industrial</td>
<td>–40</td>
<td></td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

### DC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 3.3V ± 0.3V, TA = 0°C to +70°C; Industrial: Vcc = 3.3V ± 0.3V, TA = -40°C to +85°C)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>LI(2)</td>
<td>Input Leakage Current (Any Input)</td>
<td>–1</td>
<td></td>
<td>–1</td>
<td>μA</td>
</tr>
<tr>
<td>LO(3)</td>
<td>Output Leakage Current</td>
<td>–10</td>
<td></td>
<td>10</td>
<td>μA</td>
</tr>
<tr>
<td>VOH</td>
<td>Output Logic &quot;1&quot; Voltage, IOH = –2mA</td>
<td>2.4</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>VOL</td>
<td>Output Logic &quot;0&quot; Voltage, IOI = 8mA</td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ICC1(4,5,6)</td>
<td>Active Power Supply Current (both FIFOs)</td>
<td>—</td>
<td>40</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>ICC2(3,7)</td>
<td>Standby Current</td>
<td></td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES:**
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.
2. Measurements with 0.4 ≤ Vin ≤ Vcc.
3. OEA, OEB ≥ Vin, 0.4 ≤ Vout ≤ Vcc.
4. Tested with outputs disabled (IOUT = 0).
5. RCLK and WCLK toggle at 20 MHz and data inputs switch at 10 MHz.
6. Typical ICC = 20.17 + 0.48*fS + 0.02*CL*fS (in mA).
   These equations are valid under the following conditions:
   - Vcc = 3.3V, TA = 25°C, fS = WCLK frequency = RCLK frequency (in MHz, using TTL levels), data switching at fs/2, CL = capacitive load (in pF).
7. All Inputs = Vcc - 0.2V or GND + 0.2V, except RCLK and WCLK, which toggle at 20 MHz.

### CAPACITANCE (TA = +25°C, f = 1.0MHz)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN(2)</td>
<td>Input Capacitance</td>
<td>Vin = 0V</td>
<td>10</td>
<td>pF</td>
</tr>
<tr>
<td>COUT1(1,2)</td>
<td>Output Capacitance</td>
<td>Vout = 0V</td>
<td>10</td>
<td>pF</td>
</tr>
</tbody>
</table>

**NOTE:**
1. With output deselected (OEA, OEB ≥ Vin).
2. Characterized values, not currently tested.
### AC Electrical Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Commercial</th>
<th>Com’l &amp; Ind’</th>
<th>Commercial</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>IDT72V801L10</td>
<td>IDT72V801L15</td>
<td>IDT72V801L20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V811L10</td>
<td>IDT72V811L15</td>
<td>IDT72V811L20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V821L10</td>
<td>IDT72V821L15</td>
<td>IDT72V821L20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V831L10</td>
<td>IDT72V831L15</td>
<td>IDT72V831L20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V841L10</td>
<td>IDT72V841L15</td>
<td>IDT72V841L20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>IDT72V851L10</td>
<td>IDT72V851L15</td>
<td>IDT72V851L20</td>
</tr>
</tbody>
</table>

#### AC Test Conditions

**In Pulse Levels**
- GND to 3.0V
- 1.5V
- 1.5V

**Input Rise/Fall Times**
- 3ns

**Input Timing Reference Levels**
- 1.5V

**Output Reference Levels**
- 1.5V

**Output Load**
- See Figure 1

**NOTES:**
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not currently tested.

---

3.3V

330Ω

510Ω

30pF*

or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.
SIGNAL DESCRIPTIONS

FIFO A and FIFO B are identical in every respect. The following description explains the interaction of input and output signals for FIFO A. The corresponding signal names for FIFO B are provided in parentheses.

INPUTS:

Data In (DA0 – DA8, DB0 – DB8) — DA0 - DA8 are the nine data inputs for memory array A. DB0 - DB8 are the nine data inputs for memory array B.

CONTROLS:

Reset (RSA, RSB) — Reset of FIFO A (B) is accomplished whenever RSA (RSB) input is taken to a LOW state. During reset, the internal read and write pointers associated with the FIFO are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag, FFA (FFB) and Programmable Almost-Full Flag, PFA (PFB) will be reset to HIGH after tRF. The Empty Flag, FEA (EFB) and Programmable Almost-Empty Flag, PEA (PEB) will be reset to LOW after tREF. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLKA, WCLKB) — A write cycle to Array A (B) is initiated on the LOW-to-HIGH transition of WCLKA (WCLKB). Data set-up and hold times must be met with respect to the LOW-to-HIGH transition of WCLKA (WCLKB). The Full Flag, FFA (FFB) and Programmable Almost-Full Flag, PFA (PFB) are synchronized with respect to the LOW-to-HIGH transition of the Write Clock, WCLKA (WCLKB).

The Write and Read clock can be asynchronous or coincident.

Write Enable 1 (WENA1, WENB1) — If FIFO A (B) is configured for programmable flags, WENA1 (WENB1) is the only enable control pin. In this configuration, when WENA1 (WENB1) is LOW, data can be loaded into the input register of RAM Array A (B) on the LOW-to-HIGH transition of every Write Clock, WCLKA (WCLKB). Data is stored in Array A (B) sequentially and independently of any on-going read operation.

In this configuration, when WENA1 (WENB1) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enable controls, which allows for depth expansion. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, FFA (FFB) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the FFA (FFB) will go HIGH after twRF, allowing a valid write to begin. WENA1 (WENB1) is ignored when FIFO A (B) is full.

Read Clock (RCLKA, RCLKB) — Data can be read from Array A (B) on the LOW-to-HIGH transition of RCLKA (RCLKB). The Empty Flag, FEA (EFB) and Programmable Almost-Empty Flag, PEA (PEB) are synchronized with respect to the LOW-to-HIGH transition of RCLKA (RCLKB).

The Write and Read Clock can be asynchronous or coincident.

Read Enables (RENA1, RENB1, RENB2) — When both Read Enables, RENA1, RENB2 (RENB1, RENB2) are LOW, data is read from Array A (B) to the output register on the LOW-to-HIGH transition of the Read Clock, RCLKA (RCLKB).

When either of the two Read Enable, REN1, REN2 (RENB1, RENB2) associated with FIFO A (B) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from FIFO A (B), the Empty Flag, FEA (EFB) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, FEA (EFB) will go HIGH after tREF and a valid read can begin. The Read Enables, RENA1, RENB1, RENB2 are ignored when FIFO A (B) is empty.

Output Enable (OEA, OEB) — When Output Enable, OEA (OEB) is enabled (LOW), the parallel output buffers of FIFO A (B) receive data from their respective output register. When Output Enable, OEA (OEB) is disabled (HIGH), the QA (QB) output data bus is in a high-impedance state.

Write Enable 2/Load (WENA2/LDA, WENB2/LDB) — This is a dual-purpose pin. FIFO A (B) is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If WENA2/LDA (WENB2/LDB) is set HIGH at Reset, RSA = LOW (RSB = LOW), this pin operates as a second Write Enable pin.

If FIFO A (B) is configured to have two write enables, when Write Enable 1, WENA1 (WENB1) is LOW and WENA2/LDA (WENB2/LDB) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every Write Clock, WCLKA (WCLKB). Data is stored in the array sequentially and independently of any on-going read operation.

In this configuration, when WENA1 (WENB1) is HIGH and/or WENA2/LDA (WENB2/LDB) is LOW, the input register of Array A holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag, FFA (FFB) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, FFA (FFB) will go HIGH after twRF, allowing a valid write to begin. WENA1, (WENB1) and WENA2/LDA (WENB2/LDB) are ignored when the FIFO is full.

If FIFO A (B) is configured to have programmable flags when the WENA2/LDA (WENB2/LDB) is set LOW at Reset, RSA = LOW (RSB = LOW). Each FIFO

<table>
<thead>
<tr>
<th>LDA</th>
<th>WENA1</th>
<th>WCLKA</th>
<th>OPERATION ON FIFO A</th>
<th>OPERATION ON FIFO B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
<td>Empty Offset (LSB)</td>
<td>Empty Offset (MSB)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Full Offset (LSB)</td>
<td>Full Offset (MSB)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td>Write Into FIFO</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE:

1. For the purposes of this table, WENA2 and WENB2 = Vih.
2. The same selection sequence applies to reading from the registers. RENA1 and RENB2 (RENB1 and RENB2) are enabled and read is performed on the LOW-to-HIGH transition of RCLKA (RCLKB).

Figure 2. Writing to Offset Registers for FIFOs A and B
contains four 8-bit offset registers which can be loaded with data on the inputs, or read on the outputs. See Figure 3 for details of the size of the registers and the default values.

If FIFO A (B) is configured to have programmable flags, when the WENAT (WENB1) and WENAT (WENB1) are set LOW, data on the DA (DB) inputs are written into the Empty (Least Significant Bit) Offset register on the first LOW-to-HIGH transition of the WCLKA (WCLKB). Data are written into the Empty (Most Significant Bit) Offset register on the second LOW-to-HIGH transition of WCLKA (WCLKB), into the Full (Least Significant Bit) Offset register on the third transition, and into the Full (Most Significant Bit) Offset register on the fourth transition. The fifth transition of WCLKA (WCLKB) again writes to the Empty (Least Significant Bit) Offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing LDA (LDB) HIGH, FIFO A (B) is returned to normal read/write operation. When LDA (LDB) is set LOW, and WENA1 (WENB1) is LOW, the next offset register in sequence is written.

The contents of the offset registers can be read on the QA (QB) outputs when WENA2/LDA (WENB2/LDB) is set LOW and both Read Enables RENA1, RENA2 (RENB1, RENB2) are set LOW. Data can be read on the LOW-to-HIGH transition of the Read Clock RCLKA (RCLKB).

A read and write should not be performed simultaneously to the offset registers.

Figure 3. Offset Register Formats and Default Values for the A and B FIFOs
### OUTPUTS:

Full Flag (FFA, FFB) — FFA (FFB) will go LOW, inhibiting further write operations, when Array A (B) is full. If no reads are performed after reset, FFA (FFB) will go LOW after 256 writes to the IDT72V801’s FIFO A (B), 512 writes to the IDT72V811’s FIFO A (B), 1,024 writes to the IDT72V821’s FIFO A (B), 2,048 writes to the IDT72V831’s FIFO A (B), or 4,096 writes to the IDT72V841’s FIFO A (B), or 8,192 writes to the IDT72V851’s FIFO A (B).

FFA (FFB) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock WCLKA (WCLKB).

Empty Flag (EFA, EFB) — EFA (EFB) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating that Array A (B) is empty. EFA (EFB) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock RCLKA (RCLKB).

Programmable Almost–Full Flag (PAFA, PAFB) — PAFA (PAFB) will go LOW when the amount of data in Array A (B) reaches the Almost-Full condition. If no reads are performed after reset, PAFA (PAFB) will go LOW after (256-m) writes to the IDT72V801’s FIFO A (B), (512-m) writes to the IDT72V811’s FIFO A (B), (1,024-m) writes to the IDT72V821’s FIFO A (B), (2,048-m) writes to the IDT72V831’s FIFO A (B), (4,096-m) writes to the IDT72V841’s FIFO A (B), or (8,192-m) writes to the IDT72V851’s FIFO A (B). PAFA (PAFB) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock WCLKA (WCLKB). The offset “m” is defined in the Full Offset Registers.

If there is no Full offset specified, PAFA (PAFB) will go LOW at Full-7 words. PAFA (PAFB) is synchronized with respect to the LOW-to-HIGH transition of the Write Clock WCLKA (WCLKB).

Programmable Almost–Empty Flag (PAEA, PAEB) — PAEA (PAEB) will go LOW when the read pointer is “n+1” locations less than the write pointer. The offset “n” is defined in the Empty Offset Registers. If no reads are performed after reset, PAEA (PAEB) will go HIGH after “n+1” writes to FIFO A (B). If there is no Empty offset specified, PAEA (PAEB) will go LOW at Empty+7 words. PAEA (PAEB) is synchronized with respect to the LOW-to-HIGH transition of the Read Clock RCLKA (RCLKB).

Data Outputs (QA0 – QA8, QB0 – QB8) — QA0-QA8 are the nine data outputs for memory array A, QB0-QB8 are the nine data outputs for memory array B.

### TABLE 1: STATUS FLAGS FOR A AND B FIFOS

<table>
<thead>
<tr>
<th>IDT72V801</th>
<th>IDT72V811</th>
<th>IDT72V821</th>
<th>IDT72V831</th>
<th>IDT72V841</th>
<th>IDT72V851</th>
</tr>
</thead>
<tbody>
<tr>
<td>NUMBER OF WORDS IN ARRAY A</td>
<td>FFA</td>
<td>PAFA</td>
<td>PAEA</td>
<td>EFA</td>
<td>FFB</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>1 to n(1)</td>
<td>1 to n(1)</td>
<td>1 to n(1)</td>
<td>H</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>(n+1) to (256-(m+1))</td>
<td>(n+1) to (512-(m+1))</td>
<td>(n+1) to (1,024-(m+1))</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>(256-m)(2) to 255</td>
<td>(512-m)(2) to 511</td>
<td>(1,024-m)(2) to 1,023</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>256</td>
<td>512</td>
<td>1,024</td>
<td>L</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>IDT72V811</th>
<th>IDT72V821</th>
<th>IDT72V831</th>
<th>IDT72V841</th>
<th>IDT72V851</th>
</tr>
</thead>
<tbody>
<tr>
<td>NUMBER OF WORDS IN ARRAY A</td>
<td>FFA</td>
<td>PAFA</td>
<td>PAEA</td>
<td>EFA</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>1 to n(1)</td>
<td>1 to n(1)</td>
<td>1 to n(1)</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>(n+1) to (2,048-(m+1))</td>
<td>(n+1) to (4,096-(m+1))</td>
<td>(n+1) to (8,192-(m+1))</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>(2,048-m)(2) to 2,047</td>
<td>(4,096-m)(2) to 4,096</td>
<td>(8,192-m)(2) to 8,191</td>
<td>H</td>
<td>L</td>
</tr>
<tr>
<td>2,048</td>
<td>4,096</td>
<td>8,192</td>
<td>L</td>
<td>L</td>
</tr>
</tbody>
</table>

**NOTES:**
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)
NOTES:
1. Holding WENA2/LDA (WENB2/LDB) HIGH during reset will make the pin act as a second Write Enable pin. Holding WENA2/LDA (WENB2/LDB) LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, QA0 - QA8 (QB0 - QB8) will be LOW if OEA (OEB) = 0 and tri-state if OEA (OEB) = 1.
3. The clocks RCLKA, WCLKA (RCLKB, WCLKB) can be free-running during reset.

Figure 4. Reset Timing

NOTE:
1. tSKEW1 is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for FFA (FFB) to change during the current clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than tSKEW1, then FFA (FFB) may not change state until the next WCLKA (WCLKB) edge.

Figure 5. Write Cycle Timing
NOTE:

1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = tCLK + t_{SKEW1}$

2. When $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2tCLK + t_{SKEW1}$ or $tCLK + t_{SKEW1}$

The Latency Timings apply only at the Empty Boundary (EFA, EFB = LOW).

Figure 6. Read Cycle Timing

Figure 7. First Data Word Latency Timing
NOTE: 1. Only one of the two Write Enable inputs, WEN1 or WEN2, needs to go inactive to inhibit writes to the FIFO.

Figure 8. Full Flag Timing

Figure 9. Empty Flag Timing
NOTES:
1. \( m = \text{PAF} \) offset.
2. \((256-m)\) words for the IDT72V801, \((512-m)\) words for the IDT72V811, \((1,024-m)\) words for the IDT72V821, \((2,048-m)\) words for the IDT72V831, \((4,096-m)\) words for the IDT72V841, or \((8,192-m)\) words for the IDT72V851.
3. \( \text{tSKEW2} \) is the minimum time between a rising RCLKA (RCLKB) edge and a rising WCLKA (WCLKB) edge for \( \text{PAFA} \) (\( \text{PAFB} \)) to change during that clock cycle. If the time between the rising edge of RCLKA (RCLKB) and the rising edge of WCLKA (WCLKB) is less than \( \text{tSKEW2} \), then \( \text{PAFA} \) (\( \text{PAFB} \)) may not change state until the next WCLKA (WCLKB) rising edge.
4. If a write is performed on this rising edge of the Write Clock, there will be Full - (m+1) words in FIFO A (B) when \( \text{PAFA} \) (\( \text{PAFB} \)) goes LOW.

Figure 10. Programmable Full Flag Timing

NOTES:
1. \( n = \text{PAE} \) offset.
2. \( \text{tSKEW2} \) is the minimum time between a rising WCLKA (WCLKB) edge and a rising RCLKA (RCLKB) edge for \( \text{PAEA} \) (\( \text{PAEB} \)) to change during that clock cycle. If the time between the rising edge of WCLKA (WCLKB) and the rising edge of RCLKA (RCLKB) is less than \( \text{tSKEW2} \), then \( \text{PAEA} \) (\( \text{PAEB} \)) may not change state until the next RCLKA (RCLKB) rising edge.
3. If a read is performed on this rising edge of the Read Clock, there will be Empty + (n-1) words in FIFO A (B) when \( \text{PAEA} \) (\( \text{PAEB} \)) goes LOW.

Figure 11. Programmable Empty Flag Timing
Figure 12. Write Offset Register Timing

Figure 13. Read Offset Register Timing
OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION — When FIFO A (B) is in a Single Device Configuration, the Read Enable 2 REN_A2 (REN_B2) control input can be grounded (see Figure 14). In this configuration, the Write Enable 2/Load WENA2/LDA (WENB2/LDB) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

WIDTH EXPANSION CONFIGURATION — Word width may be increased simply by connecting the corresponding input control signals of FIFOs A and B. A composite flag should be created for each of the endpoint status flags EFA and EFB, also FFA and FFB. The partial status flags PEA, PAFB, PAEA and PAEB can be detected from any one device. Figure 15 demonstrates an 18-bit word width using the two FIFOs contained in one IDT72V801/72V811/72V821/72V831/72V841/72V851’s. Any word width can be attained by adding additional IDT72V801/72V811/72V821/72V831/72V841/72V851s.

When these devices are in a Width Expansion Configuration, the Read Enable 2 (RENA2 and RENB2) control inputs can be grounded (see Figure 15). In this configuration, the Write Enable 2/Load (WENA2/LDA, WENB2/LDB) pins are set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Figure 14. Block Diagram of One of the IDT72V801/72V811/72V821/72V831/72V841/72V851’s two FIFOs configured as a single device

Figure 15. Block diagram of the two FIFOs contained in one IDT72V801/72V811/72V821/72V831/72V841/72V851 configured for an 18-bit width-expansion
TWO PRIORITY DATA BUFFER CONFIGURATION

The two FIFOs contained in the IDT72V801/72V811/72V821/72V831/72V841/72V851 can be used to prioritize two different types of data shared on a system bus. When writing from the bus to the FIFO, control logic sorts the intermixed data according to type, sending one kind to FIFO A and the other kind to FIFO B. Then, at the outputs, each data type is transferred to its appropriate destination. Additional IDT72V801/72V811/72V821/72V831/72V841/72V851s permit more than two priority levels. Priority buffering is particularly useful in network applications.

BIDIRECTIONAL CONFIGURATION

The two FIFOs of the IDT72V801/72V811/72V821/72V831/72V841/72V851 can be used to buffer data flow in two directions. In the example that follows, a processor can write data to a peripheral controller via FIFO A, and, in turn, the peripheral controller can write the processor via FIFO B.
DEPTH EXPANSION — These FIFOs can be adapted to applications that require greater than 256/512/1,024/2,048/4,096/8,192 words. The existence of double enable pins on the read and write ports allow depth expansion. The Write Enable 2/Load (WENA2, WENB2) pins are used as a second write enables in a depth expansion configuration, thus the Programmable flags are set to the default values. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner.

ORDERING INFORMATION

Device Type | Power | Speed | Package | Process / Temperature Range | Tube or Tray |
---|---|---|---|---|---|
BLANK | L(1) | pf | TF(3) | Commercial (0°C to +70°C) |
BLANK | 8 | | | |
| | | | | Industrial (-40°C to +85°C) |
| | | | | Green |
| | | | | Thin Quad Flatpack (TQFP, PN64) |
| | | | | Slim Thin Plastic Quad Flatpack (STQFP, PP64) |
| | | | | Commercial Only |
| | | | | Commercial And Industrial |
| | | | | Clock Cycle Time (tCLK), speed in Nanoseconds |
| | | | | Commercial Only |
| | | | | Low Power |
| | | | | |
72V801 | 256 x 9 — 3.3 Volt DUAL SyncFIFO |
72V811 | 512 x 9 — 3.3 Volt DUAL SyncFIFO |
72V821 | 1,024 x 9 — 3.3 Volt DUAL SyncFIFO |
72V831 | 2,048 x 9 — 3.3 Volt DUAL SyncFIFO |
72V841 | 4,096 x 9 — 3.3 Volt DUAL SyncFIFO |
72V851 | 8,192 x 9 — 3.3 Volt DUAL SyncFIFO |

NOTES:
1. Industrial temperature range product for the 15ns speed grade is available as a standard device.
2. Green parts available. For specific speeds and packages contact your local sales office.
3. TF package is End of Life. Last time buy is July 28, 2015.

DATASHEET DOCUMENT HISTORY

04/24/2001 pgs. 4, 5 and 16
02/02/2006 pgs. 1 and 16.
10/22/2008 pg. 16.
11/06/2014 pgs. 1, 2 and 16.
03/15/2018 Product Discontinuation Notice - PDN# SP-17-02
Last time buy expires June 15, 2018.
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades; “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   *Standard*: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   *High Quality*: Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software itself is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) *Renesas Electronics* as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) *Renesas Electronics product(s)* means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.IDT.com/go/support

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2019 Renesas Electronics Corporation. All rights reserved.