General Description

The 813N252DI-02 device uses IDT’s fourth generation FemtoClock® NG technology for optimal high clock frequency and low phase noise performance, combined with a low power consumption and high power supply noise rejection. The 813N252DI-02 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation.

The 813N252DI-02 is a fully integrated Phase Locked loop utilizing a FemtoClock NG Digital VCXO that provides the low jitter, high frequency SONET/PDH output clock that easily meets OC-48 jitter requirements. This VCXO technology simplifies PLL design by replacing the pullable crystal requirement of analog VCXOs with a fixed 27MHz generator crystal. Jitter attenuation down to 10Hz is provided by an external loop filter. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The device requires the use of an external, inexpensive fundamental mode 27MHz crystal. The device is packaged in a space-saving 32-VFQFN package and supports industrial temperature range.

Features

• Fourth generation FemtoClock® NG technology
• Two LVPECL output pairs
• Each output supports independent frequency selection at 25MHz, 125MHz, 156.25MHz and 312.5MHz
• Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, HCSL
• Accepts input frequencies from 8kHz to 155.52MHz including 8kHz, 1.544MHz, 2.048MHz, 19.44MHz, 25MHz, 77.76MHz, 125MHz and 155.52MHz
• Crystal interface optimized for a 27MHz, 10pF parallel resonant crystal
• Attenuates the phase jitter of the input clock by using a low-cost fundamental mode crystal
• Customized settings for jitter attenuation and reference tracking using an external loop filter connection
• FemtoClock NG frequency multiplier provides low jitter, high frequency output
• Absolute pull range: ±100ppm
• Power supply noise rejection (PSNR): -85dB (typical)
• FemtoClock NG VCXO frequency: 2500MHz
• RMS phase jitter @ 156.25MHz, using a 27MHz crystal (12kHz – 20MHz): 0.6ps (typical)
• RMS phase jitter @ 125MHz, using a 27MHz crystal (12kHz – 20MHz): 0.65ps (typical)
• 3.3V supply voltage
• -40°C to 85°C ambient operating temperature
• Available in lead-free (RoHS 6) package

Pin Assignment

32-pin, 5mm x 5mm VFQFN Package
Block Diagram

**Block Diagram of a Jitter Attenuator & FemtoClock NG**

- **Phase Detector**
- **Charge Pump**
- **A/D Control Block**
- **Fractional Feedback Divider**
- **Digital VCXO**
- **27MHz Osc.**

**External Components**:
- **Pullup**
- **Pulldown**

**Signal Inputs**:
- **CLK_SEL**
- **PDSEL[2:0]**
- **CLK0**, **nCLK0**, **CLK1**, **nCLK1**

**Signal Outputs**:
- **QA**, **nQA**
- **QB**, **nQB**
- **ODASEL[1:0]**
- **ODBSEL[1:0]**

**Notes**:
- Dashed lines indicate external components.

---

**Diagram Source**: Renesas Electronics Corporation

**Revision**: 08/14/15
**Table 1. Pin Descriptions**

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2</td>
<td>LF1, LF0</td>
<td>Analog Input/Output</td>
<td>Loop filter connection node pins. LF0 is the output. LF1 is the input.</td>
</tr>
<tr>
<td>3</td>
<td>ISET</td>
<td>Analog Input/Output</td>
<td>Charge pump current setting pin.</td>
</tr>
<tr>
<td>4, 8, 18, 24</td>
<td>VEE</td>
<td>Power</td>
<td>Negative supply pins.</td>
</tr>
<tr>
<td>5</td>
<td>CLK_SEL</td>
<td>Input Pulldown</td>
<td>Input clock select. When HIGH selects CLK1, nCLK1. When LOW, selects CLK0, nCLK0. LVCMOS / LVTTL interface levels.</td>
</tr>
<tr>
<td>6, 12, 27</td>
<td>VCC</td>
<td>Power</td>
<td>Core supply pins.</td>
</tr>
<tr>
<td>7</td>
<td>RESERVED</td>
<td>Reserve</td>
<td>Reserved pin.</td>
</tr>
<tr>
<td>9, 10, 11</td>
<td>PDSEL_2, PDSEL_1, PDSEL_0</td>
<td>Input Pulldown</td>
<td>Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.</td>
</tr>
<tr>
<td>13</td>
<td>VCCA</td>
<td>Power</td>
<td>Analog supply pin.</td>
</tr>
<tr>
<td>14, 15</td>
<td>ODBSEL_1, ODBSEL_0</td>
<td>Input Pulldown</td>
<td>Frequency select pins for Bank B output. See Table 3B. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>16, 17</td>
<td>ODASEL_1, ODASEL_0</td>
<td>Input Pulldown</td>
<td>Frequency select pins for Bank A output. See Table 3B. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>19, 20</td>
<td>QA, nQA</td>
<td>Output</td>
<td>Differential Bank A clock outputs. LVPECL interface levels.</td>
</tr>
<tr>
<td>21</td>
<td>VCO</td>
<td>Power</td>
<td>Output supply pin.</td>
</tr>
<tr>
<td>22, 23</td>
<td>QB, nQB</td>
<td>Output</td>
<td>Differential Bank B clock outputs. LVPECL interface levels.</td>
</tr>
<tr>
<td>25</td>
<td>nCLK1</td>
<td>Input Pulldown/Pulldown</td>
<td>Inverting differential clock input. VCC/2 bias voltage when left floating.</td>
</tr>
<tr>
<td>26</td>
<td>CLK1</td>
<td>Input Pulldown</td>
<td>Non-inverting differential clock input.</td>
</tr>
<tr>
<td>28</td>
<td>nCLK0</td>
<td>Input Pulldown/Pulldown</td>
<td>Inverting differential clock input. VCC/2 bias voltage when left floating.</td>
</tr>
<tr>
<td>29</td>
<td>CLK0</td>
<td>Input Pulldown</td>
<td>Non-inverting differential clock input.</td>
</tr>
<tr>
<td>30, 31</td>
<td>XTAL_OUT, XTAL_IN</td>
<td>Input</td>
<td>Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.</td>
</tr>
<tr>
<td>32</td>
<td>VCCX</td>
<td>Power</td>
<td>Power supply pin for the crystal oscillator.</td>
</tr>
</tbody>
</table>

Note: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R_PULLDOWN</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>
## Function Tables

### Table 3A. Pre-Divider Selection Function Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>PDSEL_2</th>
<th>PDSEL_1</th>
<th>PDSEL_0</th>
<th>+P Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>193</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>256</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1944</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2500</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>7776</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>12500</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>15552 (default)</td>
</tr>
</tbody>
</table>

### Table 3B. Output Divider Function Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>ODxSEL_1</th>
<th>ODxSEL_0</th>
<th>+Nx Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>100 (default)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>20</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8</td>
</tr>
</tbody>
</table>

NOTE: x denotes A or B.
Table 3C. Frequency Function Table

<table>
<thead>
<tr>
<th>Input Frequency (MHz)</th>
<th>÷P Value</th>
<th>FemtoClock NG VCXO Center Frequency (MHz)</th>
<th>÷Nx Value</th>
<th>Output Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.008</td>
<td>1</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>0.008</td>
<td>1</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>0.008</td>
<td>1</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>0.008</td>
<td>1</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
<tr>
<td>1.544</td>
<td>193</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>1.544</td>
<td>193</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>1.544</td>
<td>193</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>1.544</td>
<td>193</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
<tr>
<td>2.048</td>
<td>256</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>2.048</td>
<td>256</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>2.048</td>
<td>256</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>2.048</td>
<td>256</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
<tr>
<td>19.44</td>
<td>1944</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>19.44</td>
<td>1944</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>19.44</td>
<td>1944</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>19.44</td>
<td>1944</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
<tr>
<td>25</td>
<td>2500</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>25</td>
<td>2500</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>25</td>
<td>2500</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>25</td>
<td>2500</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
<tr>
<td>77.76</td>
<td>7776</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>77.76</td>
<td>7776</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>77.76</td>
<td>7776</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>77.76</td>
<td>7776</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
<tr>
<td>125</td>
<td>12500</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>125</td>
<td>12500</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>125</td>
<td>12500</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>125</td>
<td>12500</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
<tr>
<td>155.52</td>
<td>15552</td>
<td>2500</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>155.52</td>
<td>15552</td>
<td>2500</td>
<td>20</td>
<td>125</td>
</tr>
<tr>
<td>155.52</td>
<td>15552</td>
<td>2500</td>
<td>16</td>
<td>156.25</td>
</tr>
<tr>
<td>155.52</td>
<td>15552</td>
<td>2500</td>
<td>8</td>
<td>312.5</td>
</tr>
</tbody>
</table>

NOTE: x denotes A or B.
Absolute Maximum Ratings

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, V_{CC}</td>
<td>3.63V</td>
</tr>
<tr>
<td>Inputs, V_{I}</td>
<td>0V to 2V</td>
</tr>
<tr>
<td>XTAL_IN</td>
<td>-0.5V to V_{CC} + 0.5V</td>
</tr>
<tr>
<td>Other Inputs</td>
<td></td>
</tr>
<tr>
<td>Outputs, I_{O}</td>
<td></td>
</tr>
<tr>
<td>Continuous Current</td>
<td>50mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td>100mA</td>
</tr>
<tr>
<td>Package Thermal Impedance, \theta_{JA}</td>
<td>33.1°C/W (0 mps)</td>
</tr>
<tr>
<td>Storage Temperature, T_{STG}</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics

Table 4A. LVPECL Power Supply DC Characteristics, V_{CC} = V_{CCO} = V_{CCX} = 3.3V ± 5%, V_{EE} = 0V, T_{A} = -40°C to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{CC}</td>
<td>Core Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>V_{CCA}</td>
<td>Analog Supply Voltage</td>
<td></td>
<td>V_{CC} - 0.30</td>
<td>3.3</td>
<td>V_{CC}</td>
<td>V</td>
</tr>
<tr>
<td>V_{CCO}</td>
<td>Output Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>V_{CCX}</td>
<td>Crystal Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>I_{EE}</td>
<td>Power Supply Current</td>
<td></td>
<td>253</td>
<td>321</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>I_{CCA}</td>
<td>Analog Supply Current</td>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{CC} = V_{CCO} = V_{CCX} = 3.3V ± 5%, T_{A} = -40°C to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{IH}</td>
<td>Input High Voltage</td>
<td></td>
<td>2</td>
<td>V_{CC} + 0.3</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{IL}</td>
<td>Input Low Voltage</td>
<td></td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>I_{IH}</td>
<td>Input High Current</td>
<td>CLK_SEL,</td>
<td>V_{CC} = V_{IN} = 3.465V</td>
<td>150</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ODASEL_[1:0],</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ODBSEL_[1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>PDSEL_[2:0]</td>
<td>V_{CC} = V_{IN} = 3.465V</td>
<td>10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Input Low Current</td>
<td>CLK_SEL,</td>
<td>V_{CC} = 3.465V, V_{IN} = 0V</td>
<td>-10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ODASEL_[1:0],</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ODBSEL_[1:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>PDSEL_[2:0]</td>
<td>V_{CC} = 3.465, V_{IN} = 0V</td>
<td>-150</td>
<td></td>
<td>µA</td>
</tr>
</tbody>
</table>
Table 4C. Differential DC Characteristics, \( V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%, \ T_A = -40°C \) to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{IH}</td>
<td>Input High Current</td>
<td>( \text{CLK0, nCLK0, } \text{CLK1, nCLK1} ) ( V_{CC} = V_{IN} = 3.465V )</td>
<td>150</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I_{IL}</td>
<td>Input Low Current</td>
<td>( \text{CLK0, CLK1} ) ( V_{CC} = 3.465V, \ V_{IN} = 0V )</td>
<td>-10</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>( \text{nCLK0, nCLK1} ) ( V_{CC} = 3.465V, \ V_{IN} = 0V )</td>
<td>-150</td>
<td>( \mu A )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V_{PP}</td>
<td>Peak-to-Peak Input Voltage; NOTE 1</td>
<td>( V_{EE} )</td>
<td>0.15</td>
<td></td>
<td>1.3</td>
<td>V</td>
</tr>
<tr>
<td>V_{CMR}</td>
<td>Common Mode Input Voltage; NOTE 1, 2</td>
<td>( V_{EE} )</td>
<td>( V_{CC} - 0.85 )</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1: \( V_{IL} \) should not be less than -0.3V.
NOTE 2. Common mode voltage is defined at the crosspoint.

Table 4D. LVPECL DC Characteristics, \( V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%, \ V_{EE} = 0V, \ T_A = -40°C \) to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{OH}</td>
<td>Output High Voltage; NOTE 1</td>
<td>( V_{CCO} - 1.10 )</td>
<td>( V_{CCO} - 0.75 )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{OL}</td>
<td>Output Low Voltage; NOTE 1</td>
<td>( V_{CCO} - 2.0 )</td>
<td>( V_{CCO} - 1.6 )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>V_{SWING}</td>
<td>Peak-to-Peak Output Voltage Swing</td>
<td>0.6</td>
<td>1.0</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1: Outputs terminated with 50\( \Omega \) to \( V_{CCO} - 2V \). See Parameter Measurement Information section, 3.3V Output Load Test Circuit.
**AC Electrical Characteristics**

Table 5. AC Characteristics, \( V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\% \), \( T_A = -40^\circ C \) to \( 85^\circ C \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{IN} )</td>
<td>Input Frequency</td>
<td></td>
<td>0.008</td>
<td>155.52</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( f_{OUT} )</td>
<td>Output Frequency</td>
<td></td>
<td>25</td>
<td>312.5</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( \delta(\Omega) )</td>
<td>RMS Phase Jitter, (Random), NOTE 1</td>
<td>125MHz ( f_{OUT} ), 27MHz crystal, Integration Range: 12kHz – 20MHz</td>
<td>0.65</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>156.25MHz ( f_{OUT} ), 27MHz crystal, Integration Range: 12kHz – 20MHz</td>
<td>0.6</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PSNR</td>
<td>Power Supply Noise Rejection; NOTE 2</td>
<td>( V_{PP} = 50mV ) Sine Wave, Range: 10kHz – 10MHz</td>
<td>-85</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{sk(\Omega)} )</td>
<td>Output Skew; NOTE 3, 4</td>
<td></td>
<td>80</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_R / t_F )</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>150</td>
<td>450</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( odc )</td>
<td>Output Duty Cycle</td>
<td></td>
<td>48</td>
<td>52</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( t_{LOCK} )</td>
<td>Output-to-Input Phase Lock Time; NOTE 5</td>
<td>Reference Clock Input is ( \pm 100ppm ) from Nominal Frequency</td>
<td>4</td>
<td>s</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: Characterized with outputs at the same frequency using the loop filter components for the 35Hz loop bandwidth.

Refer to Jitter Attenuator Loop Bandwidth Selection Table.

NOTE 1: Refer to the Phase Noise Plot.

NOTE 2: PSNR results achieved by injecting noise on \( V_{CCA} \) supply pin with no external filter network.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 5: Lock Time measured from power-up to stable output frequency.
Typical Phase Noise at 125MHz

![Phase Noise Plot]

- Noise Power dBc
- Offset Frequency (Hz)

-20.00
-30.00
-40.00
-50.00
-60.00
-70.00

-10
-100
1k
10k
100k
1M
10M

Carrier 124.009301 MHz, -4.27dBm

- Start: 12 kHz
- Stop: 20 MHz
- Center: 10.006 MHz
- Span: 19.988 MHz
- Analysis Range X: Band Marker
- Analysis Range Y: Band Marker
- Integ Noise: -68.8160 dBc / 19.69 MHz
- RMS Noise: 512.524 μrad
- RMS Jitter: 29.3655 ndeg
- Residual PH: 2.02713 kHz
Parameter Measurement Information

**3.3V LVPECL Output Load AC Test Circuit**

- Input to Output Phase Lock Time
- Output Skew
- Output Duty Cycle/Pulse Width/Period
- LVPECL Output Rise/Fall Time

**Differential Input Level**

- RMS Phase Jitter

**Supply Voltage**

- Vcc
- VEE
- 60% of Vcc
- Output-to-Input Phase Lock
- Not to Scale

**Output-to-Input Phase Lock Time**

- Lock Time
- Offsets

**Output Skew**

- nQx, Qx, nQy, Qy
- tsk(o)

**LVPECL Output Rise/Fall Time**

- nQA, nQB, QA, QB
- 80%
- VSWING
- 20%
- tR, tF

**RMS Phase Jitter**

- RMS Phase Jitter = \( \frac{1}{\sqrt{2} \pi} \times \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}} \)
Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage \( V_1 = V_{CC}/2 \) is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the \( V_1 \) in the center of the input voltage swing. For example, if the input clock is driven from a single-ended 2.5V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25V, the R1 and R2 values should be adjusted to set the \( V_1 \) at 1.25V. The values below are for when both the single ended swing and \( V_{CC} \) are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however \( V_{IL} \) cannot be less than -0.3V and \( V_{IH} \) cannot be more than \( V_{CC} + 0.3V \). Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

![Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels](image-url)
3.3V Differential Clock Input Interface

The CLK / nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both differential inputs must meet the \( V_{PP} \) and \( V_{CMR} \) input requirements. Figures 2A to 2E show interface examples for the CLK / nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 2A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

Figure 2B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

Figure 2C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

Figure 2D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

Figure 2E. CLK/nCLK Input Driven by an HCSL Driver
Recommendations for Unused Input and Output Pins

**Inputs:**

**CLK/nCLK Inputs**
For applications requiring only one differential input, the unused CLKx and nCLKx pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the unused CLK input to ground.

**LVCMOS Control Pins**
All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

**Outputs:**

**LVPECL Outputs**
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

**Termination for 3.3V LVPECL Outputs**
The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.*

![Figure 3A. 3.3V LVPECL Output Termination](image)

![Figure 3B. 3.3V LVPECL Output Termination](image)
Jitter Attenuator **EXTERNAL COMPONENTS**
Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the Jitter Attenuator. In choosing a crystal, special precaution must be taken with load capacitance ($C_L$), frequency accuracy and temperature range.

The crystal's $C_L$ characteristic determines its resonating frequency and is closely related to the center tuning of the crystal. The total external capacitance ($C_{EXTERNAL}$) seen by the crystal when installed on a PCB is the sum of the stray board capacitance, IC package lead capacitance, internal device capacitance and any installed tuning capacitors ($C_{TUNE}$). The recommended $C_L$ in the **Crystal Parameter Table** balances the tuning range by centering the tuning curve for a typical PCB. If the crystal $C_L$ is greater than the total external capacitance ($C_L > C_{EXTERNAL}$), the crystal will oscillate at a higher frequency than the specification. If the crystal $C_L$ is lower than the total external capacitance ($C_L < C_{EXTERNAL}$), the crystal will oscillate at a lower frequency than the specification. Mismatches between $C_L$ and $C_{EXTERNAL}$ require adjustments in $C_{TUNE}$ in order to center the tuning curve. For example, given a board with 5pF of stray capacitance, $C_{TUNE}$ would be 0. In addition, the frequency accuracy specification in the **Crystal Characteristics Table** are used to calculate the APR (Absolute Pull Range). It is recommended that the crystal $C_L$ not exceed the value stated in the **Crystal Parameter Table** because it can lead to a reduced APR.

### Crystal Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_N$</td>
<td>Frequency</td>
<td></td>
<td>27</td>
<td>±20</td>
<td>±20</td>
<td>MHz</td>
</tr>
<tr>
<td>$f_T$</td>
<td>Frequency Tolerance</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ppm</td>
</tr>
<tr>
<td>$f_S$</td>
<td>Frequency Stability</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ppm</td>
</tr>
<tr>
<td></td>
<td>Operating Temperature Range</td>
<td></td>
<td>-40</td>
<td>+85</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>$C_L$</td>
<td>Load Capacitance</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_O$</td>
<td>Shunt Capacitance</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
<td></td>
<td>40</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td>Drive Level</td>
<td></td>
<td>100</td>
<td>1</td>
<td>±3</td>
<td>μW</td>
</tr>
<tr>
<td></td>
<td>Aging @ 25 °C</td>
<td>First Year</td>
<td></td>
<td></td>
<td></td>
<td>ppm</td>
</tr>
</tbody>
</table>

The VCXO-PLL Loop Bandwidth Selection Table shows $R_S$, $C_S$, $C_P$, and $R_{SET}$ values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. In addition, the digital VCXO gain ($k_{VCXO}$) has been provided for additional loop filter requirements.

### Jitter Attenuator Characteristics Table

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Typical</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$k_{VCXO}$</td>
<td>VCXO Gain</td>
<td>2.6</td>
<td>kHz/V</td>
</tr>
</tbody>
</table>

### Jitter Attenuator Loop Bandwidth Selection Table

<table>
<thead>
<tr>
<th>Bandwidth</th>
<th>Crystal Frequency</th>
<th>$R_S$ (kΩ)</th>
<th>$C_S$ (μF)</th>
<th>$C_P$ (μF)</th>
<th>$R_{SET}$ (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7Hz (Low)</td>
<td>27MHz</td>
<td>110</td>
<td>10</td>
<td>0.01</td>
<td>2.21</td>
</tr>
<tr>
<td>35Hz (Mid)</td>
<td>27MHz</td>
<td>365</td>
<td>1</td>
<td>0.002</td>
<td>1.5</td>
</tr>
<tr>
<td>45Hz (High)</td>
<td>27MHz</td>
<td>470</td>
<td>1</td>
<td>0.0005</td>
<td>1.5</td>
</tr>
</tbody>
</table>

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.
VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 4. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mil (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad(slug) and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)
Schematic Example

*Figure 5* (on next page) shows an example of 813N252DI-02 application schematic. In this example, the device is operated at $V_{CC} = V_{CCX} = V_{CCO} = 3.3V$. A 10pF parallel resonant 27MHz crystal is used. Spare placement pads for the load capacitance C1 and C2 are recommended for frequency accuracy. Depending on the parasitics of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will required adjusting C1 and C2.

An Optional 3-pole filter can also be used for additional spur reduction. It is recommended that the loop filter components be laid out for the 3-pole option. This will allow the flexibility for the 2-pole filter to be used.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The 813N252DI-02 provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set.
JITTER ATTENUATOR & FEMTOCLOCK NG® MULTIPLIER

© 2019 Renesas Electronics Corporation

Figure 5. 813N252DI-02 Schematic Example
Power Considerations

This section provides information on power dissipation and junction temperature for the 813N252DI-02. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 813N252DI-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CCO} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{\text{MAX}} = V_{CCO,\text{MAX}} * I_{EE,\text{MAX}} = 3.465V \times 321mA = 1112.3mW$
- Power (outputs)$_{\text{MAX}} = 31.55mW/\text{Loaded Output pair}$
  If all outputs are loaded, the total power is $2 \times 31.55mW = 63.1mW$

**Total Power$_{\text{MAX}}$ (3.465V, with all outputs switching) = 1112.3mW + 63.1mW = 1175.4mW**

2. Junction Temperature.

Junction temperature, $T_j$, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, $T_j$, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for $T_j$ is as follows: $T_j = \theta_{JA} \times P_{d_{total}} + T_A$

- $T_j =$ Junction Temperature
- $\theta_{JA} =$ Junction-to-Ambient Thermal Resistance
- $P_{d_{total}} =$ Total Device Power Dissipation (example calculation is in section 1 above)
- $T_A =$ Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming no air flow and a multi-layer board, the appropriate value is 33.1°C/W per Table 6 below.

Therefore, $T_j$ for an ambient temperature of 85°C with all outputs switching is:

$85°C + 1.175W \times 33.1°C/W = 123.9°C$. This is below the limit of 125°C.

This calculation is only an example. $T_j$ will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance $\theta_{JA}$ for 32 Lead VFQFN, Forced Convection

<table>
<thead>
<tr>
<th>$\theta_{JA}$ by Velocity</th>
<th>0</th>
<th>1</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meters per Second</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>33.1°C/W</td>
<td>28.1°C/W</td>
<td>25.4°C/W</td>
</tr>
</tbody>
</table>
3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair. LVPECL output driver circuit and termination are shown in Figure 6.

![LVPECL Driver Circuit and Termination](image)

Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V\text{CCO} - 2V.

- For logic high, V\text{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.75V
  \[ (V_{CC\_MAX} - V_{OH\_MAX}) = 0.75V \]
- For logic low, V\text{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.6V
  \[ (V_{CC\_MAX} - V_{OL\_MAX}) = 1.6V \]

Pd\_H is the power dissipation when the output drives high.

Pd\_L is the power dissipation when the output drives low.

\[
Pd\_H = \left( \frac{(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L}{(V_{CC\_MAX} - V_{OH\_MAX})} \right) \cdot (V_{CCO\_MAX} - V_{OH\_MAX}) = \left( \frac{(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))}{50\Omega} \right) \cdot 0.75V = 18.75mW
\]

\[
Pd\_L = \left( \frac{(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L}{(V_{CC\_MAX} - V_{OL\_MAX})} \right) \cdot (V_{CCO\_MAX} - V_{OL\_MAX}) = \left( \frac{(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))}{50\Omega} \right) \cdot 1.6V = 12.80mW
\]

Total Power Dissipation per output pair = Pd\_H + Pd\_L = 31.55mW
Reliability Information

Table 7. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>0</th>
<th>1</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>33.1°C/W</td>
<td>28.1°C/W</td>
<td>25.4°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for 813N252DI-02 is: 45,491
Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN

Table 8. Package Dimensions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Minimum</th>
<th>Nominal</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>N 32</td>
<td>0.80</td>
<td>1.00</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>0.05</td>
<td></td>
<td>0.18</td>
</tr>
<tr>
<td>A1</td>
<td>0</td>
<td></td>
<td>0.25</td>
</tr>
<tr>
<td>A3</td>
<td>0.25 Ref.</td>
<td>0.50</td>
<td></td>
</tr>
<tr>
<td>b</td>
<td>0.18</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>e</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>N &amp; N</td>
<td>0.18</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>D &amp; E</td>
<td>5.00 Basic</td>
<td>3.0</td>
<td>3.3</td>
</tr>
<tr>
<td>e</td>
<td>0.50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.30</td>
<td>0.40</td>
<td>0.50</td>
</tr>
</tbody>
</table>

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pin-out are shown on the front page. The package dimensions are in Table 8.

Reference Document: JEDEC Publication 95, MO-220
### Ordering Information

**Table 9. Ordering Information**

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>813N252DKI-02LF</td>
<td>ICSN52DI02L</td>
<td>32 Lead VFQFN, Lead-Free</td>
<td>Tray</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>813N252DKI-02LFT</td>
<td>ICSN52DI02L</td>
<td>32 Lead VFQFN, Lead-Free</td>
<td>Tape &amp; Reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   *Standard*: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   *High Quality*: Transportation equipment (railways, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations applicable to the products administered by the governments of any countries asserting jurisdiction over the parties or transactions.

10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.

11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters
TOYOSU FORESIA, 3-2-24 Toyo-su,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information
For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks
Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2020 Renesas Electronics Corporation. All rights reserved.