

GENERAL DESCRIPTION

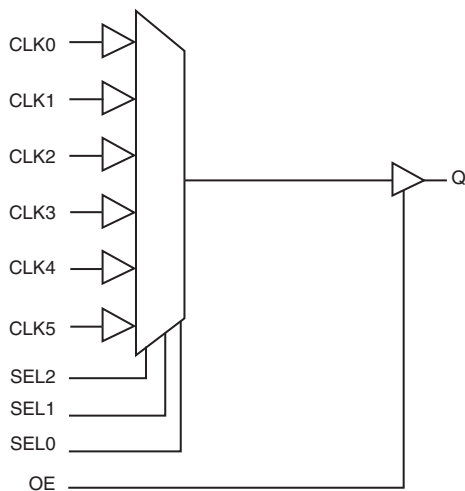
The 83056 is a low skew, 6:1, Single-ended Multiplexer from IDT. The 83056 has six selectable single-ended clock inputs and one single-ended clock output. The output has a V_{DDO} pin which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug purposes. The device operates up to 250MHz and is packaged in a 16 TSSOP package.

FEATURES

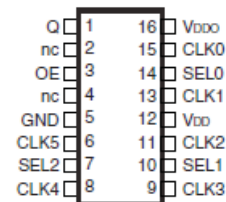
- 6:1 single-ended multiplexer
- Q nominal output impedance: 7Ω ($V_{DDO} = 3.3V$)
- Maximum output frequency: 250MHz
- Propagation delay: 3ns (maximum), $V_{DD} = V_{DDO} = 3.3V$
- Input skew: 225ps (maximum), $V_{DD} = V_{DDO} = 3.3V$
- Part-to-part skew: 475ps (maximum), $V_{DD} = V_{DDO} = 3.3V$
- Additive phase jitter, RMS: 0.19ps (typical), 3.3V/3.3V
- Operating supply modes:

V_{DD}/V_{DDO}
3.3V/3.3V
3.3V/2.5V
3.3V/1.8V
2.5V/2.5V
2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

BLOCK DIAGRAM



PIN ASSIGNMENT



83056

16-Lead TSSOP

4.4mm x 5.0mm x 0.92mm package body

G Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
2, 4	nc	Unused		No connect.
6, 8, 9, 11, 13, 15	CLK5, CLK4, CLK3, CLK2, CLK1, CLK0	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
3	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
5	GND	Power		Power supply ground.
7, 10, 14	SEL2, SEL1, SEL0	Input	Pulldown	Clock select input. See Control Input Function Table. LVCMOS / LVTTL interface levels.
12	V _{DD}	Power		Core and input supply pin.
16	V _{DDO}	Power		Output supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
C _{PD}	Power Dissipation Capacitance (per output)	V = 3.465V		18		pF
		V = 2.625V		20		pF
		V = 1.89V		30		pF
R _{OUT}	Output Impedance	V = 3.465V		7		Ω
		V = 2.625V		7		Ω
		V = 1.89V		10		Ω

TABLE 3. CONTROL INPUT FUNCTION TABLE

Control Inputs			Input Selected to Q
SEL2	SEL1	SEL0	
0	0	0	CLK0
0	0	1	CLK1
0	1	0	CLK2
0	1	1	CLK3
1	0	0	CLK4
1	0	1	CLK5
1	1	0	LOW
1	1	1	LOW

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.71	1.8	1.89	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				35	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 4E. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		1.71	1.8	1.89	V
I_{DD}	Power Supply Current				35	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 4F. LVCMOS/LVTTL DC CHARACTERISTICS, $T_A = -40^{\circ}\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.3\text{V} \pm 5\%$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5\text{V} \pm 5\%$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.3\text{V} \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5\text{V} \pm 5\%$	-0.3		0.7	V
I_{IH}	Input High Current	CLK0:CLK5, SEL0:SEL2 $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$			150	μA
		OE $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$			5	μA
I_{IL}	Input Low Current	CLK0:CLK5, SEL0:SEL2 $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$	-5			μA
		OE $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$	-150			μA
V_{OH}	Output High Voltage	$V_{DDO} = 3.3\text{V} \pm 5\%$; NOTE 1	2.6			V
		$V_{DDO} = 2.5\text{V} \pm 5\%$; NOTE 1	1.8			V
		$V_{DDO} = 1.8\text{V} \pm 5\%$; NOTE 1	$V_{DD} - 0.3$			V
V_{OL}	Output Low Voltage	$V_{DDO} = 3.3\text{V} \pm 5\%$; NOTE 1			0.5	V
		$V_{DDO} = 2.5\text{V} \pm 5\%$; NOTE 1			0.45	V
		$V_{DDO} = 1.8\text{V} \pm 5\%$; NOTE 1			0.35	V

NOTE 1: Outputs terminated with 50 Ω to $V_{DDO}/2$. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 3.3\text{V} \pm 5\%$, $T_A = -40^{\circ}\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{pLH}	Propagation Delay, Low to High; NOTE 1		2.4	2.7	3.0	ns
t_{pHL}	Propagation Delay, High to Low; NOTE 1		2.5	2.7	2.9	ns
$t_{sk(i)}$	Input Skew; NOTE 2			55	225	ps
t_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.19		ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 4				475	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		500	ps
odc	Output Duty Cycle		45		55	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Driving only one input clock.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.5	2.8	3.1	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.6	2.8	3.0	ns
$tsk(i)$	Input Skew; NOTE 2			45	150	ps
τ_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.14		ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				400	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	50		500	ps
odc	Output Duty Cycle		45		55	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Driving only one input clock.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 5\%$, $T_A = -40^\circ\text{C}$ TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.7	3.2	3.8	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.8	3.3	3.8	ns
$tsk(i)$	Input Skew; NOTE 2			50	150	ps
τ_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.16		ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				475	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		700	ps
odc	Output Duty Cycle		45		55	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Driving only one input clock.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.5	3.0	3.5	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.5	2.9	3.4	ns
$tsk(i)$	Input Skew; NOTE 2			60	175	ps
$tjit$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.21		ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				300	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		500	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Driving only one input clock.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

TABLE 5E. AC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm -5\%$, $T_A = -40^{\circ}C$ TO $85^{\circ}C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.6	3.3	4.0	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.7	3.3	4.0	ns
$tsk(i)$	Input Skew; NOTE 2			50	150	ps
$tjit$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 3	155.52MHz, (12kHz to 20MHz)		0.17		ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				325	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		700	ps
odc	Output Duty Cycle		40		60	%
MUX_{ISOL}	MUX Isolation	@ 100MHz		45		dB

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DDO}/2$ of the output.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

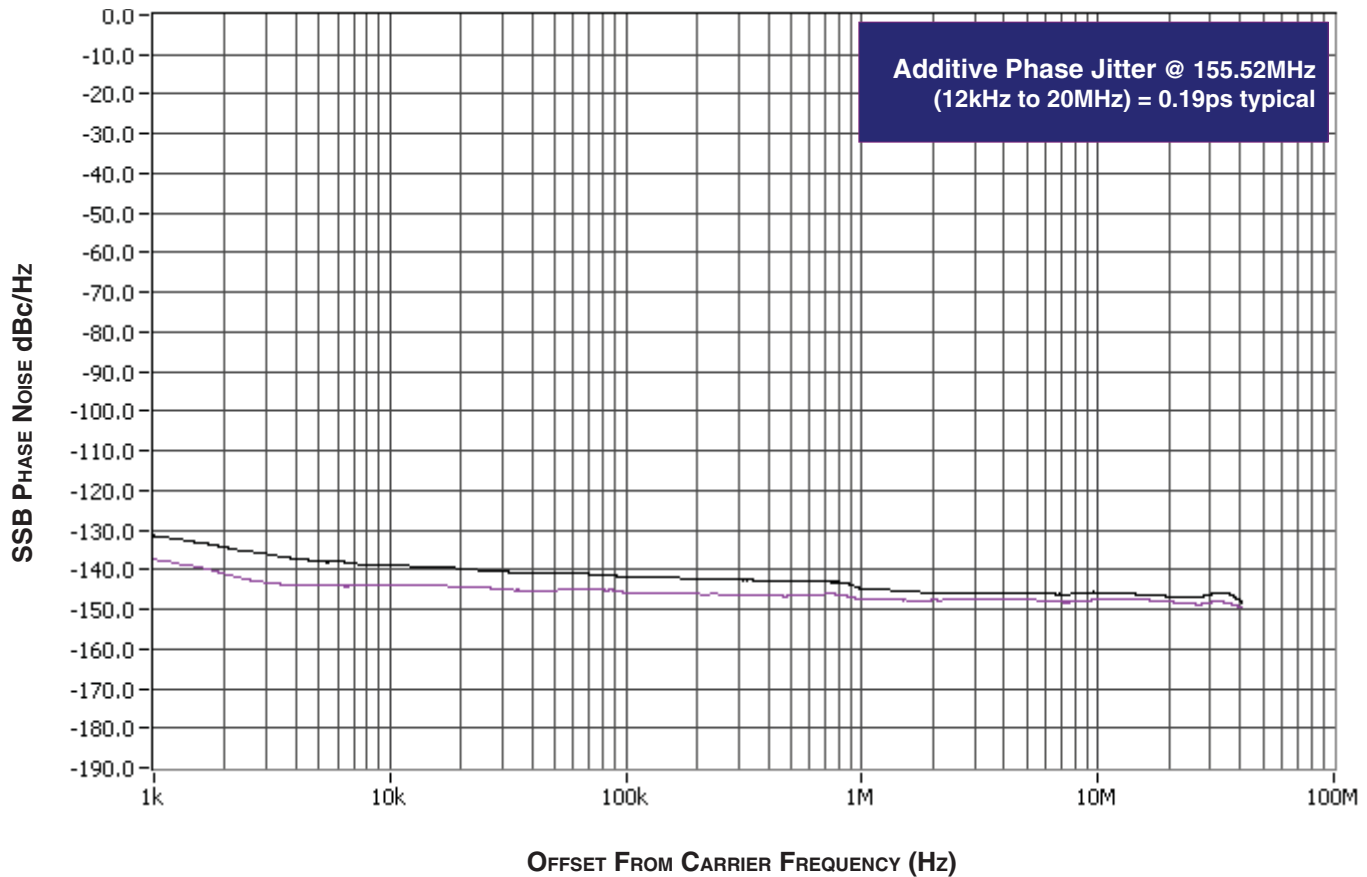
NOTE 3: Driving only one input clock.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at $V_{DDO}/2$.

ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the

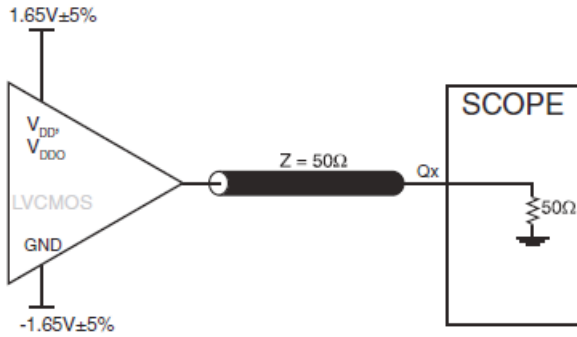
fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



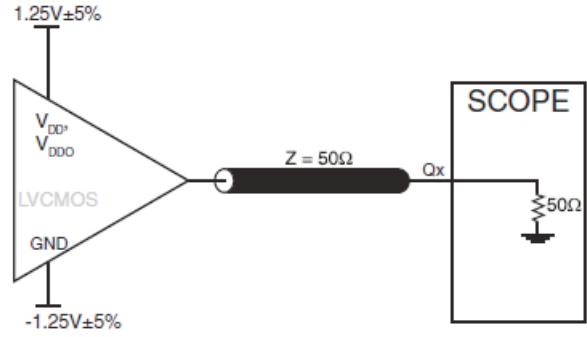
As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise

floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

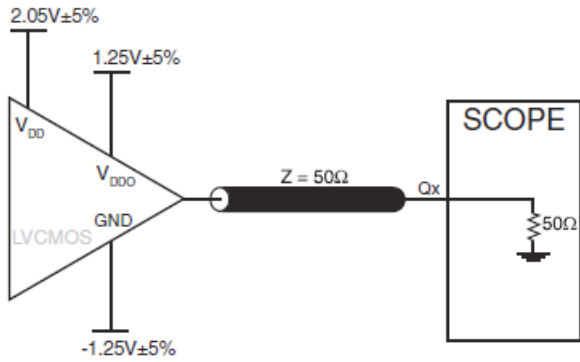
PARAMETER MEASUREMENT INFORMATION



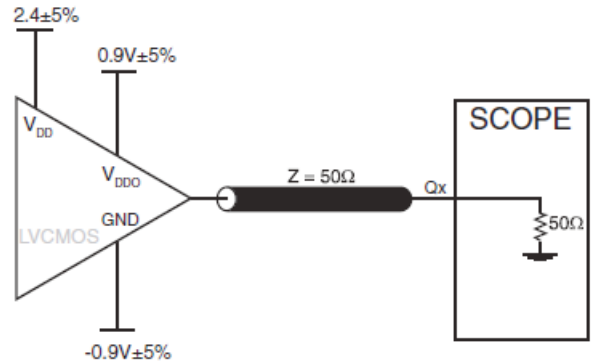
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



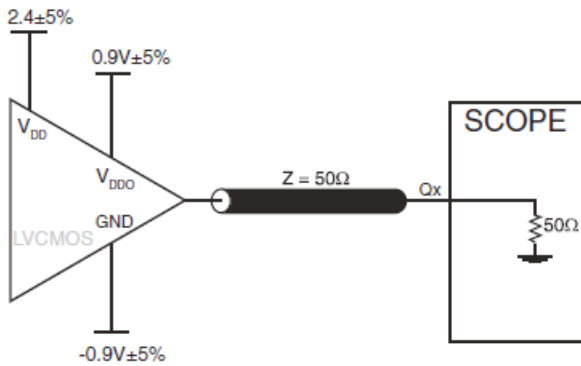
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



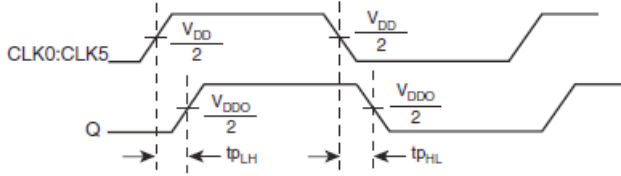
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



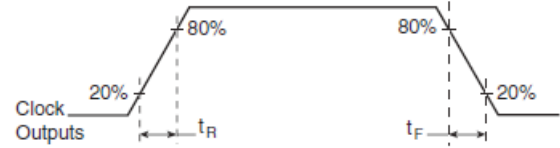
2.5V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



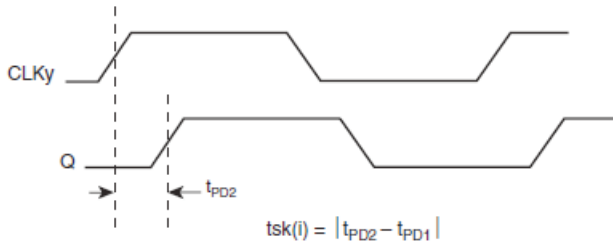
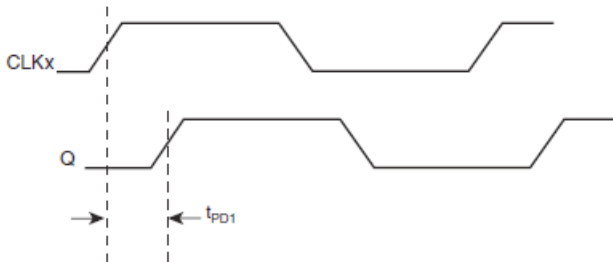
PART-TO-PART SKEW



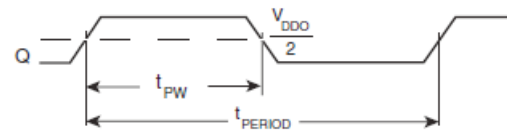
PROPAGATION DELAY



OUTPUT RISE/FALL TIME



INPUT SKEW



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT PINS

INPUTS:

CLK INPUT:

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the CLK input to ground.

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

RELIABILITY INFORMATION

TABLE 6. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 83056 is: 874

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

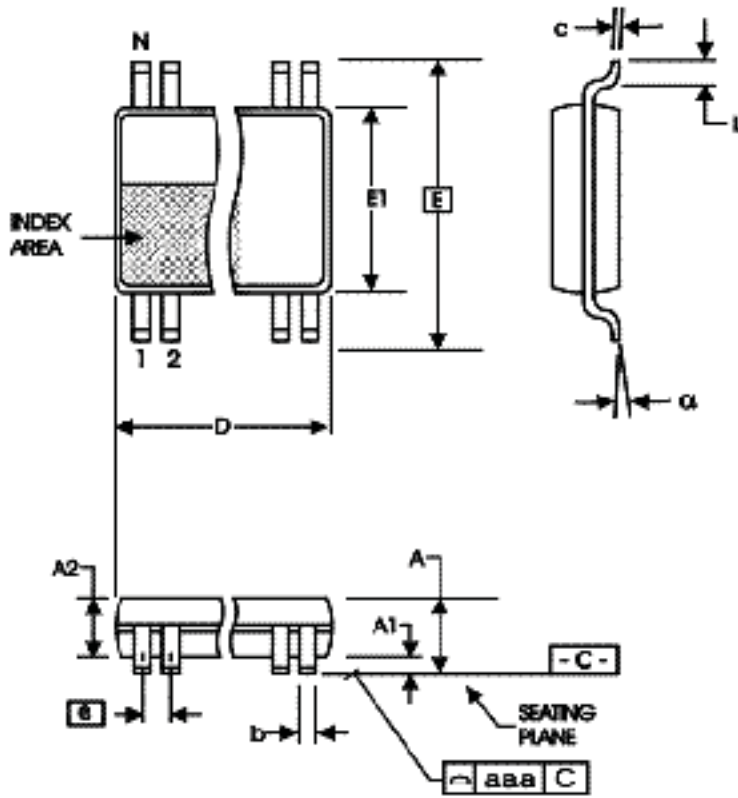


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 8. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
83056AGILF	83056AIL	16 Lead "Lead-Free" TSSOP	tube	-40°C to 85°C
83056AGILFT	83056AIL	16 Lead "Lead-Free" TSSOP	tape & reel	-40°C to 85°C

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T8	12	Ordering Information Table - added Lead-Free marking.	1/18/06
B	T5A - T5E	1 4 - 6 7	Features Section - added Additive Phase Jitter bullet. AC Characteristics Tables - added tjit row and spec. Added Additive Phase Jitter section.	01/04/07
B	T8	13	Ordering Information - removed leaded devices. Updated data sheet format.	3/20/15
B	T8	13	Ordering Information - Removed ICS from the Part/Order Number. Deleted LF note below table. Updated header and footer.	3/10/16

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
 - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
 - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.