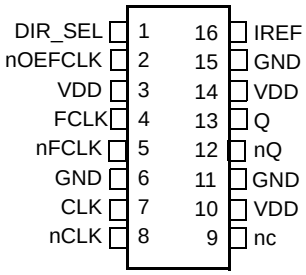
General Description

The 831752 is a high-performance, differential HCSL clock switch. The device is designed for the routing of PCIe clock signals in ATCA/AMC system and is optimized for PCIe Gen 1, Gen 2 and Gen 3. The device has one differential, bi-directional I/O (FCLK) for connection to ATCA clock sources and to clock receivers through a connector. The differential clock input CLK is the local clock input and the HCSL output Q is the local clock output. In the common clock mode, FCLK serves as an input and is routed to the differential HCSL output Q. There are two local clock modes. In the local clock mode 0, CLK is the input, Q is the clock output and FCLK is in high-impedance state. In the local clock mode 1, CLK is the input and both Q and FCLK are the outputs of the locally generated PCIe clock signal. The 831752 is characterized to operate from a 3.3V power or 2.5V power supply. The 831752 supports the switching of PCI Express (2.5 Gb/s), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) clock signals.

Features

- Clock switch for PCIe and ATCA/AMC applications
- Supports local and common ATCA/AMC clock modes
- Bi-directional clock I/O FCLK:
  - When operating as an output, FCLK is a source-terminated HCSL signal.
  - When operating as an input, FCLK accepts HCSL, LVDS and LVPECL levels.
- Local clock input (CLK) accepts HCSL, LVDS and LVPECL differential signals
- Local HCSL clock output (Q)
- Maximum input/output clock frequency: 500MHz
- Maximum input/output data rate: 1000Mb/s (NRZ)
- LVCMOS interface levels for the control inputs
- PCI Express (2.5 Gb/S), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) jitter compliant
- Full 3.3V or 2.5V supply voltage
- Lead-free (RoHS 6) 16-lead TSSOP package
- -40°C to 85°C ambient operating temperature

Pin Assignment



831752
16-lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package, Top View

Block Diagram

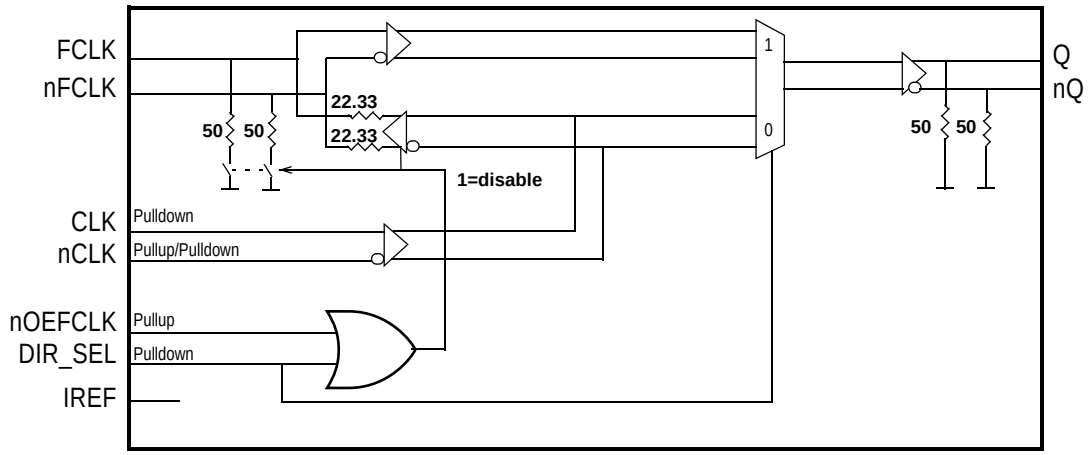


Table 1. Pin Descriptions

Number	Name	Type		Description
1	DIR_SEL	Input	Pulldown	Direction control for the FCLK I/O. Works in conjunction with nOEFCLK. See Table 3 for function. LVCMOS/LVTTL interface levels.
2	nOEFCLK	Input	Pullup	Output enable for the FCLK I/O output. Works in conjunction with DIR_SEL. See Table 3 for function. LVCMOS/LVTTL interface levels.
3, 10, 14	V_{DD}	Power		Core and output power supply pin.
4, 5	FCLK, nFCLK	I/O		Differential I/O. Signal direction is controlled by DIR_SEL. Accepts differential signals when operating as an input. Differential HCSL signals when operating as an output. Internal source termination can be disabled. See Table 3 for function.
6, 11, 15	GND	Power		Power supply ground.
7	CLK	Input	Pulldown	Non-inverting input.
8	nCLK	Input	Pulldown/Pullup	Inverting differential clock input.
9	nc	Unused		No connect.
12, 13	nQ, Q	Output		Differential output pair. HCSL interface levels.
16	IREF	Input		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for the differential current-mode Q and FCLK outputs.

NOTE: P*ullup and pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Function Table

Table 3. Direction Control Function Table

Input DIR_SEL	Input nOEFCLK	Operation	FCLK Function
0	0	Local clock mode 0. The input signal at CLK is routed to both outputs Q and FCLK.	Differential HCSL output with internal 50Ω source termination
0 (default)	1 (default)	Local clock mode 1. The input signal at CLK is routed to the output Q.	Output is disabled (high impedance). Internal 50Ω termination is disabled.
1	X	Common reference clock mode. FCLK is the clock input. Q is the clock output.	Differential clock input. Internal 50Ω source termination is disabled as well as output driver and 22.33Ω resistors.

NOTE: X = 0 or 1

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	81.2°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
I_{DD}	Power Supply Current				64	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	DIR_SEL	V_{DD} = V_{IN} = 2.625V or 3.465V			150	µA
		nOEFLCK				5	µA
I_{IL}	Input Low Current	DIR_SEL	V_{DD} = 2.625V or 3.465V, V_{IN} = 0V	-5			µA
		nOEFLCK		-150			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{DD} = V_{IN} = 3.3V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.3V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.3V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. PCI Express Jitter Specifications, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	f = 100MHz Evaluation Band: 0Hz - Nyquist (clock frequency/2)		9.95	15.5	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz High Band: 1.5MHz - Nyquist (clock frequency/2)		0.82	1.12	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	f = 100MHz Low Band: 10kHz - 1.5MHz		0.04	0.08	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	f = 100MHz Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.153	0.203	0.8	ps

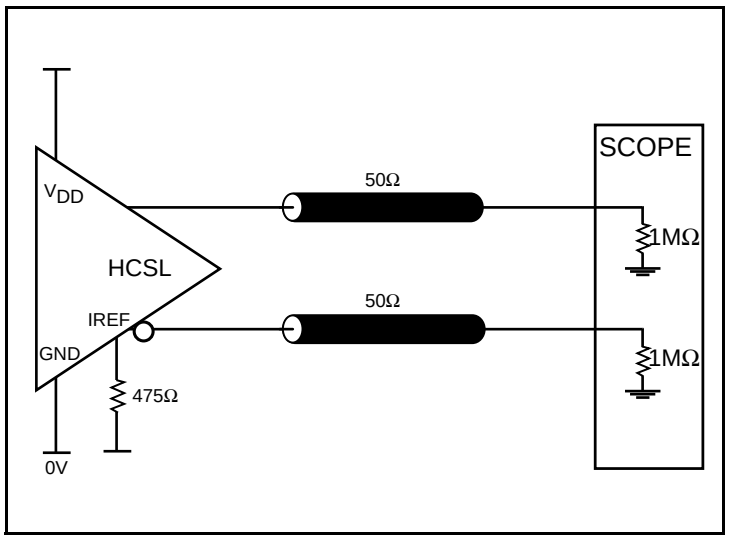
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE: PCI Express Jitter Specifications apply to FCLK and nFCLK and Q, nQ operating as outputs. The source generator used in the PCI Express Jitter measurements is the Stanford Research Systems CG635 2.0GHz Synthesized Clock Generator.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Gen 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

Table 5B. HCSL AC Characteristics, V_{DD} = 3.3V±5% or 2.5V±5%, T_A = -40°C to 85°C

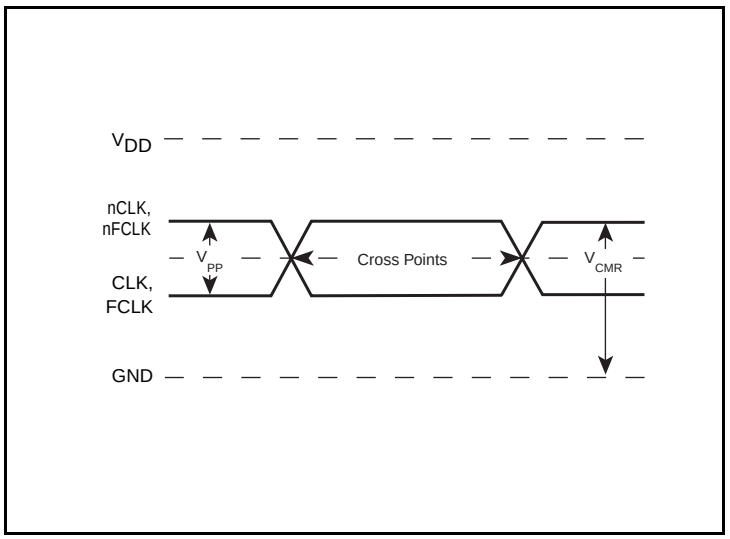
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency			100	500	MHz
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Plot	100MHz, Integration Range: 12kHz – 20MHz		0.3	0.505	ps
t_{PD}	Propagation Delay, NOTE 1	FCLK to Q	1.75		3.65	ns
		CLK to Q	1.95		3.90	ns
		CLK to FCLK	1.50		3.70	ns
MUX_{ISOL}	Mux Isolation	f = 100MHz		-70		dB
Edge Rate	Rise/Fall Edge Rate; NOTE 2, 3		0.6		4	V/ns
V_{RB}	Ringback Voltage; NOTE 2, 4		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; NOTE 2, 4		500			ps
V_{MAX}	Absolute Max Output Voltage; NOTE 5, 6			800	1350	mV
V_{MIN}	Absolute Min Output Voltage; NOTE 5, 7		-300	-35		mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 5, 8, 9		250	385	650	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over all edges; NOTE 5, 8, 10			40	140	mV
odc	Output Duty Cycle; NOTE 11	f ≤ 312.5MHz	44	50	56	%
		f > 312.5MHz	40	50	60	

NOTE: Measurements taken with Q output and FCLK output.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All measurements were taken with FCLK, nFCLK and Q, nQ operating as outputs unless otherwise noted.
NOTE 1: Measured from the differential input cross point to the differential output crossing point.
NOTE 2: Measurement taken from differential waveform.
NOTE 3: Measurement from -150mV to +150mV on the differential waveform (derived from Q minus nQ). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
NOTE 4: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100 differential range. See Parameter Measurement Information Section.
NOTE 5: Measurement taken from single-ended waveform.
NOTE 6: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 7: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 8: Measured at crossing point where the instantaneous voltage value of the rising edge of Q equals the falling edge of nQ. See Parameter Measurement Information Section.
NOTE 9: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.
NOTE 10: Defined as the total variation of all crossing voltage of rising Q and falling nQ. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.
NOTE 11: Input duty cycle must be 50%.
NOTE 12: Matching applies to rising edge rate for Q and falling edge rate for nQ. It is measured using a ±75mV window centered on the median crosspoint where Q meets nQ falling. The median crosspoint is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of Q should be compared to the fall edge rate of nQ, the maximum allowed difference should not exceed 20% of the slowest edge rate.

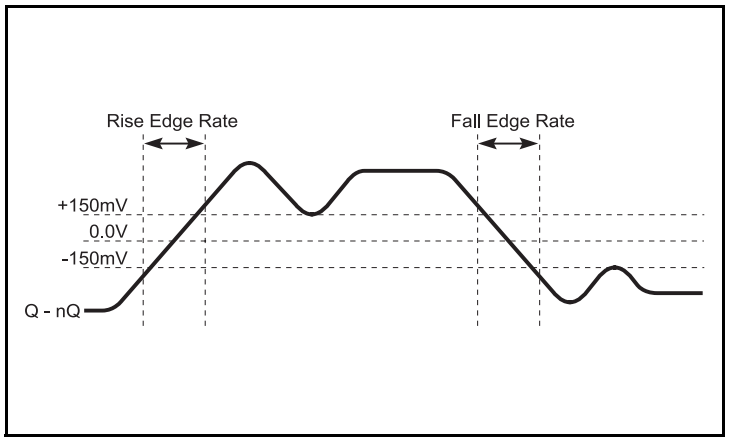
Parameter Measurement Information



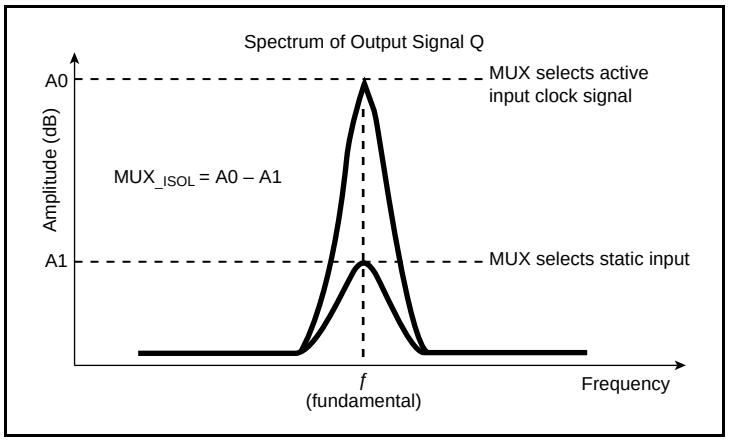
HCSL Output Load AC Test Circuit



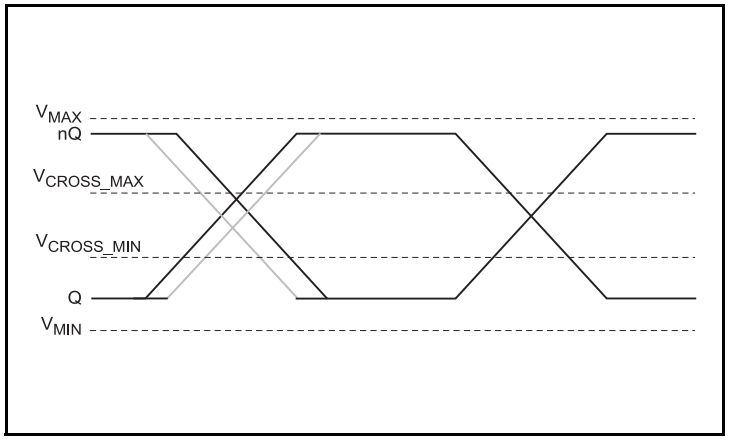
Differential Input Levels



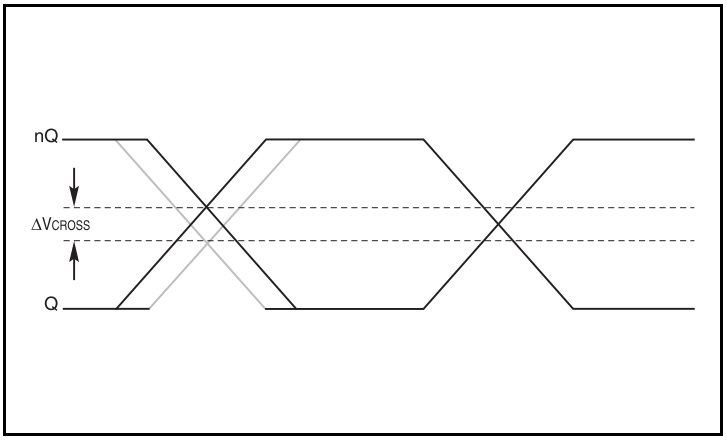
Differential Measurement Points for Rise/Fall Edge Rate



MUX_ISOLATION

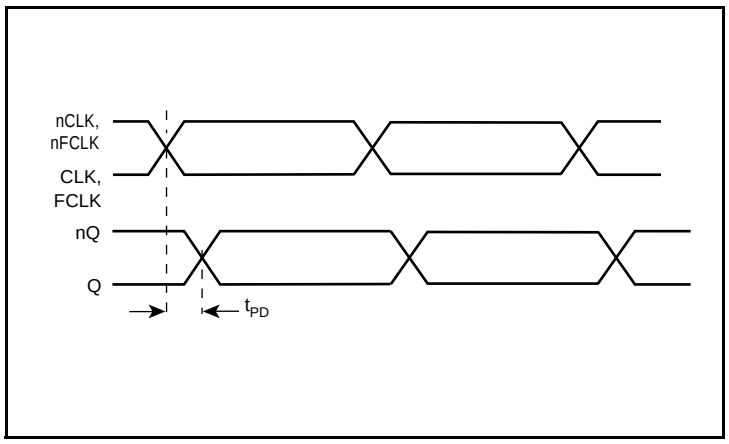


Single-ended Measurement Points for Absolute Cross Point/Swing

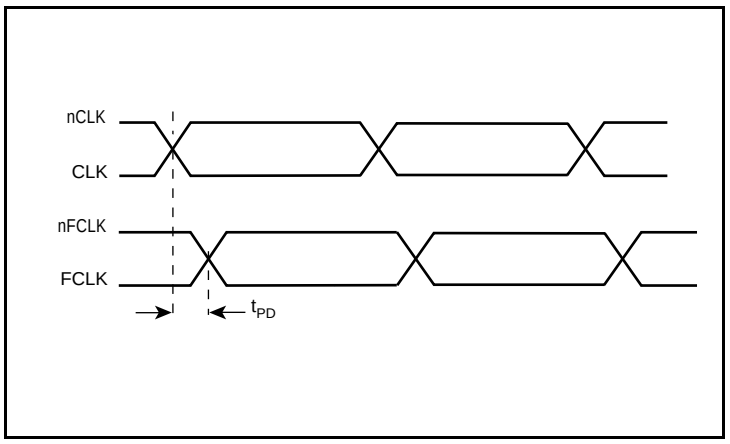


Single-ended Measurement Points for Delta Cross Point

Parameter Measurement Information, continued



Propagation Delay



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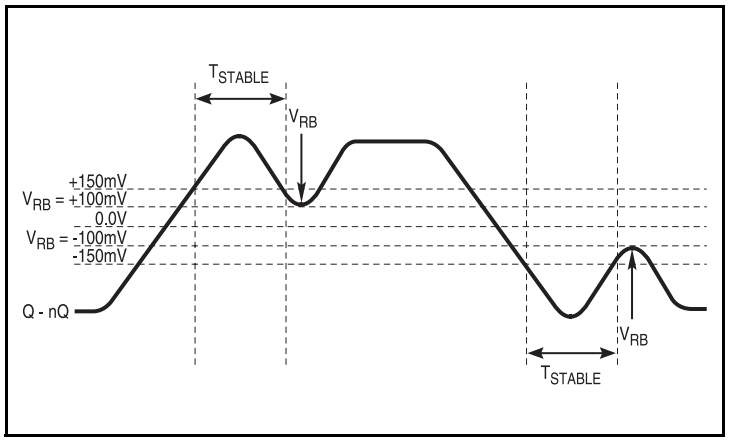


Differential Measurement Points for Ringback

Applications Information

Recommended Termination

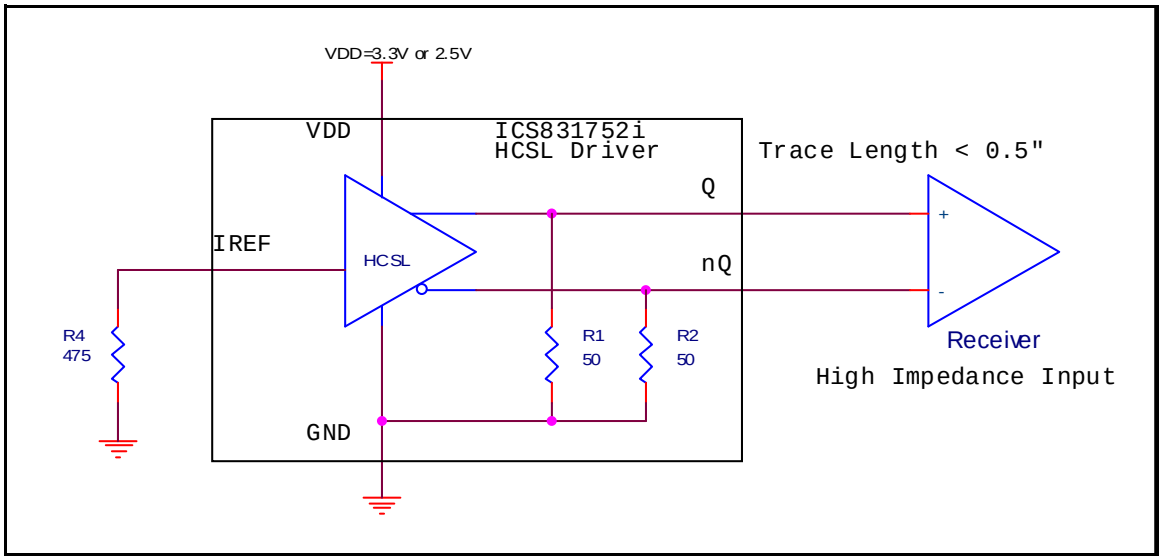


Figure 1. Interface for 831752I HCSL driver with built-in 50 ohm Termination to Receiver with High Input Impedance

Recommendations for Unused Input Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

FCLK/nFCLK Pins

In case FCLK/nFCLK are unused, one of the following two configurations can be used: either FCLK/nFCLK are configured as an output (DIR_SEL = 1) and left floating, or FCLK/nFCLK are configured as an input (DIR_SEL = 0). In this case 1kΩ pulldown is required on FCLK and 1kΩ Pullup is required on nFCLK.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{DD} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

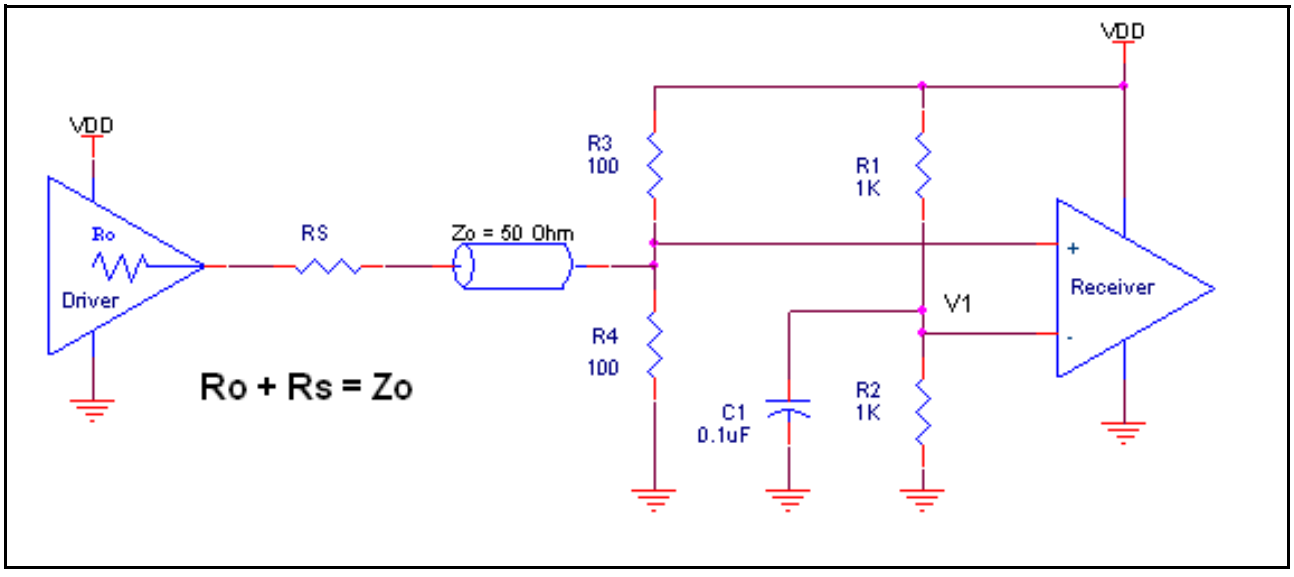


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK/nCLK accepts HCSL, LVDS and LVPECL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements. The figures below also apply to FCLK/nFCLK operating as an input.

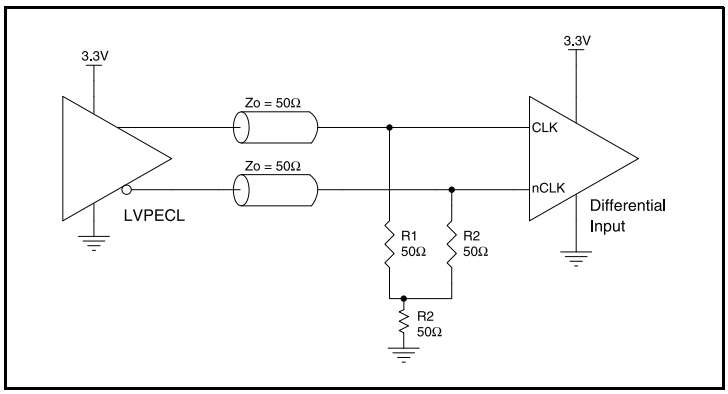


Figure 3A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

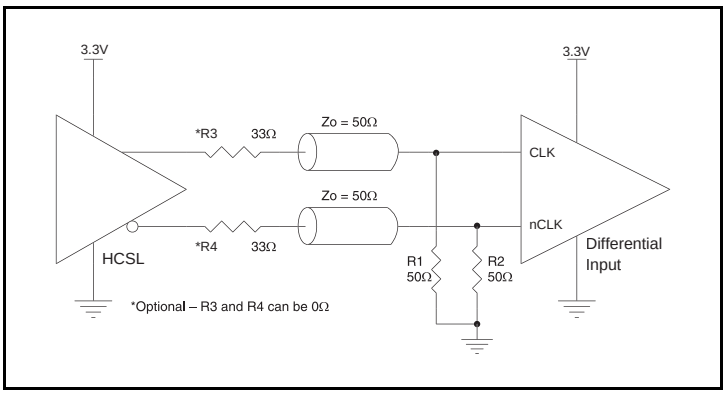


Figure 3B. CLK/nCLK Input Driven by a 3.3V HCSL Driver

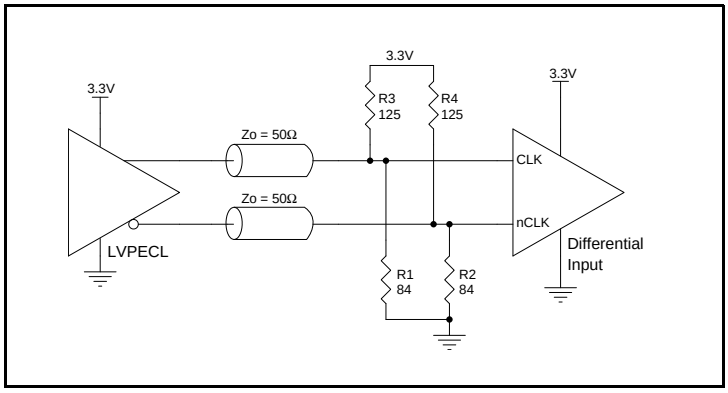


Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

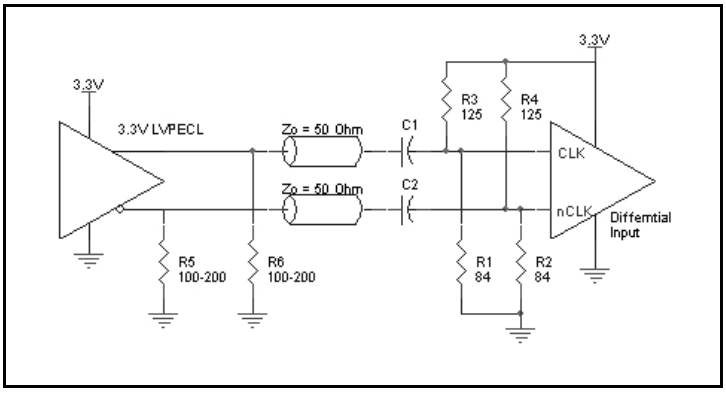


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

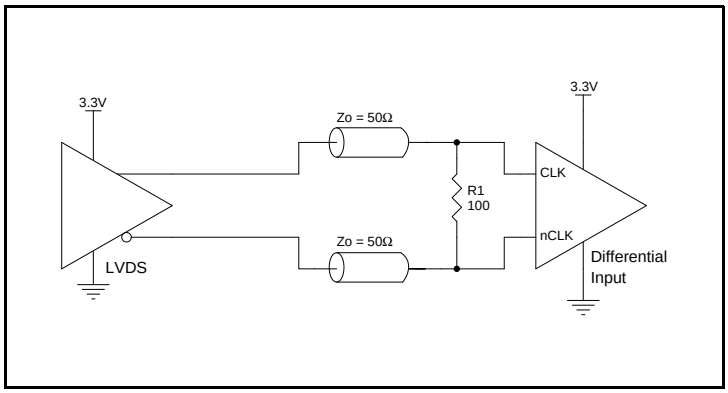


Figure 3E. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK/nCLK accepts HCSL, LVDS and LVPECL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4 E* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements. The figures below also apply to FCLK/nFCLK operating as an input.

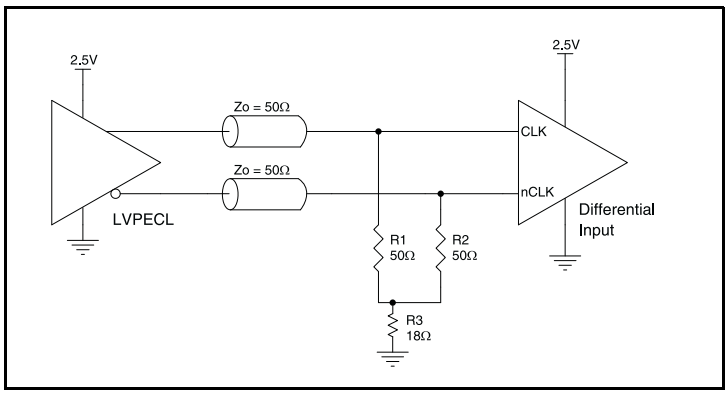


Figure 4A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

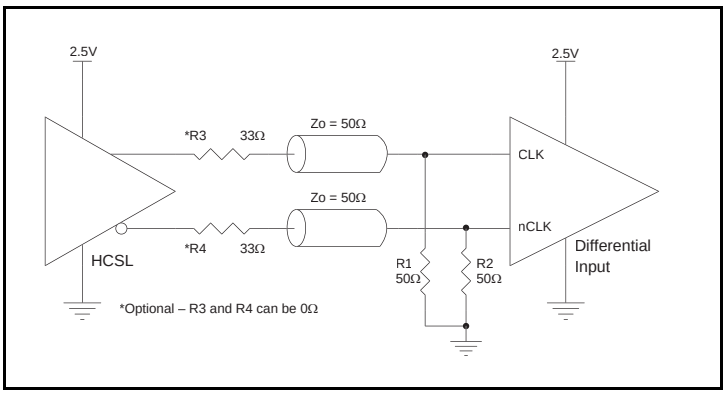


Figure 4B. CLK/nCLK Input Driven by a 2.5V HCSL Driver

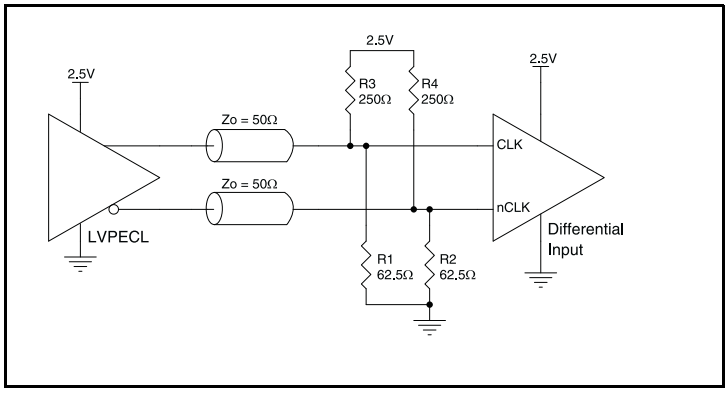


Figure 4C. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

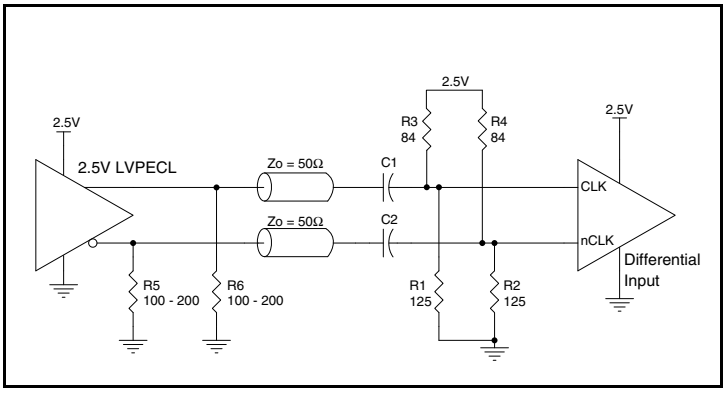


Figure 4D. CLK/nCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

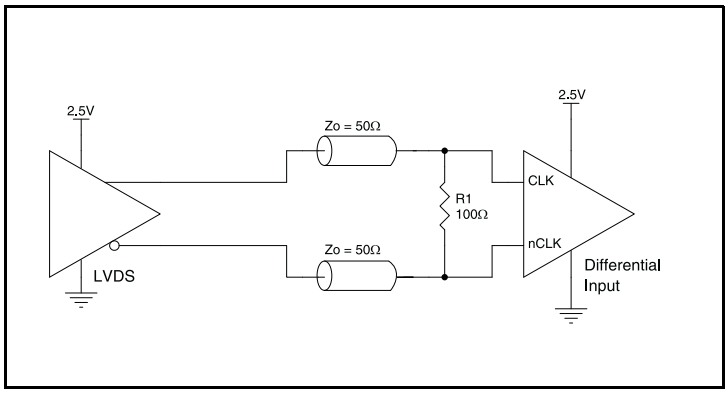


Figure 4E. CLK/nCLK Input Driven by a 2.5V LVDS Driver

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

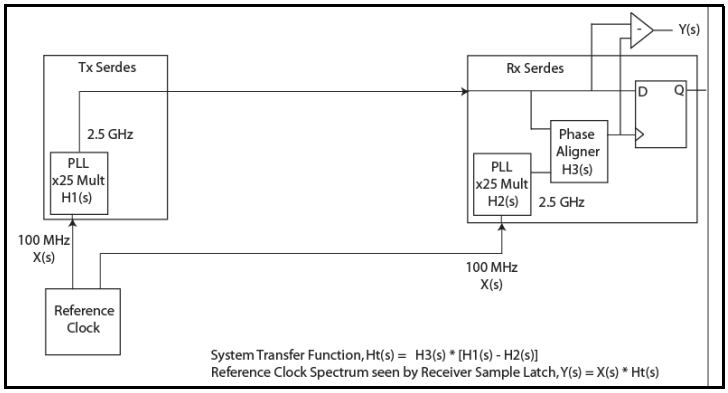
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

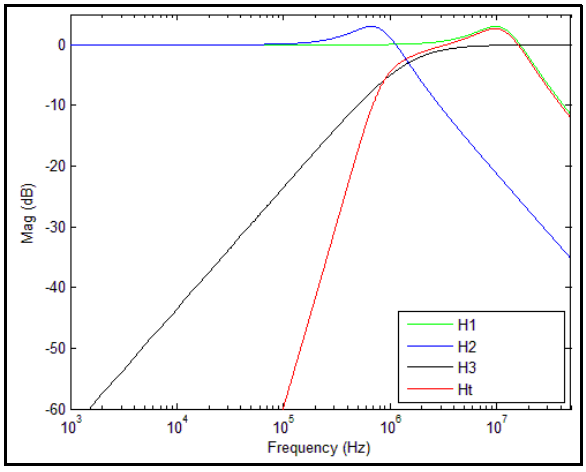
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



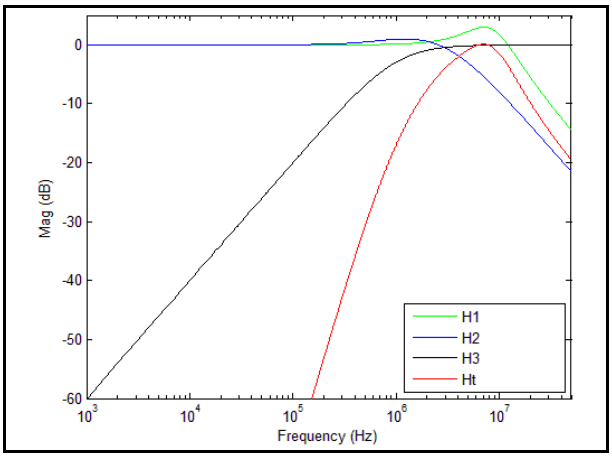
PCI Express Common Clock Architecture

For PCI Express Gen 1, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

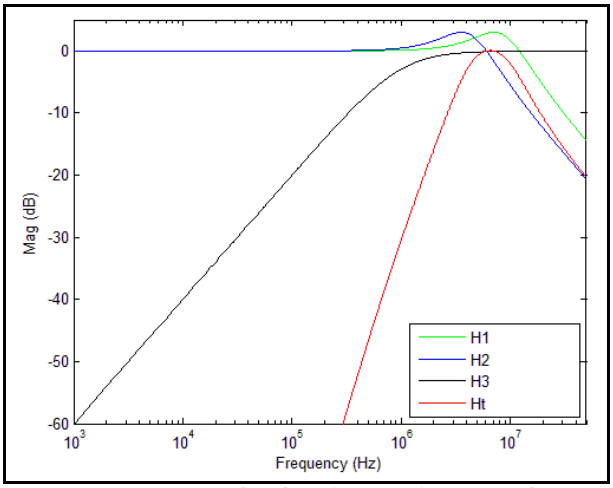


PCIe Gen 1 Magnitude of Transfer Function

For PCI Express Gen 2, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.



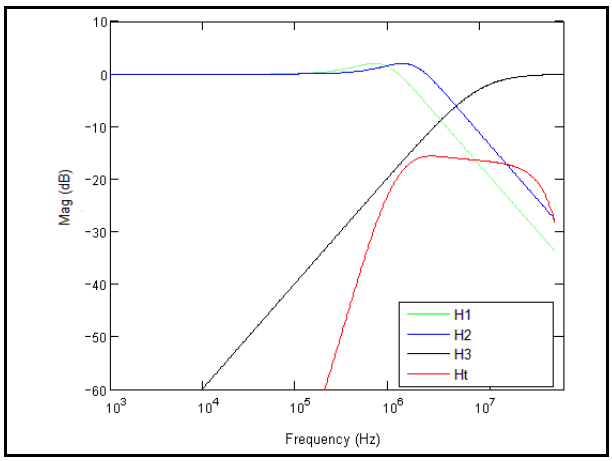
PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

PCI Express Application Note.

For PCI Express Gen 3, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

Power Considerations

This section provides information on power dissipation and junction temperature for the 831752I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 831752I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 64mA = **221.76mW**

Power dissipation for the FCLK, nFCLK input internal 50ohm termination. Assume the FCLK, nFCLK input is driven by a HCSL driver. Logic High input current ~ 17mA. Logic low current ~ 0mA.

- Power (input) = 50ohm * $(17mA)^2$ = 14.45mW

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 221.76mW + 14.45mW = **236.21mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 81.2°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.236W * 81.2°C/W = 104.2°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance θ_{JA} for 16 Lead TSSOP, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Package Outline and Package Dimensions

Table 7. θ_{JA} vs. Air Flow Table for a 16 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	81.2°C/W	73.9°C/W	70.2°C/W

Transistor Count

The transistor count for 831752I is: 446

Package Outline and Package Dimensions

Package Outline - G Suffix for 16 Lead TSSOP

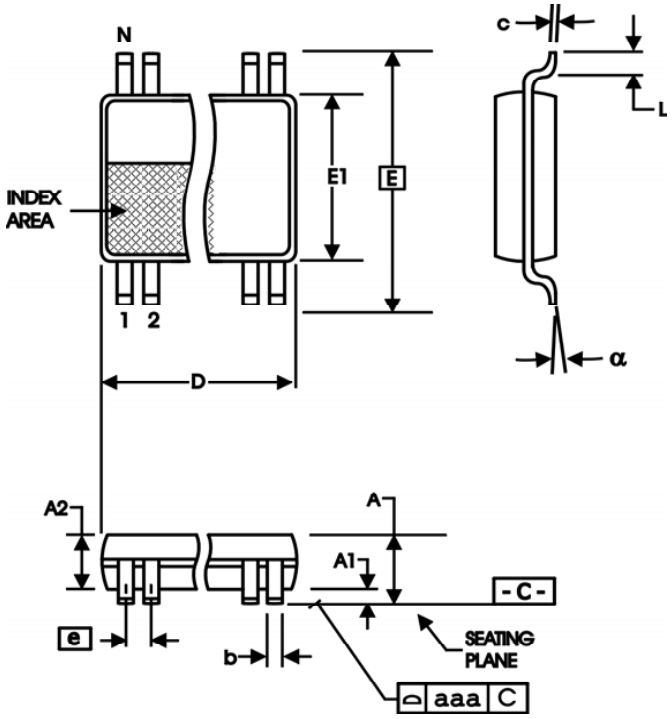


Table 8. Package Dimensions for 16 Lead TSSOP

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	16	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
831752AGILF	31752AIL	Lead-Free, 16-lead TSSOP	Tube	-40°C to 85°C
831752AGILFT	31752AIL	Lead-Free, 16-lead TSSOP	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	9	15	Ordering Information Table - corrected marking	12/20/13
A			Removed ICS from part number where needed. Updated header and footer.	4/5/16
B		1	Block Diagram - corrected labels. Deleted “I” suffix from part number.	6/28/16

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