**General Description**

The 83905I is a low skew, 1-to-6 LVCMOS / LVTTL Fanout Buffer. The low impedance LVCMOS/LVTTL outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased from 6 to 12 by utilizing the ability of the outputs to drive two series terminated lines. The 83905I is characterized at full 3.3V, 2.5V, and 1.8V, mixed 3.3V/2.5V, 3.3V/1.8V and 2.5V/1.8V output operating supply modes. Guaranteed output and part-to-part skew characteristics along with the 1.8V output capabilities makes the 83905I ideal for high performance, single ended applications that also require a limited output voltage.

**Features**

- Six LVCMOS / LVTTL outputs
- Outputs able to drive 12 series terminated lines
- Crystal Oscillator Interface
- Crystal input frequency range: 10MHz to 40MHz
- Output skew: 80ps (maximum)
- RMS phase jitter @ 25MHz, (100Hz – 1MHz): 0.26ps (typical), $V_{DD} = V_{DDO} = 2.5V$
- 5V tolerant enable inputs
- Synchronous output enables
- Operating power supply modes:
  - Full 3.3V, 2.5V, 1.8V
  - Mixed 3.3V core/2.5V output operating supply
  - Mixed 3.3V core/1.8V output operating supply
  - Mixed 2.5V core/1.8V output operating supply
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

**Pin Assignments**

| XTAL_OUT  | 1  | XTAL_IN | 16 |
| ENABLE2   | 2  | ENABLE1 | 15 |
| GND       | 3  | BCLK5   | 14 |
| BCLK4     | 4  | VDDO    | 13 |
| BCLK3     | 5  | BCLK4   | 12 |
| BCLK1     | 6  | GND     | 11 |
| GND       | 7  | BCLK3   | 10 |
| BCLK2     | 8  | BCLK2   | 9  |

16-Lead TSSOP
4.4mm x 5.0mm x 0.925mm package body
G Package
Top View

**Offset Noise Power**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Offset Noise Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>100Hz</td>
<td>-129.7 dBC/Hz</td>
</tr>
<tr>
<td>1kHz</td>
<td>-144.4 dBC/Hz</td>
</tr>
<tr>
<td>10kHz</td>
<td>-147.3 dBC/Hz</td>
</tr>
<tr>
<td>100kHz</td>
<td>-157.3 dBC/Hz</td>
</tr>
</tbody>
</table>

**Block Diagram**
Pin Descriptions and Characteristics

Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>XTAL_OUT</td>
<td>Output</td>
<td>Crystal oscillator interface. XTAL_OUT is the output.</td>
</tr>
<tr>
<td>2</td>
<td>ENABLE2</td>
<td>Input</td>
<td>Clock enable. LVCMOS/LVTTL interface levels. See Table 3.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>4</td>
<td>BCLK0</td>
<td>Output</td>
<td>Clock output. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>5</td>
<td>V_DDO</td>
<td>Power</td>
<td>Output supply pin.</td>
</tr>
<tr>
<td>6</td>
<td>BCLK1</td>
<td>Output</td>
<td>Clock output. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>8</td>
<td>BCLK2</td>
<td>Output</td>
<td>Clock output. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>9</td>
<td>V_DD</td>
<td>Power</td>
<td>Power supply pin.</td>
</tr>
<tr>
<td>10</td>
<td>BCLK3</td>
<td>Output</td>
<td>Clock output. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>12</td>
<td>BCLK4</td>
<td>Output</td>
<td>Clock output. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>13</td>
<td>V_DDO</td>
<td>Power</td>
<td>Output supply pin.</td>
</tr>
<tr>
<td>14</td>
<td>BCLK5</td>
<td>Output</td>
<td>Clock output. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>15</td>
<td>ENABLE1</td>
<td>Input</td>
<td>Clock enable. LVCMOS/LVTTL interface levels. See Table 3.</td>
</tr>
<tr>
<td>16</td>
<td>XTAL_IN</td>
<td>Input</td>
<td>Crystal oscillator interface. XTAL_IN is the input.</td>
</tr>
</tbody>
</table>

Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td>V_DD = 3.465V</td>
<td>4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 2.625V</td>
<td>19</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 2.0V</td>
<td>18</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>C_PD</td>
<td>Power Dissipation Capacitance (per output)</td>
<td>V_DD = 3.3V ± 5%</td>
<td>7</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 2.5V ± 5%</td>
<td>7</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DD = 1.8V ± 0.2V</td>
<td>10</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>
Function Table

Table 3. Output Enable and Clock Enable Function Table

<table>
<thead>
<tr>
<th>Control Inputs</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BCLK[0:4]</td>
</tr>
<tr>
<td>ENABLE 1</td>
<td>ENABLE2</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Figure 1. Enable Timing Diagram
Absolute Maximum Ratings

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{DD}$</td>
<td>4.6V</td>
</tr>
<tr>
<td>Inputs, $V_I$</td>
<td>-0.5V to $V_{DD} + 0.5V$</td>
</tr>
<tr>
<td>Outputs, $V_O$</td>
<td>-0.5V to $V_{DDO} + 0.5V$</td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_{JA}$</td>
<td>89°C/W (0 mps)</td>
</tr>
<tr>
<td>16-Lead TSSOP package</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td>ENABLE [1:2] = 00</td>
<td></td>
<td></td>
<td>10</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>Output Supply Current</td>
<td>ENABLE [1:2] = 00</td>
<td></td>
<td></td>
<td>5</td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td>ENABLE [1:2] = 00</td>
<td></td>
<td></td>
<td>8</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>Output Supply Current</td>
<td>ENABLE [1:2] = 00</td>
<td></td>
<td></td>
<td>4</td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 4C. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td>ENABLE [1:2] = 00</td>
<td></td>
<td></td>
<td>5</td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>Output Supply Current</td>
<td>ENABLE [1:2] = 00</td>
<td></td>
<td></td>
<td>3</td>
<td>mA</td>
</tr>
</tbody>
</table>
## Table 4D. Power Supply DC Characteristics, $V_{DD} = 3.3\,\text{V} \pm 5\%, V_{DDO} = 2.5\,\text{V} \pm 5\%, T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Power Supply Current</td>
<td>$\text{ENABLE [1:2]} = 00$</td>
<td></td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>Output Supply Current</td>
<td>$\text{ENABLE [1:2]} = 00$</td>
<td></td>
<td>4</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

## Table 4E. Power Supply DC Characteristics, $3.3\,\text{V} \pm 5\%, V_{DDO} = 1.8\,\text{V} \pm 0.2\,\text{V}, T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Power Supply Current</td>
<td>$\text{ENABLE [1:2]} = 00$</td>
<td></td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>Output Supply Current</td>
<td>$\text{ENABLE [1:2]} = 00$</td>
<td></td>
<td>3</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

## Table 4F. Power Supply DC Characteristics, $V_{DD} = 2.5\,\text{V} \pm 5\%, V_{DDO} = 1.8\,\text{V} \pm 0.2\,\text{V}, T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDO}$</td>
<td>Output Supply Voltage</td>
<td></td>
<td>1.6</td>
<td>1.8</td>
<td>2.0</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Power Supply Current</td>
<td>$\text{ENABLE [1:2]} = 00$</td>
<td></td>
<td>8</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDO}$</td>
<td>Output Supply Current</td>
<td>$\text{ENABLE [1:2]} = 00$</td>
<td></td>
<td>3</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>
### Table 4G. LVCMOS/LVTTL DC Characteristics, $T_A = -40°C$ to $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{DD} = 3.3V \pm 5%$</td>
<td>2</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%$</td>
<td>1.7</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 1.8V \pm 0.2V$</td>
<td>0.65 * $V_{DD}$</td>
<td>$V_{DD} + 0.3$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{DD} = 3.3V \pm 5%$</td>
<td>-0.3</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V \pm 5%$</td>
<td>-0.3</td>
<td>0.7</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 1.8V \pm 0.2V$</td>
<td>-0.3</td>
<td>$0.35 \times V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage</td>
<td>$V_{DDO} = 3.3V \pm 5%$; NOTE 1</td>
<td>2.6</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DDO} = 2.5V \pm 5%$; $I_{OH} = -1mA$</td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DDO} = 2.5V \pm 5%$; NOTE 1</td>
<td>1.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DDO} = 1.8V \pm 0.2V$; NOTE 1</td>
<td>$V_{DDO} - 0.3$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>$V_{DDO} = 3.3V \pm 5%$; NOTE 1</td>
<td>0.5</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DDO} = 2.5V \pm 5%$; $I_{OL} = 1mA$</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DDO} = 2.5V \pm 5%$; NOTE 1</td>
<td>0.45</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DDO} = 1.8V \pm 0.2V$; NOTE 1</td>
<td>0.35</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1: Outputs terminated with $50\Omega$ to $V_{DDO}/2$. See Parameter Measurement Information, *Output Load Test Circuit diagrams*.

### Table 5. Crystal Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode of Oscillation</td>
<td>Fundamental</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>10</td>
<td>40</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equivalent Series Resistance (ESR)</td>
<td>50</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shunt Capacitance</td>
<td>7</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drive Level</td>
<td>1</td>
<td>mW</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
AC Electrical Characteristics

Table 6A. AC Characteristics, \( V_{DD} = V_{DDO} = 3.3V \pm 5\% \), \( T_A = -40^\circ C \) to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{MAX}} )</td>
<td>Output Frequency</td>
<td>Using External Crystal</td>
<td>10</td>
<td>40</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Using External Clock Source NOTE 1</td>
<td>DC</td>
<td>100</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( \text{odc} )</td>
<td>Output Duty Cycle</td>
<td></td>
<td>48</td>
<td>52</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{sk}} )</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td></td>
<td>80</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{j}it} )</td>
<td>RMS Phase Jitter (Random); NOTE 4</td>
<td>25MHz, Integration Range: 100Hz – 1MHz</td>
<td>0.13</td>
<td>0.13</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_R / t_F )</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>200</td>
<td>800</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{EN}} )</td>
<td>Output Enable Time; NOTE 5</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{DIS}} )</td>
<td>Output Disable Time; NOTE 5</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at \( f \leq f_{\text{MAX}} \) using a crystal input unless noted otherwise.

NOTE: Terminated at 50Ω to \( V_{DDO}/2 \).

NOTE 1: XTAL_IN can be overdriven by a single-ended LVCMOS signal. Please refer to Application Information section.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at \( V_{DDO}/2 \).

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

Table 6B. AC Characteristics, \( V_{DD} = V_{DDO} = 2.5V \pm 5\% \), \( T_A = -40^\circ C \) to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{MAX}} )</td>
<td>Output Frequency</td>
<td>Using External Crystal</td>
<td>10</td>
<td>40</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Using External Clock Source NOTE 1</td>
<td>DC</td>
<td>100</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>( \text{odc} )</td>
<td>Output Duty Cycle</td>
<td></td>
<td>47</td>
<td>53</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{sk}} )</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td></td>
<td>80</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{j}it} )</td>
<td>RMS Phase Jitter (Random); NOTE 4</td>
<td>25MHz, Integration Range: 100Hz – 1MHz</td>
<td>0.26</td>
<td>0.26</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_R / t_F )</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>200</td>
<td>800</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{EN}} )</td>
<td>Output Enable Time; NOTE 5</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td>( t_{\text{DIS}} )</td>
<td>Output Disable Time; NOTE 5</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at \( f \leq f_{\text{MAX}} \) using a crystal input unless noted otherwise.

NOTE: Terminated at 50Ω to \( V_{DDO}/2 \).

NOTE 1: XTAL_IN can be overdriven by a single-ended LVCMOS signal. Please refer to Application Information section.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at \( V_{DDO}/2 \).

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
Table 6C. AC Characteristics, $V_{DD} = V_{DDO} = 1.8V \pm 0.2V, T_A = -40°C to 85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Output Frequency</td>
<td>Using External Crystal</td>
<td>10</td>
<td>40</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Using External Clock Source NOTE 1</td>
<td>DC</td>
<td>100</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td></td>
<td>47</td>
<td>53</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>fsk(0)</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td></td>
<td>80</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>tjit(Ø)</td>
<td>RMS Phase Jitter (Random)</td>
<td>25MHz, Integration Range: 100Hz – 1MHz</td>
<td></td>
<td>0.27</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$t_R / t_F$</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>200</td>
<td>900</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>Output Enable Time; NOTE 4</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>Output Disable Time; NOTE 4</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

NOTE: Terminated at 50Ω to $V_{DDO}/2$.

NOTE 1: XTAL_IN can be overdriven by a single-ended LVCMOS signal. Please refer to Application Information section.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

Table 6D. AC Characteristics, $V_{DD} = 3.3V \pm 5\%, V_{DDO} = 2.5V \pm 5\%, T_A = -40°C to 85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Output Frequency</td>
<td>Using External Crystal</td>
<td>10</td>
<td>40</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Using External Clock Source NOTE 1</td>
<td>DC</td>
<td>100</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td></td>
<td>48</td>
<td>52</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>fsk(0)</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td></td>
<td>80</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>tjit</td>
<td>RMS Phase Jitter (Random)</td>
<td>25MHz, Integration Range: 100Hz – 1MHz</td>
<td></td>
<td>0.14</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$t_R / t_F$</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>200</td>
<td>800</td>
<td>ps</td>
<td></td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>Output Enable Time; NOTE 4</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>Output Disable Time; NOTE 4</td>
<td>ENABLE1</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ENABLE2</td>
<td></td>
<td>4</td>
<td>cycles</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

NOTE: Terminated at 50Ω to $V_{DDO}/2$.

NOTE 1: XTAL_IN can be overdriven by a single-ended LVCMOS signal. Please refer to Application Information section.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
Table 6E. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Output Frequency</td>
<td>Using External Crystal</td>
<td>10</td>
<td>40</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Using External Clock Source NOTE 1</td>
<td>DC</td>
<td>100</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td></td>
<td>48</td>
<td>52</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td>80</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{jit}$</td>
<td>RMS Phase Jitter (Random)</td>
<td>25MHz, Integration Range: $100Hz - 1MHz$</td>
<td>0.18</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_R / t_F$</td>
<td>Output Rise/Fall Time</td>
<td>$20%$ to $80%$</td>
<td>200</td>
<td>900</td>
<td>ps</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

NOTE 1: XTAL_IN can be overdriven by a single-ended LVCMOS signal. Please refer to Application Information section.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.

Table 6F. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $V_{DDO} = 1.8V \pm 0.2V$, $T_A = -40^\circ C$ to $85^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Output Frequency</td>
<td>Using External Crystal</td>
<td>10</td>
<td>40</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Using External Clock Source NOTE 1</td>
<td>DC</td>
<td>100</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td></td>
<td>47</td>
<td>53</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td>80</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{jit}$</td>
<td>RMS Phase Jitter (Random)</td>
<td>25MHz, Integration Range: $100Hz - 1MHz$</td>
<td>0.19</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_R / t_F$</td>
<td>Output Rise/Fall Time</td>
<td>$20%$ to $80%$</td>
<td>200</td>
<td>900</td>
<td>ps</td>
<td></td>
</tr>
</tbody>
</table>

NOTE: All parameters measured at $f \leq f_{MAX}$ using a crystal input unless noted otherwise.

NOTE 1: XTAL_IN can be overdriven by a single-ended LVCMOS signal. Please refer to Application Information section.

NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: See phase noise plot.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.
Typical Phase Noise at 25MHz (2.5V Core/2.5V Output)

- RMS Phase Jitter (Random)
  - 100Hz to 1MHz = 0.26ps (typical)

Raw Phase Noise Data

Typical Phase Noise at 25MHz (2.5V Core/2.5V Output)

- RMS Phase Jitter (Random)
  - 100Hz to 1MHz = 0.13ps (typical)

Raw Phase Noise Data
Parameter Measurement Information

3.3V Core/3.3V LVCMOS Output Load AC Test Circuit

2.5V Core/2.5V LVCMOS Output Load AC Test Circuit

1.8V Core/1.8V LVCMOS Output Load AC Test Circuit

3.3V Core/2.5V LVCMOS Output Load AC Test Circuit

3.3V Core/1.8V LVCMOS Output Load AC Test Circuit

2.5V Core/1.8V LVCMOS Output Load AC Test Circuit
Parameter Measurement Information, continued

Output Skew

Output Duty Cycle/Pulse Width/Period

Output Rise/Fall Time
Applications Information

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure 2. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

Figure 2. General Diagram for LVCMOS Driver to XTAL Input Interface
VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 3. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13milis (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

![Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)](image)

Recommendations for Unused Input and Output Pins

**Inputs:**

**LVCMOS Control Pins**

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

**Outputs:**

**LVCMOS Outputs**

All unused LVCMOS output can be left floating. There should be no trace attached.
**Layout Guideline**

*Figure 4* shows an example of 83905I application schematic. The schematic example focuses on functional connections and is not configuration specific. In this example, the device is operated at $V_{DD} = 3.3\text{V}$ and $V_{DDO} = 1.8\text{V}$. The crystal inputs are loaded with an 18pf load resonant quartz crystal. The tuning capacitors ($C_1$, $C_2$) are fairly accurate, but minor adjustments might be required. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For the LVCMOS output drivers, two termination examples are shown in the schematic. For additional termination examples are shown in the LVCMOS Termination Application Note.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 83905I provides separate $V_{DD}$ and $V_{DDO}$ power supplies to isolate any high switching noise from coupling into the internal oscillator. In order to achieve the best possible filtering, it is highly recommended that the 0.1uF capacitors on the device side of the ferrite beads be placed on the device side of the PCB as close to the power pins as possible. This is represented by the placement of these capacitors in the schematic. If space is limited, the ferrite beads, 10uF and 0.1uF capacitor connected to the board supplies can be placed on the opposite side of the PCB. If space permits, place all filter components on the device side of the board.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 0kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

---

*Figure 4. Schematic of Recommended Layout*
Power Considerations

This section provides information on power dissipation and junction temperature for the 83905I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 83905I is the sum of the core power plus the analog power plus the power dissipated due to the load. The following is the power dissipation for VDD = 3.3V + 5% = 3.465V, which gives worst case results.

- Power (core)\text{MAX} = VDD\text{MAX} \times (I_{DD} + I_{DDO}) = 3.465V \times (10mA + 5mA) = 51.9mW
- Output Impedance R\text{OUT} Power Dissipation due to Loading 50\Omega to VDD/2
  Output Current I_{OUT} = VDD\text{MAX} / (2 \times (50\Omega + R\text{OUT})) = 3.465V / (2 \times (50\Omega + 7\Omega)) = 30.4mA
- Power Dissipation on the R\text{OUT} per LVCMOS output
  Power (R\text{OUT}) = R\text{OUT} \times (I_{OUT})^2 = 7\Omega \times (30.4\text{mA})^2 = 6.5mW per output
- Total Power Dissipation on the R\text{OUT}
  Total Power (R\text{OUT}) = 6.5mW \times 6 = 39mW

Dynamic Power Dissipation at 25MHz

\[ \text{Power (25MHz)} = C_{PD} \times \text{Frequency} \times (VDD)^2 = 19pF \times 25MHz \times (3.465V)^2 = 5.70mW per output \]
\[ \text{Total Power (25MHz)} = 5.70mW \times 6 = 34.2mW \]

Total Power Dissipation

- Total Power
  \[ = \text{Power (core)MAX} + \text{Total Power (R\text{OUT})} + \text{Total Power (25MHz)} \]
  \[ = 51.98mW + 39mW + 34.2mW \]
  \[ = 125.1mW \]

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: \[ Tj = \theta_{JA} \times Pd_{\text{total}} + T_A \]

\[ Tj = \text{Junction Temperature} \]
\[ \theta_{JA} = \text{Junction-to-Ambient Thermal Resistance} \]
\[ Pd_{\text{total}} = \text{Total Device Power Dissipation (example calculation is in section 1 above)} \]
\[ T_A = \text{Ambient Temperature} \]

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \( \theta_{JA} \) must be used. Assuming no air flow and a multi-layer board, the appropriate value is 89°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

\[ 85°C + 0.125W \times 89°C/W = 96.1°C. \] This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance \( \theta_{JA} \) for 16-Lead TSSOP, Forced Convection

<table>
<thead>
<tr>
<th>( \theta_{JA} ) by Velocity</th>
<th>0</th>
<th>200</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linear Feet per Minute</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Single-Layer PCB, JEDEC Standard Test Boards</td>
<td>137.1°C/W</td>
<td>118.2°C/W</td>
<td>106.8°C/W</td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>89.0°C/W</td>
<td>81.8°C/W</td>
<td>78.1°C/W</td>
</tr>
</tbody>
</table>

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.
## Reliability Information

### Table 8. $\theta_{JA}$ vs. Air Flow Table for a 16-Lead TSSOP

<table>
<thead>
<tr>
<th>Linear Feet per Minute</th>
<th>$\theta_{JA}$ vs. Air Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td>Single-Layer PCB, JEDEC Standard Test Boards</td>
<td>137.1°C/W</td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>89.0°C/W</td>
</tr>
</tbody>
</table>

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## Transistor Count

The transistor count for 83905I: 339
### Package Outline and Package Dimensions

**Package Outline - G Suffix for 16-Lead TSSOP**

#### Table 9. Package Dimensions for 16-Lead TSSOP

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>1.20</td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>0.80</td>
<td>1.05</td>
</tr>
<tr>
<td>b</td>
<td>0.19</td>
<td>0.30</td>
</tr>
<tr>
<td>c</td>
<td>0.09</td>
<td>0.20</td>
</tr>
<tr>
<td>D</td>
<td>4.90</td>
<td>5.10</td>
</tr>
<tr>
<td>E</td>
<td>6.40 Basic</td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>4.30</td>
<td>4.50</td>
</tr>
<tr>
<td>e</td>
<td>0.65 Basic</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.75</td>
</tr>
<tr>
<td>α</td>
<td>0°</td>
<td>8°</td>
</tr>
<tr>
<td>aaa</td>
<td>0.10</td>
<td></td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MO-153
### Ordering Information

Table 10. Ordering Information

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>83905AGILF</td>
<td>83905AIL</td>
<td>16-Lead TSSOP, Lead-Free</td>
<td>Tube</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>83905AGILFT</td>
<td>83905AIL</td>
<td>16-Lead TSSOP, Lead-Free</td>
<td>Tape &amp; Reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>
# Revision History Sheet

<table>
<thead>
<tr>
<th>Rev</th>
<th>Table</th>
<th>Page</th>
<th>Description of Change</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td></td>
<td>2</td>
<td>Added Enable Timing Diagram.</td>
<td>3/28/05</td>
</tr>
<tr>
<td>B</td>
<td>T6A - T6F</td>
<td>1 5 - 7 8</td>
<td>Features Section - added RMS Phase Jitter bullet. AC Characteristics Tables - added RMS Phase Jitter specs. Corrected ambient operating temperature Added Phase Noise Plot.</td>
<td>4/8/05</td>
</tr>
<tr>
<td>B</td>
<td></td>
<td>11 12</td>
<td>Added Crystal Input Interface in Application Section. Added Schematic layout.</td>
<td>5/16/05</td>
</tr>
<tr>
<td>B</td>
<td>T9</td>
<td>15</td>
<td>Ordering Information - removed leaded parts. Removed ICS from ordering part number. Removed 2500 on tape and reel shipping information. Removed lead free note.</td>
<td>12/3/15</td>
</tr>
<tr>
<td>C</td>
<td></td>
<td>3 13 14 15 16</td>
<td>Corrected Figure 1, Enable Timing Diagram. Applications Information Section: Deleted Crystal Input Interface application note, see Layout Guideline Added LVCMOS to XTAL Interface application note Added VFQFN EPAD Thermal Release Path application note Added Recommendations for Unused Input and Output Pins application note Updated Layout Guideline, adding crystal interface Added Power Considerations section. Updated datasheet header/footer and format.</td>
<td>9/28/16</td>
</tr>
</tbody>
</table>
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(Rev.4.0-1 November 2017)

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