**GENERAL DESCRIPTION**

The ICS843241 is a low jitter, high performance clock generator and a member of the FemtoClocks™ family of silicon timing products. The ICS843241 is designed for use in the SAS-2 interconnect and the three transport protocols that use the SAS-2 interconnect: Serial SCSI Protocol (SSP), Serial ATA Tunneled Protocol (STP), and Serial Management Protocol (SMP). The ICS843241 has excellent (<1ps) RMS phase jitter, over the SAS defined integration range. The ICS843241 uses an external, 25MHz, parallel resonant crystal to generate three selectable output frequencies: 75MHz, 100MHz, 150MHz, and 300MHz. This silicon based approach provides excellent frequency stability and reliability. The ICS843241 features up, down, and center spread spectrum (SSC) clocking techniques. The up, down and center SSC will be required in the SAS-2 applications that have three clock trees in the HBA and expander ASICs (see Applications Information section, Figure 3).

**APPLICATIONS:**

- SAS/ SATA Host Bus Adapters
- SATA Port Multipliers
- SAS I/O Controllers
- TapeDrive and HDD Array Controllers
- SAS Edge and Fanout Expanders
- HDDs and Tape Drives
- Disk Storage Enterprise

**FEATURES**

- Designed for use in SAS-2 systems
- Up, down and center spread spectrum clocking
- One differential 3.3V or 2.5V LVPECL output pair
- Selectable output frequencies: 75MHz, 100MHz, 150MHz, 300MHz
- RMS phase jitter @ 75MHz, (900kHz – 7.5MHz): 0.70ps (typical)
- 3.3V or 2.5V operating supply
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

**ADDITIONAL ORDERING INFORMATION TABLE**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Package</th>
<th>Output Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICS843241BG</td>
<td>16 TSSOP</td>
<td>75MHz, 100MHz, 150MHz, 300MHz</td>
</tr>
<tr>
<td>ICS843241BM-75</td>
<td>8 SOIC</td>
<td>75MHz</td>
</tr>
<tr>
<td>ICS843241BM-100</td>
<td>8 SOIC</td>
<td>100MHz</td>
</tr>
<tr>
<td>ICS843241BM-150</td>
<td>8 SOIC</td>
<td>150MHz</td>
</tr>
<tr>
<td>ICS843241BM-300</td>
<td>8 SOIC</td>
<td>300MHz</td>
</tr>
</tbody>
</table>

**PIN ASSIGNMENT**

ICS843241-XXX
8-Lead SOIC, 150 mil
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

<table>
<thead>
<tr>
<th>Pin Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTL_IN</td>
</tr>
<tr>
<td>XTL_OUT</td>
</tr>
<tr>
<td>SSC_SEL0</td>
</tr>
<tr>
<td>SSC_SEL1</td>
</tr>
<tr>
<td>F_SEL1</td>
</tr>
<tr>
<td>Vcc</td>
</tr>
<tr>
<td>VEE</td>
</tr>
</tbody>
</table>

ICS843241
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

<table>
<thead>
<tr>
<th>Pin Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vcc</td>
</tr>
<tr>
<td>XTL_IN</td>
</tr>
<tr>
<td>XTL_OUT</td>
</tr>
<tr>
<td>SSC_SEL0</td>
</tr>
<tr>
<td>SSC_SEL1</td>
</tr>
<tr>
<td>F_SEL1</td>
</tr>
<tr>
<td>nPLL_SEL</td>
</tr>
<tr>
<td>F_SEL1</td>
</tr>
<tr>
<td>nQ</td>
</tr>
<tr>
<td>Q</td>
</tr>
<tr>
<td>Vcc</td>
</tr>
<tr>
<td>VEE</td>
</tr>
</tbody>
</table>
### Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XTAL_OUT, XTAL_IN</td>
<td>Input</td>
<td>Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.</td>
</tr>
<tr>
<td>SSC_SEL0, SSC_SEL1</td>
<td>Input Pulldown</td>
<td>SSC select pins. See Table 3A. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>F_SEL0</td>
<td>Input Pulldown</td>
<td>Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>F_SEL1</td>
<td>Input Pullup</td>
<td>Output frequency select pin. See Table 3B. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>nPLL_SEL</td>
<td>Input Pulldown</td>
<td>Bypasses the PLL. LVCMOS/LVTTL interface levels.</td>
</tr>
<tr>
<td>nQ, Q</td>
<td>Output Pulldown</td>
<td>Differential clock outputs. LVPECL interface levels.</td>
</tr>
<tr>
<td>VEE</td>
<td>Power</td>
<td>Negative supply pin.</td>
</tr>
<tr>
<td>VCC</td>
<td>Power</td>
<td>Power supply pin.</td>
</tr>
<tr>
<td>nc</td>
<td>Unused</td>
<td>No connect.</td>
</tr>
</tbody>
</table>

### Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_in</td>
<td>Input Capacitance</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_pulldown</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R_pullup</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

### Table 3A. SSC_SEL[1:0] Function Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSC_SEL1</td>
<td>SSC_SEL0</td>
</tr>
<tr>
<td>0 (default)</td>
<td>0 (default)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

### Table 3B. F_SEL[1:0] Function Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>F_SEL1</td>
<td>F_SEL0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1 (default)</td>
<td>0 (default)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{cc}$ 4.6V

Inputs, $V_i$ -0.5V to $V_{cc} + 0.5V$

Outputs, $I_o$

Continuous Current 50mA

Surge Current 100mA

Package Thermal Impedance, $\theta_{JA}$
8 SOIC 96°C/W (0 lfpm)
16 TSSOP 92.4°C/W (0 mps)

Storage Temperature, $T_{STG}$ -65°C to 150°C

**NOTE:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{cc} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO 70$^\circ C$**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{cc}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td></td>
<td></td>
<td>77</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{cc} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO 70$^\circ C$**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{cc}$</td>
<td>Power Supply Voltage</td>
<td></td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td></td>
<td></td>
<td>75</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{cc} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ C$ TO 70$^\circ C$**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{cc} = 3.3V$</td>
<td>2</td>
<td>$V_{cc} + 0.3$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{cc} = 2.5V$</td>
<td>1.7</td>
<td>$V_{cc} + 0.3$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{cc} = 3.3V$</td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{cc} = 2.5V$</td>
<td>-0.3</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>$F_SEL0,$</td>
<td>150</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$nPLL_SEL$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$SSC_SEL[0:1]$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$F_SEL0,$</td>
<td>-5</td>
<td></td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$nPLL_SEL$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$SSC_SEL[0:1]$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** $V_{cc} = 3.465V$ or $2.625V$
### TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = 3.3V\pm5\%$, $TA = 0^\circ C$ TO 70$^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>$V_{CC} - 1.4$</td>
<td>$V_{CC} - 0.9$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>$V_{CC} - 2.0$</td>
<td>$V_{CC} - 1.7$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{SWING}$</td>
<td>Peak-to-Peak Output Voltage Swing</td>
<td>0.6</td>
<td>1.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE 1:** Outputs terminated with $50\Omega$ to $V_{CC} - 2V$.

### TABLE 4E. LVPECL DC CHARACTERISTICS, $V_{CC} = 2.5V\pm5\%$, $TA = 0^\circ C$ TO 70$^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output High Voltage; NOTE 1</td>
<td>$V_{CC} - 1.4$</td>
<td>$V_{CC} - 0.9$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Low Voltage; NOTE 1</td>
<td>$V_{CC} - 2.0$</td>
<td>$V_{CC} - 1.5$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{SWING}$</td>
<td>Peak-to-Peak Output Voltage Swing</td>
<td>0.4</td>
<td>1.0</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE 1:** Outputs terminated with $50\Omega$ to $V_{CC} - 2V$.

### TABLE 5. CRYSTAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode of Oscillation</td>
<td>Fundamental</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Equivalent Series Resistance (ESR)</td>
<td>50</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Shunt Capacitance</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

### TABLE 6A. AC CHARACTERISTICS, $V_{CC} = 3.3V\pm5\%$, $TA = 0^\circ C$ TO 70$^\circ C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{out}$</td>
<td>Output Frequency</td>
<td>$F_{SEL[1:0]} = 00$</td>
<td>75</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$F_{SEL[1:0]} = 01$</td>
<td>100</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$F_{SEL[1:0]} = 10$</td>
<td>150</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$F_{SEL[1:0]} = 11$</td>
<td>300</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$f_{jitter}$</td>
<td>RMS Phase Jitter ( Random); NOTE 1</td>
<td>75MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.70</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.69</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>150MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.69</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td></td>
<td></td>
<td>300MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.68</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_r$</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>335</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_d$</td>
<td>Output Duty Cycle</td>
<td>48</td>
<td>52</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

**NOTE 1:** Refer to the Phase Noise Plots.
### Table 6B. AC Characteristics, $V_{cc} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{out}$</td>
<td>Output Frequency</td>
<td>$F_{SEL}[1:0] = 00$</td>
<td>75</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$F_{SEL}[1:0] = 01$</td>
<td>100</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$F_{SEL}[1:0] = 10$</td>
<td>150</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$F_{SEL}[1:0] = 11$</td>
<td>300</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f_{j\it{(O)}}$</td>
<td>RMS Phase Jitter (Random); NOTE 1</td>
<td>75MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.72</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.61</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>150MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.68</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>300MHz @ Integration Range: 900kHz - 7.5MHz</td>
<td>0.64</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_{r}$ / $t_{f}$</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>360</td>
<td>ps</td>
<td>500</td>
<td></td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td>48</td>
<td>%</td>
<td>52</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE 1: Refer to the Phase Noise Plots.
Typical Phase Noise at 75MHz (3.3V)

RMS Phase Jitter (Random)
900kHz to 7.5MHz = 0.70ps (typical)

Phase Noise Result by adding a SATA/SAS Filter to raw data

Raw Phase Noise Data

SATA/SAS Jitter Filter
**Typical Phase Noise at 300MHz (3.3V)**

- **RMS Phase Jitter (Random)**
  - 900kHz to 7.5MHz = 0.68ps (typical)

---

**Offset Frequency (Hz)**

- **Noise Power (dBc/Hz)**
  - Various levels ranging from -100 to -190 dBc/Hz

---

**Graph Details**

- **Raw Phase Noise Data**
  - Line representing raw phase noise data.

- **Phase Noise Result by adding a SATA/SAS Filter to raw data**
  - Line showing the effect of adding a SATA/SAS filter to the raw data.

---

**SATA/SAS Jitter Filter**

300MHz

- **RMS Phase Jitter (Random)**
  - 900kHz to 7.5MHz = 0.68ps (typical)
PARAMETER MEASUREMENT INFORMATION

3.3V OUTPUT LOAD AC TEST CIRCUIT

2.5V OUTPUT LOAD AC TEST CIRCUIT

OUTPUT RISE/FALL TIME

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

RMS PHASE JITTER

RMS Jitter = \sqrt{\text{Area Under the Masked Phase Noise Plot}}
APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

The ICS843241 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in Figure 1 below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

![Figure 1. Crystal Input Interface](image)

LVCMOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in Figure 2. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

![Figure 2. General Diagram for LVCMOS Driver to XTAL Input Interface](image)
**RECOMMENDATIONS FOR UNUSED INPUT PINS**

**INPUTS:**

**LVCMOS Control Pins**
All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

**TERMINATION FOR 3.3V LVPECL OUTPUTS**

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 3A and 3B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

**Figure 3A. LVPECL Output Termination**

**Figure 3B. LVPECL Output Termination**
**Termination for 2.5V LVPECL Outputs**

*Figure 4A* and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to \( V_{cc} - 2V \). For \( V_{cc} = 2.5V \), the \( V_{cc} - 2V \) is very close to ground level. The R3 in *Figure 4B* can be eliminated and the termination is shown in *Figure 4C*.

---

**Figure 4A. 2.5V LVPECL Driver Termination Example**

- VCC = 2.5V
- Zo = 50 Ohm
- 2.5V LVPECL Driver
- R1 250
- R2 62.5
- R3 250
- R4 62.5

**Figure 4B. 2.5V LVPECL Driver Termination Example**

- VCC = 2.5V
- Zo = 50 Ohm
- 2.5V LVPECL Driver
- R1 50
- R2 50
- R3 18

**Figure 4C. 2.5V LVPECL Termination Example**

- VCC = 2.5V
- Zo = 50 Ohm
- 2.5V LVPECL Driver
- R1 50
- R2 50
**Schematic Example**

*Figure 5 shows an example of ICS843241 application schematic.*

In this example, the device is operated at \( V_{CC} = 3.3 \text{V} \). The 18pF parallel resonant 25MHz crystal is used. The \( C_1 = 27 \text{pF} \) and \( C_2 = 27 \text{pF} \) are recommended for frequency accuracy. For different board layout, the \( C_1 \) and \( C_2 \) may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL termination are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

---

**Figure 5. ICS843241 Schematic Example**
**POWER CONSIDERATIONS**

This section provides information on power dissipation and junction temperature for the ICS843241. Equations and example calculations are also provided.

1. **Power Dissipation.**
   The total power dissipation for the ICS843241 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for \( V_{CC} = 3.3V + 5\% = 3.465V \), which gives worst case results.

   **NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

   - Power (core) \(_{MAX}\) = \( V_{CC,MAX} \times I_{EE,MAX} = 3.465V \times 77mA = 266.8mW \)
   - Power (outputs) \(_{MAX}\) = 30mW/Loaded Output pair

   **Total Power \(_{MAX}\)** (3.465V, with all outputs switching) = 266.8mW + 30mW = 296.8mW

2. **Junction Temperature.**
   Junction temperature, \( T_j \), is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

   The equation for \( T_j \) is as follows: \( T_j = \theta_{JA} \times Pd_{total} + T_A \)
   \( T_{j} = \) Junction Temperature
   \( \theta_{JA} = \) Junction-to-Ambient Thermal Resistance
   \( Pd_{total} = \) Total Device Power Dissipation (example calculation is in section 1 above)
   \( T_A = \) Ambient Temperature

   In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \( \theta_{ja} \) must be used. Assuming no air flow and a multi-layer board, the appropriate value is 96°C/W per Table 7B below.

   Therefore, \( T_j \) for an ambient temperature of 70°C with all outputs switching is:
   \( 70°C + 0.297W \times 96°C/W = 97.6°C \). This is well below the limit of 125°C.

   This calculation is only an example. \( T_j \) will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board.

   **TABLE 7A. \( \theta_{JA} \) VS. AIR FLOW TABLE FOR 16 LEAD TSSOP**

<table>
<thead>
<tr>
<th>( \theta_{JA} ) by Velocity (Meters per Second)</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>92.4°C/W</td>
<td>88.0°C/W</td>
<td>85.9°C/W</td>
</tr>
</tbody>
</table>

   **TABLE 7B. \( \theta_{JA} \) VS. AIR FLOW TABLE FOR 8 LEAD SOIC**

<table>
<thead>
<tr>
<th>( \theta_{JA} ) by Velocity (Linear Feet per Minute)</th>
<th>0</th>
<th>200</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>96°C/W</td>
<td>87°C/W</td>
<td>82°C/W</td>
</tr>
</tbody>
</table>
3. Calculations and Equations.
The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 6.

**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of \( V_{CC} - 2V \).

- For logic high, \( V_{OUT} = V_{OH\_MAX} = V_{CC\_MAX} - 0.9V \)
  \( (V_{CC\_MAX} - V_{OH\_MAX}) = 0.9V \)

- For logic low, \( V_{OUT} = V_{OL\_MAX} = V_{CC\_MAX} - 1.7V \)
  \( (V_{CC\_MAX} - V_{OL\_MAX}) = 1.7V \)

\( Pd_{H} \) is power dissipation when the output drives high.
\( Pd_{L} \) is the power dissipation when the output drives low.

\[
Pd_{H} = \frac{(2V - (V_{CC\_MAX} - V_{OH\_MAX}))}{R_L} \times (V_{CC\_MAX} - V_{OH\_MAX}) = \frac{19.8}{50}\Omega \times 0.9V = 19.8mW
\]

\[
Pd_{L} = \frac{(2V - (V_{CC\_MAX} - V_{OL\_MAX}))}{R_L} \times (V_{CC\_MAX} - V_{OL\_MAX}) = \frac{10.2}{50}\Omega \times 1.7V = 10.2mW
\]

Total Power Dissipation per output pair = \( Pd_{H} + Pd_{L} = 30mW \)
RELIABILITY INFORMATION

TABLE 8A. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 8 LEAD SOIC

<table>
<thead>
<tr>
<th>$\theta_{JA}$ by Velocity (Linear Feet per Minute)</th>
<th>0</th>
<th>200</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>96°C/W</td>
<td>87°C/W</td>
<td>82°C/W</td>
</tr>
</tbody>
</table>

TABLE 8B. $\theta_{JA}$ VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

<table>
<thead>
<tr>
<th>$\theta_{JA}$ by Velocity (Meters per Second)</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>92.4°C/W</td>
<td>88.0°C/W</td>
<td>85.9°C/W</td>
</tr>
</tbody>
</table>

TRANSISTOR COUNT
The transistor count for ICS843241 is: 2986
TABLE 9A. 8 LEAD SOIC PACKAGE DIMENSIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>Millimeters</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>1.35</td>
<td>1.75</td>
</tr>
<tr>
<td>A1</td>
<td></td>
<td>0.10</td>
<td>0.25</td>
</tr>
<tr>
<td>B</td>
<td></td>
<td>0.33</td>
<td>0.51</td>
</tr>
<tr>
<td>C</td>
<td></td>
<td>0.19</td>
<td>0.25</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>4.80</td>
<td>5.00</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>3.80</td>
<td>4.00</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>1.27</td>
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</tr>
<tr>
<td>H</td>
<td></td>
<td>5.80</td>
<td>6.20</td>
</tr>
<tr>
<td>h</td>
<td></td>
<td>0.25</td>
<td>0.50</td>
</tr>
<tr>
<td>L</td>
<td></td>
<td>0.40</td>
<td>1.27</td>
</tr>
<tr>
<td>α</td>
<td></td>
<td>0°</td>
<td>8°</td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MS-012

TABLE 9B. 16 LEAD TSSOP PACKAGE DIMENSIONS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>Millimeters</th>
<th>MINIMUM</th>
<th>MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td></td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>--</td>
<td>1.20</td>
</tr>
<tr>
<td>A1</td>
<td></td>
<td>0.05</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td></td>
<td>0.80</td>
<td>1.05</td>
</tr>
<tr>
<td>b</td>
<td></td>
<td>0.19</td>
<td>0.30</td>
</tr>
<tr>
<td>c</td>
<td></td>
<td>0.09</td>
<td>0.20</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>4.90</td>
<td>5.10</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td>6.40</td>
<td>BASIC</td>
</tr>
<tr>
<td>E1</td>
<td></td>
<td>4.30</td>
<td>4.50</td>
</tr>
<tr>
<td>e</td>
<td></td>
<td>0.65</td>
<td>BASIC</td>
</tr>
<tr>
<td>L</td>
<td></td>
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<td>8°</td>
</tr>
<tr>
<td>aaa</td>
<td></td>
<td>--</td>
<td>0.10</td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MO-153
### Table 10. Ordering Information

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICS843241BGLF</td>
<td>843241BL</td>
<td>16 Lead &quot;Lead-Free&quot; TSSOP</td>
<td>tube</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BGLFT</td>
<td>843241BL</td>
<td>16 Lead &quot;Lead-Free&quot; TSSOP</td>
<td>2500 tape &amp; reel</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-75LF</td>
<td>3241B75L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>tube</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-75LFT</td>
<td>3241B75L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>2500 tape &amp; reel</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-100LF</td>
<td>241B100L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>tube</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-100LFT</td>
<td>241B100L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>2500 tape &amp; reel</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-150LF</td>
<td>241B150L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>tube</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-150LFT</td>
<td>241B150L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>2500 tape &amp; reel</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-300LF</td>
<td>241B300L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>tube</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>ICS843241BM-300LFT</td>
<td>241B300L</td>
<td>8 Lead &quot;Lead-Free&quot; SOIC</td>
<td>2500 tape &amp; reel</td>
<td>0°C to 70°C</td>
</tr>
</tbody>
</table>

**NOTE:** Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
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