**GENERAL DESCRIPTION**

The 844021I-01 is an Ethernet Clock Generator. The 844021I-01 uses an 18pF parallel resonant crystal over the range of 24.5MHz – 34MHz. For Ethernet applications, a 25MHz crystal is used. The 844021I-01 has excellent <1ps phase jitter performance, over the 1.875MHz – 20MHz integration range. The 844021I-01 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

**FEATURES**

- One Differential LVDS output
- Crystal oscillator interface, 18pF parallel resonant crystal (24.5MHz – 34MHz)
- Output frequency range: 122.5MHz – 170MHz
- VCO range: 490MHz – 680MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.32ps (typical) @ 3.3V
- 3.3V or 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

---

**COMMON CONFIGURATION TABLE - Gb ETHERNET**

<table>
<thead>
<tr>
<th>Crystal Frequency (MHz)</th>
<th>M</th>
<th>N</th>
<th>Multiplication Value M/N</th>
<th>Output Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>20</td>
<td>4</td>
<td>5</td>
<td>125</td>
</tr>
<tr>
<td>26.666</td>
<td>20</td>
<td>4</td>
<td>5</td>
<td>133.33</td>
</tr>
<tr>
<td>33.33</td>
<td>20</td>
<td>4</td>
<td>5</td>
<td>166.66</td>
</tr>
</tbody>
</table>

**BLOCK DIAGRAM**

**PIN ASSIGNMENT**

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm package body
G Package
Top View
TABLE 1. PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Power</td>
<td>Analog supply pin.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>3, 4</td>
<td>XTAL_OUT, XTAL_IN</td>
<td>Input</td>
<td>Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.</td>
</tr>
<tr>
<td>5</td>
<td>OE</td>
<td>Input</td>
<td>Pullup Output enable pin. When HIGH, Q/nQ output is active. When LOW, the Q/nQ output is in a high impedance state. LVCMOS/LVT-TL interface levels.</td>
</tr>
<tr>
<td>6, 7</td>
<td>nQ, Q</td>
<td>Output</td>
<td>Differential clock outputs. LVDS interface levels.</td>
</tr>
<tr>
<td>8</td>
<td>VDD</td>
<td>Power</td>
<td>Core supply pin.</td>
</tr>
</tbody>
</table>

NOTE: Pulup refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_IN</td>
<td>Input Capacitance</td>
<td></td>
<td>4</td>
<td>4</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>51</td>
<td>51</td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{DD}$</td>
<td></td>
<td>4.6V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inputs, $V_i$</td>
<td>-0.5V to $V_{DD} + 0.5$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outputs, $I_O$ (LVDS)</td>
<td>Continuous Current</td>
<td>10mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Surge Current</td>
<td>15mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_J$</td>
<td></td>
<td>129.5°C/W (0 mps)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 3A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Core Supply Voltage</td>
<td>$V_{DD} = 3.3V$</td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>Analog Supply Voltage</td>
<td>$V_{DD} - 0.10$</td>
<td>3.3</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td>$V_{DD} = 3.3V$</td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{DDA}$</td>
<td>Analog Supply Current</td>
<td>$V_{DD} = 3.3V$</td>
<td>-0.3</td>
<td>0.7</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

TABLE 3B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Core Supply Voltage</td>
<td>$V_{DD} = 2.5V$</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DDA}$</td>
<td>Analog Supply Voltage</td>
<td>$V_{DD} - 0.10$</td>
<td>2.5</td>
<td>$V_{DD}$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td>$V_{DD} = 2.5V$</td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DDA}$</td>
<td>Analog Supply Current</td>
<td>$V_{DD} = 2.5V$</td>
<td>-0.3</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

TABLE 3C. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = -40°C$ TO $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{DD} = 3.3V$</td>
<td>2</td>
<td>$V_{DD} + 0.3$</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V$</td>
<td>1.7</td>
<td>$V_{DD} + 0.3$</td>
<td>$V_{DD}$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{DD} = 3.3V$</td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DD} = 2.5V$</td>
<td>-0.3</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>$V_{DD} = V_{IH} = 3.465V$ or $2.625V$</td>
<td>5</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$V_{DD} = 3.465V$ or $2.625V, V_{IH} = 0V$</td>
<td>-150</td>
<td></td>
<td></td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>
### Table 3D. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40°C$ to $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OD}$</td>
<td>Differential Output Voltage</td>
<td></td>
<td>215</td>
<td>430</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{OD}$</td>
<td>$V_{OD}$ Magnitude Change</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Offset Voltage</td>
<td></td>
<td>1.05</td>
<td>1.45</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{OS}$</td>
<td>$V_{OS}$ Magnitude Change</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

NOTE: Please refer to Parameter Measurement Information for output information.

### Table 3E. LVDS DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OD}$</td>
<td>Differential Output Voltage</td>
<td></td>
<td>275</td>
<td>425</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{OD}$</td>
<td>$V_{OD}$ Magnitude Change</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Offset Voltage</td>
<td></td>
<td>1.15</td>
<td>1.45</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{OS}$</td>
<td>$V_{OS}$ Magnitude Change</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

NOTE: Please refer to Parameter Measurement Information for output information.

### Table 4. Crystal Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode of Oscillation</td>
<td>Fundamental</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>24.5</td>
<td>34</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Equivalent Series Resistance (ESR)</td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Shunt Capacitance</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

NOTE: It is not recommended to overdrive the crystal input with an external clock.

### Table 5. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{OUT}}$</td>
<td>Output Frequency</td>
<td>122.5</td>
<td>170</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{\text{jit}(\Omega)}$</td>
<td>RMS Phase Jitter (Random); NOTE 1</td>
<td>125MHz @ Integration Range: 1.875MHz - 20MHz</td>
<td>0.32</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>$t_{\text{R}} / t_{\text{F}}$</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80%</td>
<td>200</td>
<td>400</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>odc</td>
<td>Output Duty Cycle</td>
<td>48</td>
<td>52</td>
<td></td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

NOTE 1: Please refer to the Phase Noise Plots following this section.
Typical Phase Noise at 125MHz @ 3.3V

- RMS Phase Jitter (Random) 1.875MHz to 20MHz = 0.32ps (typical)

Typical Phase Noise at 125MHz @ 2.5V

- RMS Phase Jitter (Random) 1.875MHz to 20MHz = 0.32ps (typical)
PARAMETER MEASUREMENT INFORMATION

LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT

LVDS 2.5V OUTPUT LOAD AC TEST CIRCUIT

RMS PHASE JITTER

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

OUTPUT RISE/FALL TIME

OFFSET VOLTAGE SETUP

DIFFERENTIAL OUTPUT VOLTAGE SETUP
APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES
As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844021I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_DD and V_DDA should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. Figure 1 illustrates this for a generic V_DD pin and also shows that V_DDA requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_DDA pin.

CRYSTAL INPUT INTERFACE
The 844021I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in Figure 2 below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.
3.3V, 2.5V LVDS DRIVER TERMINATION

A general LVDS interface is shown in Figure 4 in a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

**Figure 4. Typical LVDS Driver Termination**
**SCHEMATIC LAYOUT**

*Figure 5 shows an example of 844021I-01 application schematic.* In this example, the device is operated at $V_{DD} = 3.3\, \text{V}$. The decoupling capacitor should be located as close as possible to the power pin. The 18pF parallel resonant 25MHz crystal is used. The $C_1 = 33\, \text{pF}$ and $C_2 = 27\, \text{pF}$ are recommended for frequency accuracy. For different board layout, the $C_1$ and $C_2$ may be slightly adjusted for optimizing frequency accuracy. For the LVDS output drivers, place a $100\, \Omega$ resistor as close to the receiver as possible.

![Schematic Layout](image)

**Figure 5. 844021I-01 Schematic Layout**
POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 844021I-01. Equations and example calculations are also provided.

1. Power Dissipation.
   The total power dissipation for the 844021I-01 is the sum of the core power plus the analog plus the power dissipated in the load(s). The following is the power dissipation for \( V_{DD} = 3.3V + 5\% = 3.465V \), which gives worst case results.

   \[ \text{Power (core)}_{\text{MAX}} = V_{DD_{\text{MAX}}} \times (I_{DD_{\text{MAX}}} + I_{DA_{\text{MAX}}}) = 3.465V \times (75mA + 10mA) = 294.5mW \]

2. Junction Temperature.
   Junction temperature, \( T_j \), is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

   \( T_j = \theta_{JA} \times Pd_{\text{total}} + T_a \)

   \( \theta_{JA} = \text{Junction-to-Ambient Thermal Resistance} \)

   \( Pd_{\text{total}} = \text{Total Device Power Dissipation (example calculation is in section 1 above)} \)

   \( T_a = \text{Ambient Temperature} \)

   In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \( \theta_{JA} \) must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 6 below.

   Therefore, \( T_j \) for an ambient temperature of 85°C with all outputs switching is:

   \[ 85°C + 0.295W \times 129.5°C/W = 123.2°C \]

   This is below the limit of 125°C.

   This calculation is only an example. \( T_j \) will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

### Table 6. Thermal Resistance \( \theta_{JA} \) for 8-Lead TSSOP, Forced Convection

<table>
<thead>
<tr>
<th>( \theta_{JA} ) by Velocity (Meters per Second)</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>129.5°C/W</td>
<td>125.5°C/W</td>
<td>123.5°C/W</td>
</tr>
</tbody>
</table>
RELIABILITY INFORMATION

**Table 7. \( \theta_{JA} \) vs. Air Flow Table for 8 Lead TSSOP**

<table>
<thead>
<tr>
<th>( \theta_{JA} ) by Velocity (Meters per Second)</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>129.5°C/W</td>
<td>125.5°C/W</td>
<td>123.5°C/W</td>
</tr>
</tbody>
</table>

**Transistor Count**

The transistor count for 844021I-01 is: 2533

PACKAGE OUTLINE & DIMENSIONS

**Package Outline - G Suffix for 8 Lead TSSOP**

**Table 8. Package Dimensions**

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>--</td>
<td>1.20</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>0.80</td>
<td>1.05</td>
</tr>
<tr>
<td>b</td>
<td>0.19</td>
<td>0.30</td>
</tr>
<tr>
<td>c</td>
<td>0.09</td>
<td>0.20</td>
</tr>
<tr>
<td>D</td>
<td>2.90</td>
<td>3.10</td>
</tr>
<tr>
<td>E</td>
<td>6.40 BASIC</td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>4.30</td>
<td>4.50</td>
</tr>
<tr>
<td>e</td>
<td>0.65 BASIC</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.75</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>0°</td>
<td>8°</td>
</tr>
<tr>
<td>aaa</td>
<td>--</td>
<td>0.10</td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MO-153
### TABLE 9. ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICS844021BGI-01LF</td>
<td>BI01L</td>
<td>8 lead “Lead-Free” TSSOP</td>
<td>tube</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>ICS844021BGI-01LFT</td>
<td>BI01L</td>
<td>8 lead “Lead-Free” TSSOP</td>
<td>tape &amp; reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>

NOTE: Parts that are ordered with an “LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.
## REVISION HISTORY SHEET

<table>
<thead>
<tr>
<th>Rev</th>
<th>Table</th>
<th>Page</th>
<th>Description of Change</th>
<th>Date</th>
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<td>T4</td>
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<td>Crystal Characteristics Table - added note.</td>
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<td>Deleted application note, LVCMOS to XTAL Interface.</td>
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<td>Deleted quantity from tape and reel.</td>
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<td>A</td>
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<td>Ordering Information - removed leaded devices.</td>
<td>10/27/15</td>
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<td>Updated data sheet format.</td>
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