Low Skew, 1-to-4, Crystal Oscillator/ Differential-to-3.3V LVPECL Fanout Buffer

8533-11

DATA SHEET

General Description

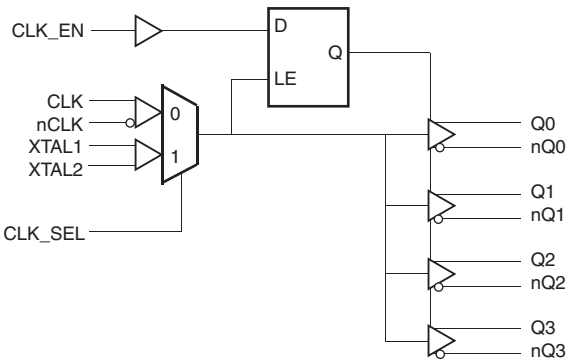
The 8533-11 is a low skew, high performance 1-to-4 Crystal Oscillator/Differential-to-3.3V LVPECL fanout buffer. The 8533-11 has selectable differential clock or crystal inputs. The CLK, nCLK pair can accept most standard differential input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the 8533-11 ideal for those applications demanding well defined performance and repeatability.

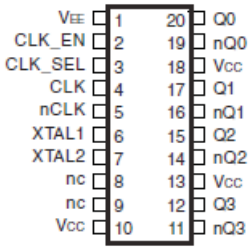
Features

- 4 differential 3.3V LVPECL outputs
- Selectable differential CLK, nCLK or crystal inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to 3.3V LVPECL levels with resistor bias on nCLK input
- Output skew: 30ps (maximum)
- Part-to-part skew: 150ps (maximum)
- Propagation delay: 2ns (maximum)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Lead-Free package fully RoHS compliant

Block Diagram



Pin Assignment



8533-11
20-Lead TSSOP
6.5mm x 4.4mm x 0.92 package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When LOW, selects CLK, nCLK input. When HIGH, selects XTAL input. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	XTAL1	Input	Pulldown	Crystal oscillator input.
7	XTAL2	Input	Pullup	Crystal oscillator input.
8, 9	nc	Unused		No connect.
10, 13, 18	V_{CC}	Power		Positive supply pins.
11, 12	nQ3, Q3	Output		Differential clock outputs. LVPECL interface levels.
14, 15	nQ2, Q2	Output		Differential clock outputs. LVPECL interface levels.
16, 17	nQ1, Q1	Output		Differential clock outputs. LVPECL interface levels.
19, 20	nQ0, Q0	Output		Differential clock outputs. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
CLK_EN	CLK_SEL	Selected Source	Q0:Q3	nQ0:nQ3
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	XTAL1, XTAL2	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	XTAL1, XTAL2	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled folowing a rising and falling input clock or crystal oscillator edge as shown in *Figure 1*.
In the active mode, the state of the outputs are a function of the CLK, nCLK and XTAL1, XTAL2 inputs as described in Table 3B.

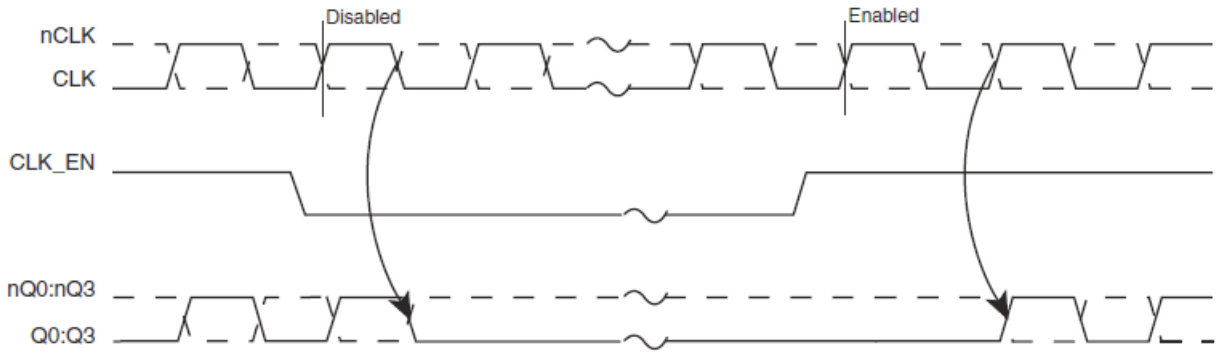


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
CLK	nCLK	Q0:Q3	nQ0:nQ3		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, “Wiring the Differential Input to Accept Single Ended Levels”.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Power Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				50	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	CLK_EN, CLK_SEL		2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	CLK_EN, CLK_SEL		-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	$V_{IN} = V_{CC} = 3.465V$			5	µA
		CLK_SEL	$V_{IN} = V_{CC} = 3.465V$			150	µA
I_{IL}	Input Low Current	CLK_EN	$V_{IN} = 0V, V_{CC} = 3.465V$	-150			µA
		CLK_SEL	$V_{IN} = 0V, V_{CC} = 3.465V$	-5			µA

Table 4C. Differential DC Characteristics, V_{CC} = 3.3V±5%, TA = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	$V_{CC} = V_{IN} = 3.465V$			5	µA
		CLK	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	nCLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-150			µA
		CLK	$V_{CC} = 3.465V, V_{IN} = 0V$	-5			µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			V_{EE} + 0.5		V_{CC} - 0.85	V

NOTE1: For single ended applications the maximum input voltage for CLK and nCLK is V_{CC} + 0.3V.
NOTE 2: Common mode voltage is defined as V_{IH}.

TABLE 4D. LVPECL DC CHARACTERISTICS, V_{CC} = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CC} - 1.4		V_{CC} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CC} - 2.0		V_{CC} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.

TABLE 5. CRYSTAL CHARACTERISTICS

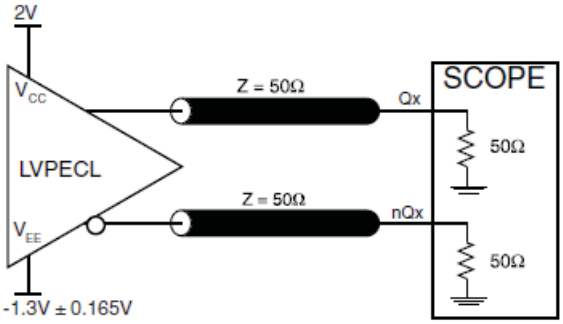
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		14		25	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

TABLE 6. AC CHARACTERISTICS, V_{CC} = 3.3V±5%, T_A = 0°C TO 70°C

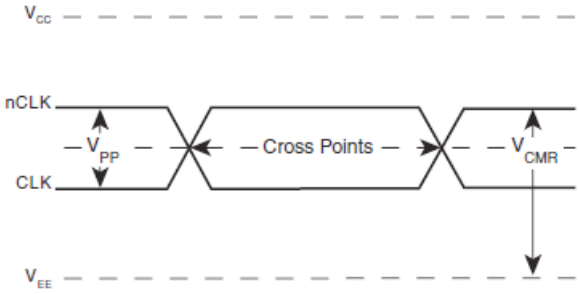
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				650	MHz
t_{PD}	Propagation Delay; NOTE 1	$f \leq$ 650MHz	1.0		2.0	ns
tsk(o)	Output Skew; NOTE 2, 5				30	ps
tsk(pp)	Part-to-Part Skew; NOTE 3, 5				150	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle; NOTE 4		47	50	53	%

All parameters measured at 500MHz unless noted otherwise.
The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: Measured using CLK. For XTAL input, refer to Application Note.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

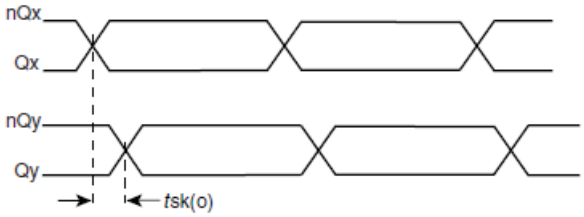
PARAMETER MEASUREMENT INFORMATION



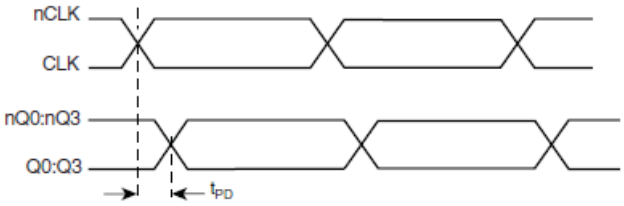
3.3V OUTPUT LOAD AC TEST CIRCUIT



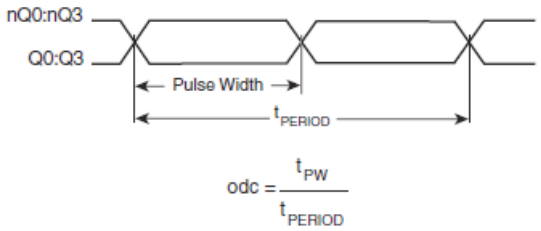
DIFFERENTIAL INPUT LEVEL



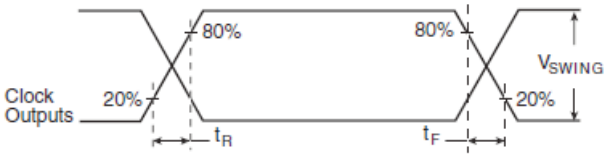
OUTPUT SKEW



PROPAGATION DELAY



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF ≃ V_{CC}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

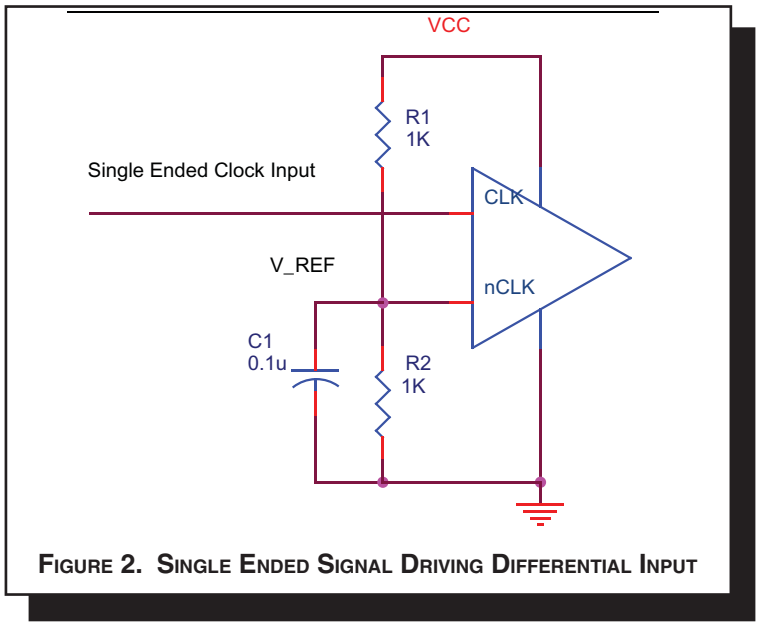


Figure 2. Single Ended Signal Driving Differential Input

Termination for LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

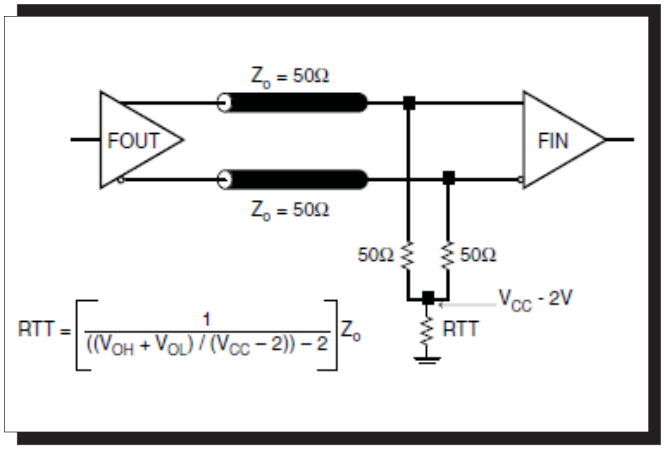


Figure 3A. LVPECL Output Termination

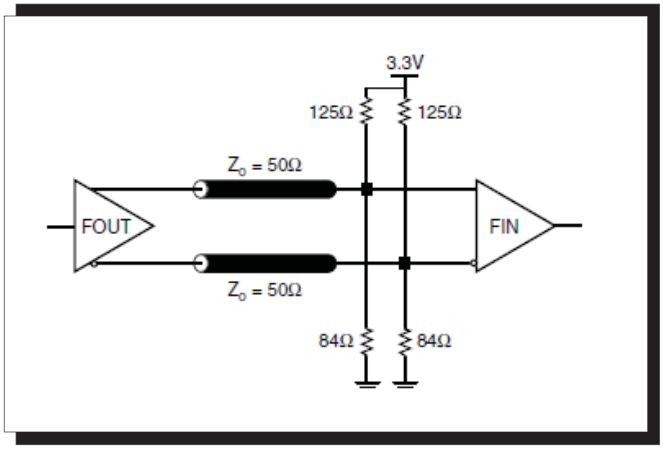


Figure 3B. LVPECL Output Termination

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4E show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

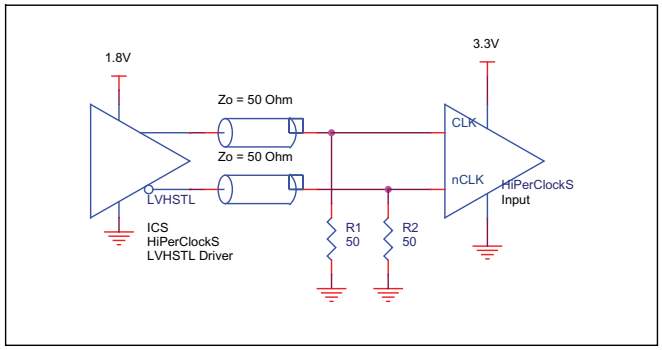


Figure 4A. HiPerClockS CLK/nCLK Input Driven by ICS HiPerClockS LVHSTL Driver

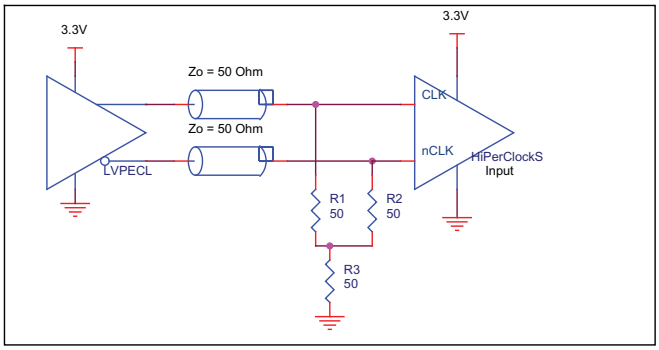


Figure 4B. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

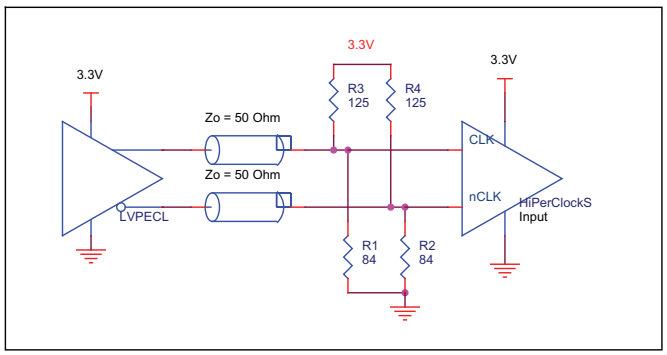


Figure 4C. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver

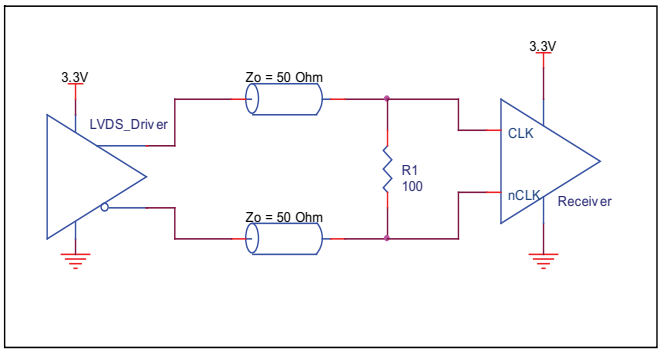


Figure 4D. HiPerClockS CLK/nCLK Input Driven by 3.3V LVDS Driver

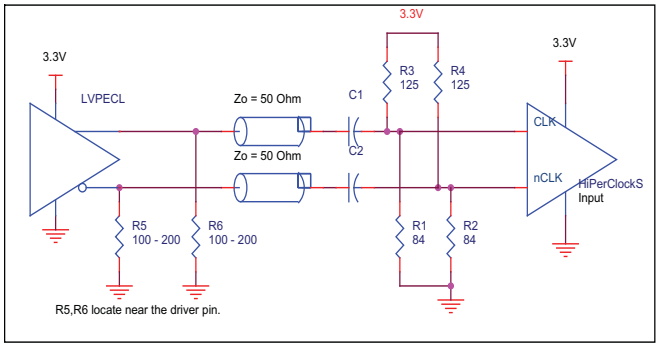


Figure 4E. HiPerClockS CLK/nCLK Input Driven by 3.3V LVPECL Driver with AC Couple

Crystal Input Interface

A crystal can be characterized for either series or parallel mode operation. The 8533-11 fanout buffer has a built-in crystal oscillator circuit. This interface can accept either a series or parallel crystal without additional components as shown in *Figure 5.* The physical location of the crystal should be located as close as possible to the XTAL1 and XTAL2 pins.

The experiments show that using a 19.44MHz crystal results in an output frequency of 19.4404746MHz and approximately 44% of duty cycle.

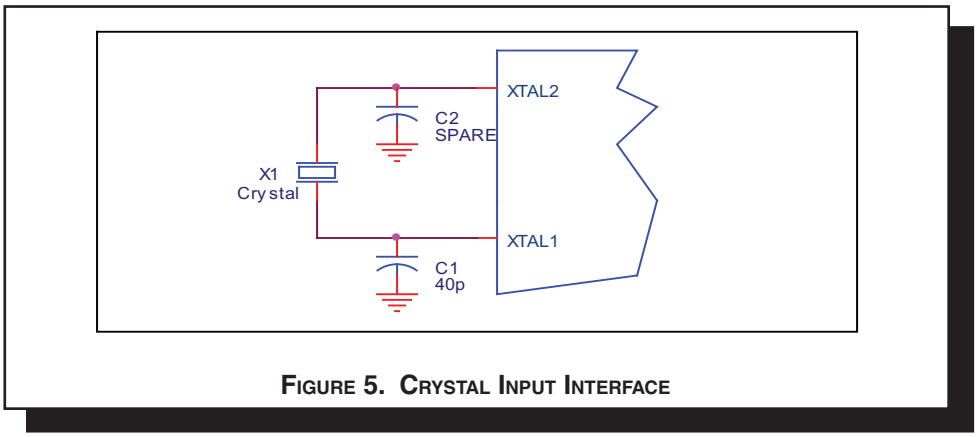


Figure 5. Crystal Input Interface

Schematic Example

Figure 6 shows a schematic example of the 8533-11. In this example, the XTAL input is selected. The decoupling capacitors should be physically located near the power pin. For 8533-11, the unused clock outputs can be left floating.

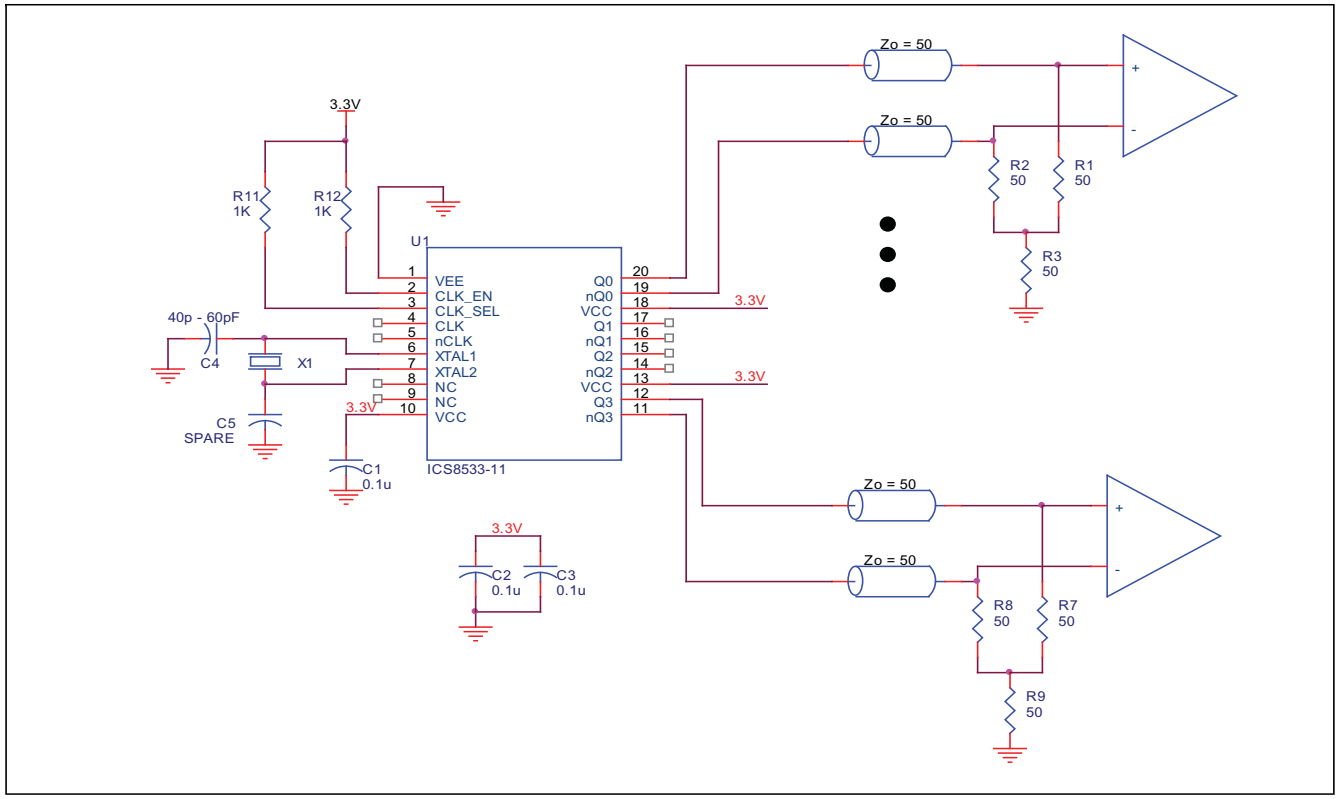


Figure 6. 8533-11 LVPECL Buffer Schematic Example

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8533-11.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the 8533-11 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 50mA = **173.3mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 30.2mW = **120.8mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 173.3mW + 120.8mW = **294.1mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.294W * 66.6°C/W = 89.58°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.
LVPECL output driver circuit and termination are shown in *Figure 7.*

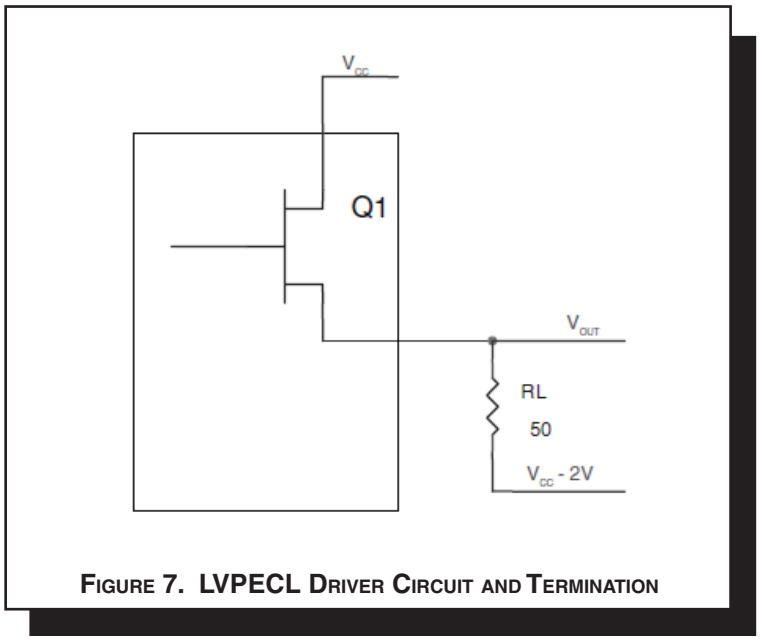


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination
voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **$V_{CC\_MAX} – 1.0V$**

  $(V_{CC\_MAX} - V_{OH\_MAX}) =$ **1.0V**

- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **$V_{CC\_MAX} – 1.7V$**

  $(V_{CC\_MAX} - V_{OL\_MAX}) =$ **1.7V**

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50Ω] * 1V =$ **20.0mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50Ω] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 20 Lead TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for 8533-11 is: 428

Package Outline - G Suffix for 20 Lead TSSOP

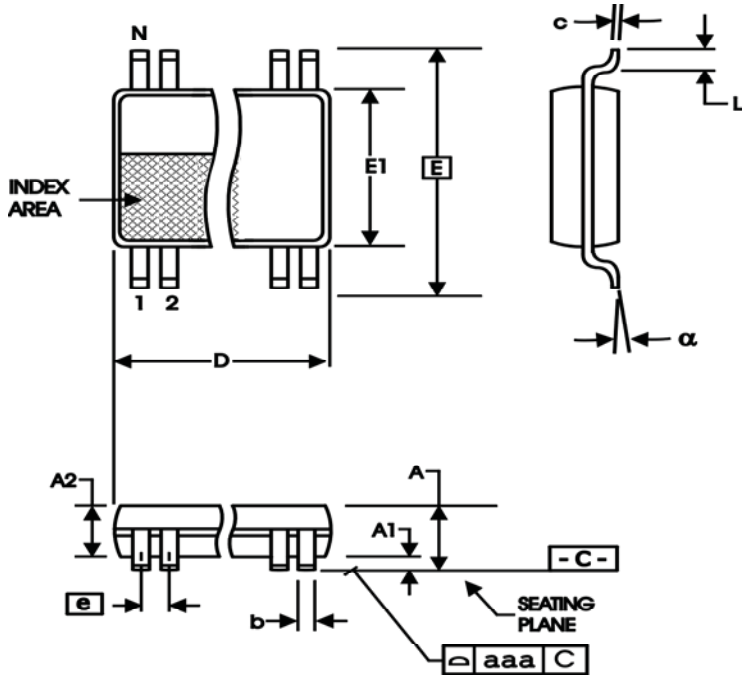


Table 9. Package Dimensions

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MS-153

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Package	Temperature
8533AG-11LF	ICS8533AG11L	20 Lead “Lead-Free” TSSOP	Tube	0°C to 70°C
8533AG-11LFT	ICS8533AG11L	20 Lead “Lead-Free” TSSOP	Tape and Reel	0°C to 70°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
D		3	Revised Figure 1, CLK_EN Timing Diagram.	10/18/01
D		3	Revised Figure 1, CLK_EN Timing Diagram.	11/2/01
D		8-10	Deleted Crystal Oscillator Circuit Frequency Fine Tuning section from datasheet.	12/11/01
D	T5	5	Shortened Crystal Characteristics table. ESR row, values have changed from 50Ω Min, 80Ω Max. to 70Ω Max.	1/11/02
D		8	Added Termination for LVPECL Outputs section.	5/28/02
D		6	Output Load Test Circuit diagram - corrected V_{EE} equation to read, V_{EE} = -1.3V ± 0.165V from V_{EE} = -1.3V ± 0.135V.	10/3/02
E	T2 T4B T4D T5	2 4 4 5 5 5 7 7 8 9 9	Pin Characteristics Table - changed C_{IN} from 4pF max. to 4pF typical. Absolute Maximum Ratings - revised Output rating. LVCMOS DC Characteristics Table - changed V_{IH} max. from 3.765V to V_{CC} + 0.3V. LVPECL DC CHaracteristics Table - changed V_{SWING} max. from 0.85V to 1.0V. Crystal Characteristics Table - changed ESR from 70Ω max. to 50Ω max. AC Characteristics Table - deleted oscTOL row from table. Updated Single Ended Signal Driving Differential Input Diagram. Updated LVPECL Output Termination Diagrams. Added Differential Clock Input Interface section. Added Crystal section. Added Schematic Example.	10/30/03
E	 T10	1 14	Features Section - added Lead-Free bullet. Ordering Information Table - added “Lead-Free” part number.	12/14/04
E	T10	14	Ordering Information Table - removed leaded devices. Updated data sheet format.	7/9/15

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