Low Skew, 1-to-4
LVCMOS/LVTTL-to-LVDS Fanout Buffer

Description

The 8545-01 is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-LVDS Clock Fanout Buffer. Utilizing Low Voltage Differential Signaling (LVDS) the 8545-01 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The 8545-01 accepts a LVCMOS/LVTTL input level and translates it to 3.3V LVDS output levels. Guaranteed output and part-to-part skew characteristics make the 8545-01 ideal for those applications demanding well defined performance and repeatability.

Features

- Four differential LVDS output pairs
- Two LVCMOS/LVTTL clock inputs to support redundant or selectable frequency fanout applications
- Maximum output frequency: 650MHz
- Translates LVCMOS/LVTTL input signals to LVDS levels
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 3.6ns (maximum)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in lead-free (RoHS 6) package

Block Diagram

Pin Assignment

8545-01
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm
package body
G Package
Top View
Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name(s)</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 9, 13</td>
<td>GND</td>
<td>Power</td>
<td>Power supply ground.</td>
</tr>
<tr>
<td>2</td>
<td>CLK_EN</td>
<td>Input</td>
<td>Pullup</td>
</tr>
<tr>
<td>3, 5, 6, 7, 8</td>
<td>nc</td>
<td>Unused</td>
<td>No connect.</td>
</tr>
<tr>
<td>4</td>
<td>CLK</td>
<td>Input</td>
<td>Pulldown</td>
</tr>
<tr>
<td>10, 18</td>
<td>VDD</td>
<td>Power</td>
<td>Positive supply pins.</td>
</tr>
<tr>
<td>11, 12</td>
<td>nQ3, Q3</td>
<td>Output</td>
<td>Differential output pair. LVDS interface levels.</td>
</tr>
<tr>
<td>14, 15</td>
<td>nQ2, Q2</td>
<td>Output</td>
<td>Differential output pair. LVDS interface levels.</td>
</tr>
<tr>
<td>16, 17</td>
<td>nQ1, Q1</td>
<td>Output</td>
<td>Differential output pair. LVDS interface levels.</td>
</tr>
<tr>
<td>19, 20</td>
<td>nQ0, Q0</td>
<td>Output</td>
<td>Differential output pair. LVDS interface levels.</td>
</tr>
</tbody>
</table>

NOTE: Pullup and Pulldown refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R_PULLDOWN</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

Function Tables

Table 3. Clock Input Function Table

<table>
<thead>
<tr>
<th>Input</th>
<th>Outputs</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK</td>
<td>Q0:Q3</td>
</tr>
<tr>
<td>0</td>
<td>LOW</td>
</tr>
<tr>
<td>1</td>
<td>HIGH</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{DD}$</td>
<td>4.6V</td>
</tr>
<tr>
<td>Inputs, $V_I$</td>
<td>-0.5V to $V_{DD}$ + 0.5V</td>
</tr>
<tr>
<td>Outputs, $I_O$</td>
<td>10mA</td>
</tr>
<tr>
<td>Continuous Current</td>
<td>15mA</td>
</tr>
<tr>
<td>Surge Current</td>
<td></td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_{JA}$</td>
<td>91.1°C/W (0 mps)</td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%, T_A = 0°C$ to 70°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$</td>
<td>Positive Supply Voltage</td>
<td></td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DD}$</td>
<td>Power Supply Current</td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td>mA</td>
</tr>
</tbody>
</table>

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%, T_A = 0°C$ to 70°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{DD} = V_{IN} = 3.465V$</td>
<td>2</td>
<td>$V_{DD}$ + 0.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td></td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>$CLK = CLK_EN$</td>
<td></td>
<td>150</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>$CLK = CLK_EN$</td>
<td>$V_{DD}$ = 3.465V, $V_{IN}$ = 0V</td>
<td>-5</td>
<td></td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>

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### Table 4C. LVDS DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OD}$</td>
<td>Differential Output Voltage</td>
<td></td>
<td>200</td>
<td>280</td>
<td>360</td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{OD}$</td>
<td>$V_{OD}$ Magnitude Change</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OS}$</td>
<td>Offset Voltage</td>
<td></td>
<td>1.125</td>
<td>1.25</td>
<td>1.375</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{OS}$</td>
<td>$V_{OS}$ Magnitude Change</td>
<td></td>
<td>5</td>
<td>25</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>$I_{Oz}$</td>
<td>High Impedance Leakage</td>
<td></td>
<td>-10</td>
<td>±1</td>
<td>+10</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{OFF}$</td>
<td>Power Off Leakage</td>
<td></td>
<td>-20</td>
<td>±1</td>
<td>+20</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{OSD}$</td>
<td>Differential Output Short Circuit Current</td>
<td></td>
<td>-3.5</td>
<td>-5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Output Short Circuit Current</td>
<td></td>
<td>-3.5</td>
<td>-5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>Output Voltage High</td>
<td></td>
<td>1.34</td>
<td>1.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Output Voltage Low</td>
<td></td>
<td>0.9</td>
<td>1.06</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

### AC Electrical Characteristics

### Table 5. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{MAX}$</td>
<td>Output Frequency</td>
<td></td>
<td></td>
<td></td>
<td>650</td>
<td>MHz</td>
</tr>
<tr>
<td>$t_{PD}$</td>
<td>Propagation Delay; NOTE 1</td>
<td></td>
<td>1.4</td>
<td>3.6</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{sk(o)}$</td>
<td>Output Skew; NOTE 2, 4</td>
<td></td>
<td></td>
<td></td>
<td>40</td>
<td>ps</td>
</tr>
<tr>
<td>$t_{sk(pp)}$</td>
<td>Part-to-Part Skew; NOTE 3, 4</td>
<td></td>
<td></td>
<td></td>
<td>500</td>
<td>ps</td>
</tr>
<tr>
<td>$t_{R} / t_{F}$</td>
<td>Output Rise/Fall Time</td>
<td>20% to 80% @ 50MHz</td>
<td></td>
<td></td>
<td>150</td>
<td>ps</td>
</tr>
<tr>
<td>$\text{odc}$</td>
<td>Output Duty Cycle</td>
<td>$f \leq 266MHz$</td>
<td>45</td>
<td>55</td>
<td></td>
<td>%</td>
</tr>
</tbody>
</table>

All parameters measured at $f_{MAX}$ unless noted otherwise.
NOTE 1: Measured from $V_{DD}/2$ of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at $V_{DD}/2$ of the input to the differential output crossing point.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
Parameter Measurement Information

3.3V LVDS Output Load AC Test Circuit

Differential Output Level

Part-to-Part Skew

Output Skew

Output Duty Cycle/Pulse Width/Period

Propagation Delay
Parameter Measurement Information, continued

Output Rise/Fall Time

Power Off Leakage Setup

Offset Voltage Setup

Differential Output Voltage Setup

High Impedance Leakage Current Setup

Differential Output Short Circuit Setup
Output Short Circuit Current Setup

Application Information

Recommendations for Unused Output Pins

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.
3.3V LVDS Driver Termination

A general LVDS interface is shown in Figure 1. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

Figure 1. Typical LVDS Driver Termination
Power Considerations

This section provides information on power dissipation and junction temperature for the 8545-01. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8545-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for \( V_{DD} = 3.3V + 5\% = 3.465V \), which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- \( \text{Power (core)_{MAX}} = V_{DD\_MAX} \times I_{DD\_MAX} = 3.465V \times 50mA = 173.25mW \)

2. Junction Temperature.

Junction temperature, \( T_j \), is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for \( T_j \) is as follows: 

\[ T_j = \theta_{JA} \times Pd\_total + T_A \]

- \( T_j \) = Junction Temperature
- \( \theta_{JA} \) = Junction-to-Ambient Thermal Resistance
- \( Pd\_total \) = Total Device Power Dissipation (example calculation is in section 1 above)
- \( T_A \) = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \( \theta_{JA} \) must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 6 below.

Therefore, \( T_j \) for an ambient temperature of 70°C with all outputs switching is:

\[ 70°C + 0.173W \times 91.1°C/W = 85.7°C \]  
This is well below the limit of 125°C.

This calculation is only an example. \( T_j \) will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance \( \theta_{JA} \) for 20 Lead TSSOP, Forced Convection

<table>
<thead>
<tr>
<th>( \theta_{JA} ) by Velocity</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meters Per Second</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>91.1°C/W</td>
<td>86.7°C/W</td>
<td>84.6°C/W</td>
</tr>
</tbody>
</table>
Reliability Information

Table 7. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP

<table>
<thead>
<tr>
<th>Meters Per Second</th>
<th>0</th>
<th>1</th>
<th>2.5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>91.1°C/W</td>
<td>86.7°C/W</td>
<td>84.6°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for 8545-01 is: 644

Package Outline and Package Dimension

Package Outline - G Suffix for 20 Lead TSSOP

Table 8. Package Dimensions

All Dimensions in Millimeters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>1.05</td>
<td>1.20</td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>0.15</td>
</tr>
<tr>
<td>A2</td>
<td>0.80</td>
<td>1.05</td>
</tr>
<tr>
<td>b</td>
<td>0.19</td>
<td>0.30</td>
</tr>
<tr>
<td>c</td>
<td>0.09</td>
<td>0.20</td>
</tr>
<tr>
<td>D</td>
<td>6.40</td>
<td>6.60</td>
</tr>
<tr>
<td>E</td>
<td>6.40 Basic</td>
<td></td>
</tr>
<tr>
<td>E1</td>
<td>4.30</td>
<td>4.50</td>
</tr>
<tr>
<td>e</td>
<td>0.65 Basic</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.75</td>
</tr>
<tr>
<td>$\alpha$</td>
<td>0°</td>
<td>8°</td>
</tr>
<tr>
<td>aaa</td>
<td>0.10</td>
<td></td>
</tr>
</tbody>
</table>

Reference Document: JEDEC Publication 95, MO-153
### Ordering Information

Table 9. Ordering Information

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>8545AG-01LF</td>
<td>ICS8545AG01L</td>
<td>“Lead-Free” 20 Lead TSSOP</td>
<td>Tube</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>8545AG-01LFT</td>
<td>ICS8545AG01L</td>
<td>“Lead-Free” 20 Lead TSSOP</td>
<td>Tape &amp; Reel</td>
<td>0°C to 70°C</td>
</tr>
</tbody>
</table>

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
### Revision History Sheet

<table>
<thead>
<tr>
<th>Rev</th>
<th>Table</th>
<th>Page</th>
<th>Description of Change</th>
<th>Date</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>T9</td>
<td>11</td>
<td>Ordering Information - removed leaded devices.</td>
<td>7/10/15</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Updated data sheet format.</td>
<td></td>
</tr>
</tbody>
</table>

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(Rev.1.0 Mar 2020)

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