1:4, Differential-to-LVCMOS/LVTTL Zero Delay Clock Generator

ICS87004

DATA SHEET

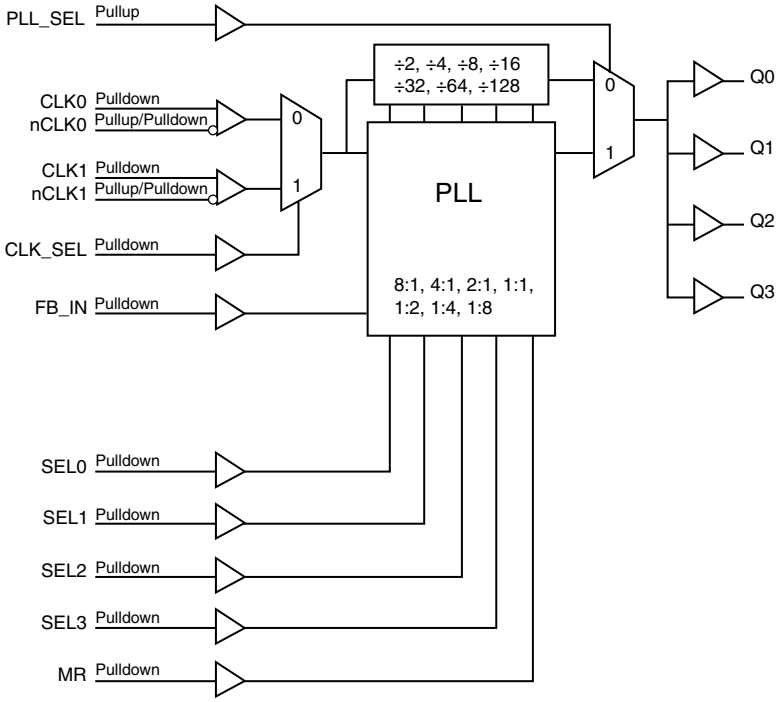
General Description

The ICS87004 is a highly versatile 1:4 Differential-to-LVCMOS/LVTTL Clock Generator and a member of the HiPerClockS® family of High Performance Clock Solutions from IDT. The ICS87004 has two selectable clock inputs. The CLK0, nCLK0 and CLK1, nCLK1 pairs can accept most standard differential input levels. Internal bias on the nCLK0 and nCLK1 inputs allows the CLK0 and CLK1 inputs to accept LVCMOS/LVTTL. The ICS87004 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider and has an input and output frequency range of 15.625MHz to 250MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve "zero delay" between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

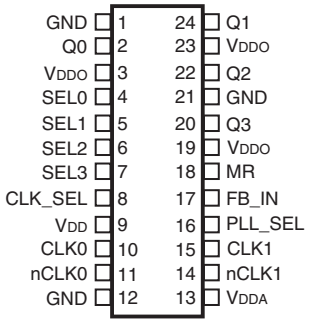
Features

- Four LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Selectable CLK0/nCLK0 or CLK1/nCLK1 clock inputs
- CLKx/nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Internal bias on nCLK0 and nCLK1 to support LVCMOS/LVTTL levels on CLK0 and CLK1 inputs
- Output frequency range: 15.625MHz to 250MHz
- Input frequency range: 15.625MHz to 250MHz
- VCO range: 250MHz to 500MHz
- External feedback for "zero delay" clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Fully integrated PLL
- Cycle-to-cycle jitter: 45ps (maximum)
- Output skew: 50ps (maximum)
- Static phase offset: 50ps ± 125ps (3.3V ± 5%), CLK0/nCLK0
- Full 3.3V or 2.5V output operating supply
- 5V tolerant inputs
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS87004

24-Lead TSSOP
7.8mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 12, 21	GND	Power		Power supply ground.
2, 20, 22, 24	Q0, Q3, Q2, Q1	Output		Single-ended clock outputs. 7Ω typical output impedance. LVCMOS/LVTTL interface levels.
3, 19, 23	V_{DDO}	Power		Output supply pins.
4, 5, 6, 7	SEL0, SEL1, SEL2, SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTL interface levels.
8	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects differential CLK1, nCLK1. When LOW, selects differential CLK0, nCLK0. LVCMOS/LVTTL interface levels.
9	V_{DD}	Power		Core supply pin.
10	CLK0	Input	Pulldown	Non-inverting differential clock input.
11	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
13	V_{DDA}	Power		Analog supply pin.
14	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
15	CLK1	Input	Pulldown	Non-inverting differential clock input.
16	PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS/LVTTL interface levels.
17	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with “Zero Delay.” Connect to one of the outputs. LVCMOS/LVTTL interface levels.
18	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DD}, V_{DDO} = 3.465V			23	pF
		V_{DD}, V_{DDO} = 2.625V			17	pF
R_{OUT}	Output Impedance		5	7	12	Ω

Function Tables

Table 3A. PLL Enable Function Table

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)	Q[0:3]
0	0	0	0	125 - 250	÷1
0	0	0	1	62.5 - 125	÷1
0	0	1	0	31.25 - 62.5	÷1
0	0	1	1	15.625 - 31.25	÷1
0	1	0	0	125 - 250	÷2
0	1	0	1	62.5 - 125	÷2
0	1	1	0	31.25 - 62.5	÷2
0	1	1	1	125 - 250	÷4
1	0	0	0	62.5 - 125	÷4
1	0	0	1	125 - 250	÷8
1	0	1	0	62.5 - 125	x2
1	0	1	1	31.25 - 62.5	x2
1	1	0	0	15.625 - 31.25	x2
1	1	0	1	31.25 - 62.5	x4
1	1	1	0	15.625 - 31.25	x4
1	1	1	1	15.625 - 31.25	x8

Table 3B. PLL Bypass Function Table

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	**SEL2**	**SEL1**	**SEL0**	**Q[0:3]**
0	0	0	0	÷8
0	0	0	1	÷8
0	0	1	0	÷8
0	0	1	1	÷16
0	1	0	0	÷16
0	1	0	1	÷16
0	1	1	0	÷32
0	1	1	1	÷32
1	0	0	0	÷64
1	0	0	1	÷128
1	0	1	0	÷4
1	0	1	1	÷4
1	1	0	0	÷8
1	1	0	1	÷2
1	1	1	0	÷4
1	1	1	1	÷2

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				100	mA
I_{DDA}	Analog Supply Current				16	mA
I_{DDO}	Output Supply Current				6	mA

Table 4B. Power Supply DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				96	mA
I_{DDA}	Analog Supply Current				15	mA
I_{DDO}	Output Supply Current				6	mA

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
			$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		$V_{DD} = 3.3V$	-0.3		0.8	V
			$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	SEL[0:3], MR, FB_IN, CLK_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	µA
I_{IL}	Input Low Current	SEL[0:3], MR, FB_IN, CLK_SEL	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		PLL_SEL	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
V_{OH}	Output High Voltage; NOTE 1		$V_{DDO} = 3.465V$	2.6			V
			$V_{DDO} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1		$V_{DD} = 3.465V$ or $2.625V$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. In the Parameter Measurement Information Section, see *Output Load Test Circuit Diagrams.*

Table 4D. Differential DC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0/nCLK0, CLK1/nCLK1	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-5			µA
		nCLK0, nCLK1	$V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$	-150			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		$V_{DD} – 0.85$	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0°C$ to $70°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			15.625		250	MHz
t_{PD}	Propagation Delay; NOTE 1	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V, f ≤ 250MHz, Qx ÷ 2	5		6.2	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	CLK0, nCLK0	PLL_SEL = 3.3V, f_{REF} ≤ 167MHz, Qx ÷ 1	-75	50	175	ps
		CLK1, nCLK1		-190	-65	175	ps
*t*sk(o)	Output Skew; NOTE 3, 4	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V		40	50	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4		f_{OUT} > 40MHz		30	45	ps
t_L	PLL Lock Time					1	ms
t_R / t_F	Output Rise/Fall Time		20% to 80%	400		800	ps
odc	Output Duty Cycle			40	50	60	%

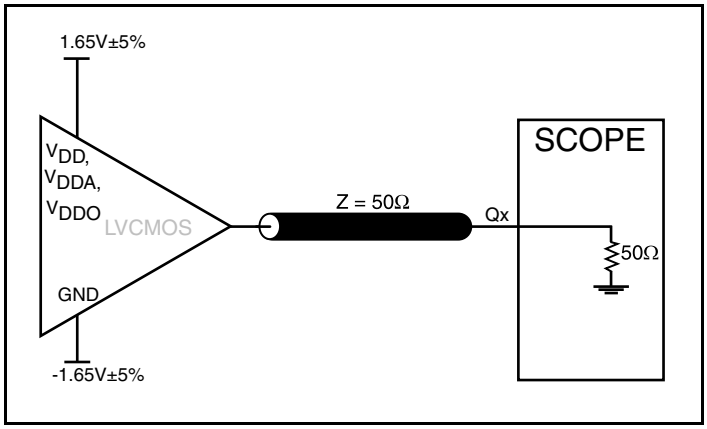
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

Table 5B. AC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0°C$ to $70°C$

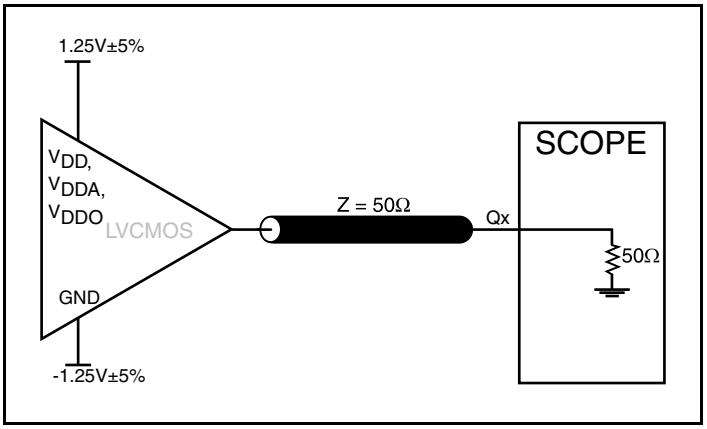
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency			15.625		250	MHz
t_{PD}	Propagation Delay; NOTE 1	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V, f ≤ 250MHz, Qx ÷ 2	5.3		6.9	ns
t(Ø)	Static Phase Offset; NOTE 2, 4	CLK0, nCLK0	PLL_SEL = 2.5V, f_{REF} ≤ 167MHz, Qx ÷ 1	-175	-25	125	ps
		CLK1, nCLK1		-290	-115	125	ps
*t*sk(o)	Output Skew; NOTE 3, 4	CLK0, nCLK0 CLK1, nCLK1	PLL_SEL = 0V		40	45	ps
*t*jit(cc)	Cycle-to-Cycle Jitter; NOTE 4		f_{OUT} > 40MHz		35	45	ps
t_L	PLL Lock Time					1	ms
t_R / t_F	Output Rise/Fall Time		20% to 80%	400		700	ps
odc	Output Duty Cycle			44	50	56	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at $V_{DDO}/2$.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

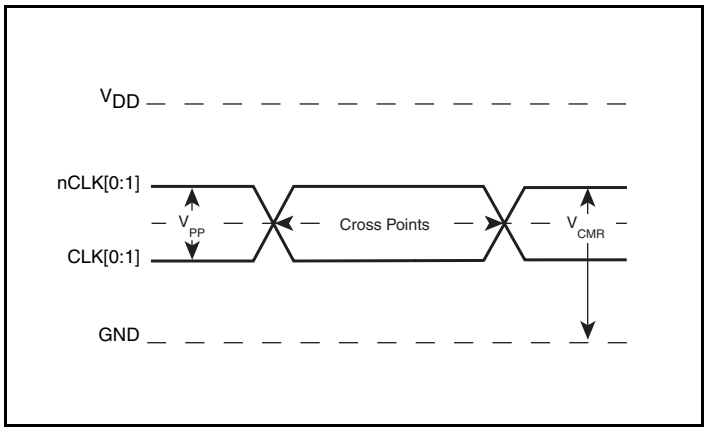
Parameter Measurement Information



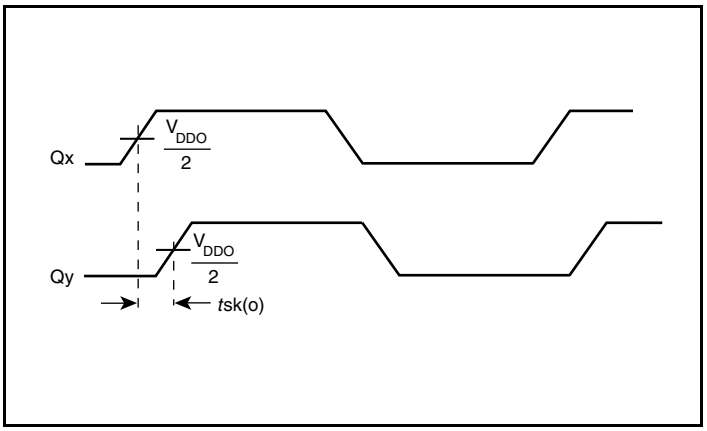
3.3V Output Load AC Test Circuit



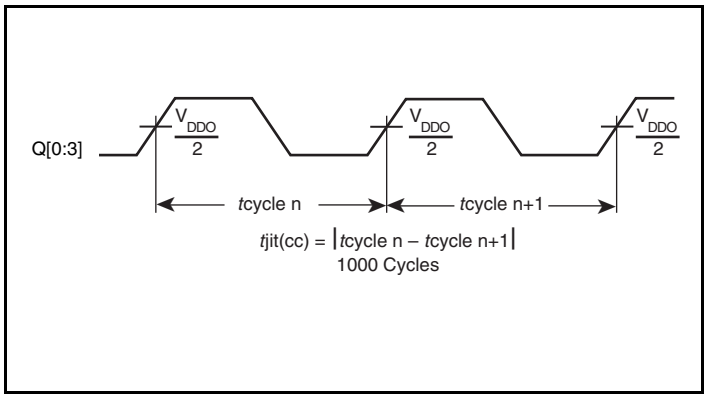
2.5V Output Load AC Test Circuit



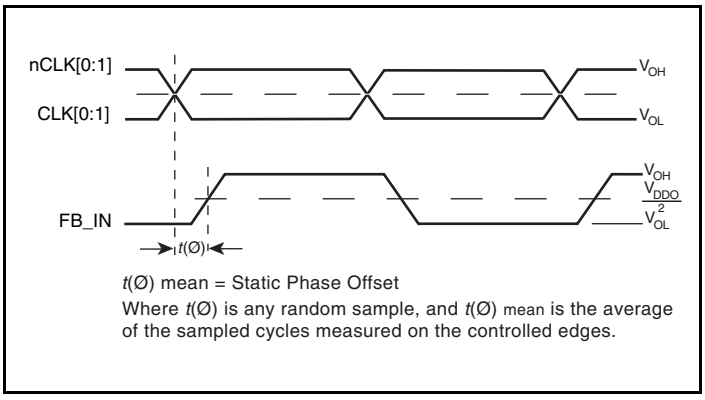
Differential Input Level



Output Skew

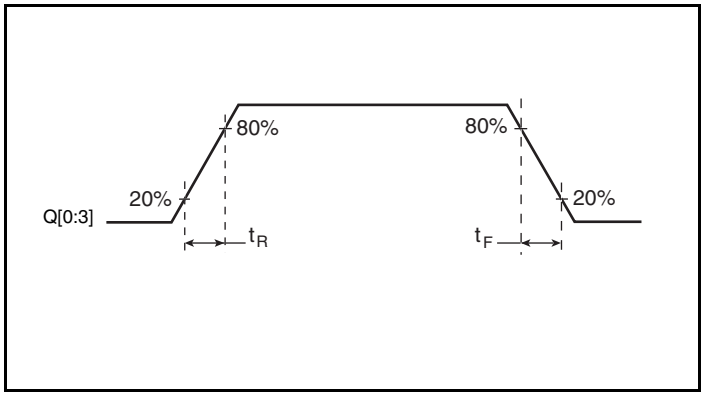


Cycle-to-Cycle Jitter

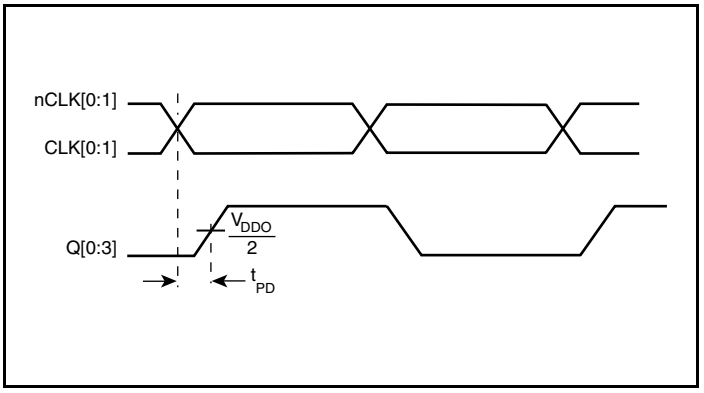


Static Phase Offset

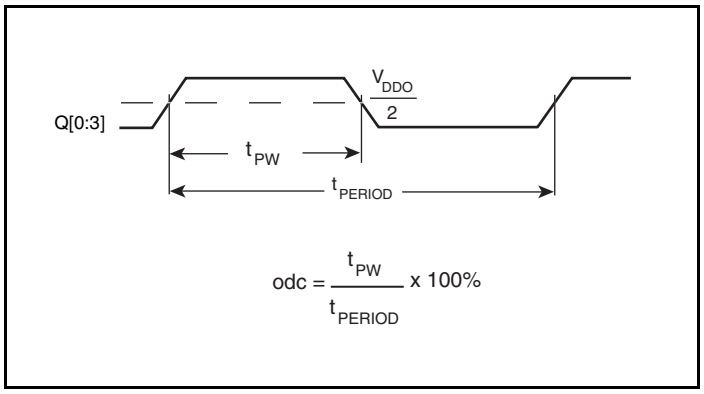
Parameter Measurement Information, continued



Output Rise/Fall Time



Propagation Delay



Output Duty Cycle/Pulse Width/Period

Application Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS87004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA} and V_{DDO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin. The 10Ω resistor can also be replaced by a ferrite bead.

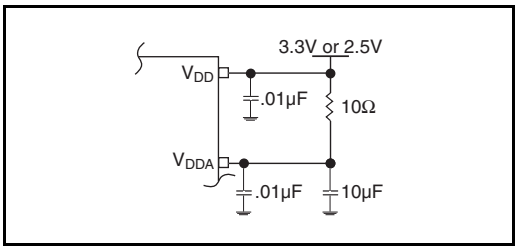


Figure 1. Power Supply Filtering

Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = V_{DD}/2 is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

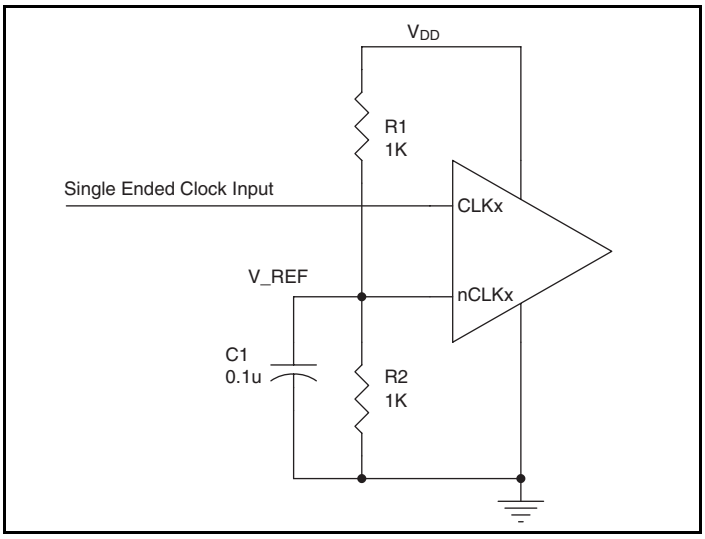


Figure 2. Single-Ended Signal Driving Differential Input

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVCMOS Outputs

All unused LVCMOS output can be left floating. There should be no trace attached.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

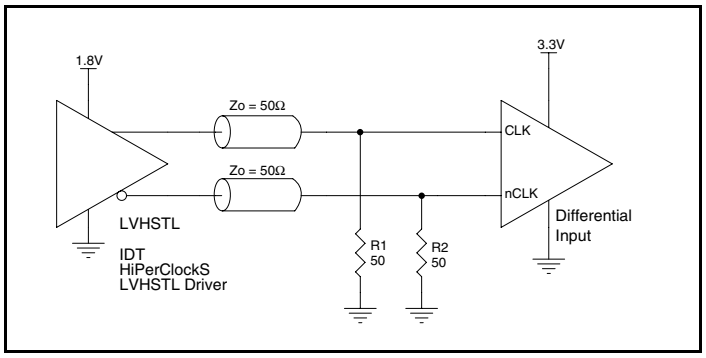


Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver

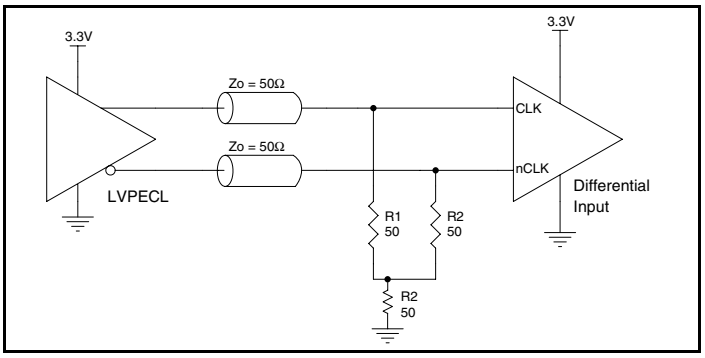


Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

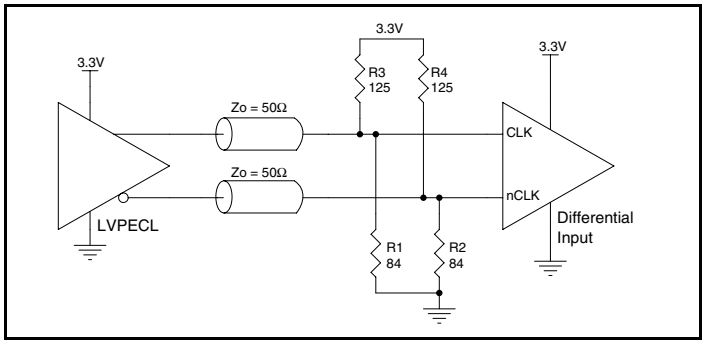


Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver

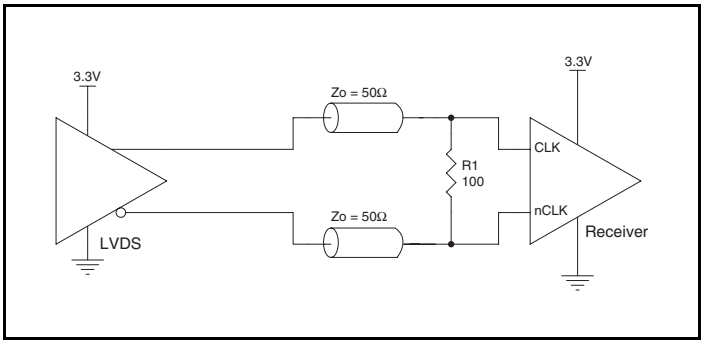


Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver

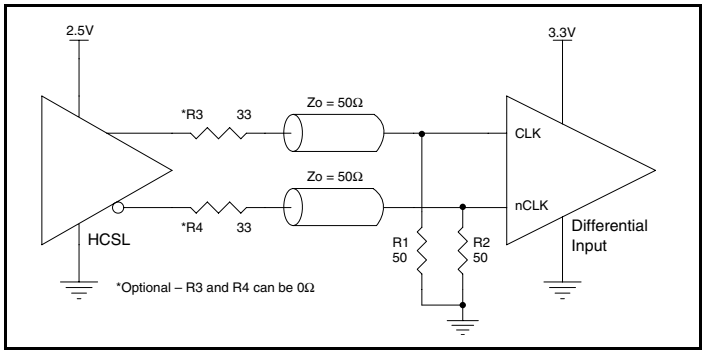


Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver

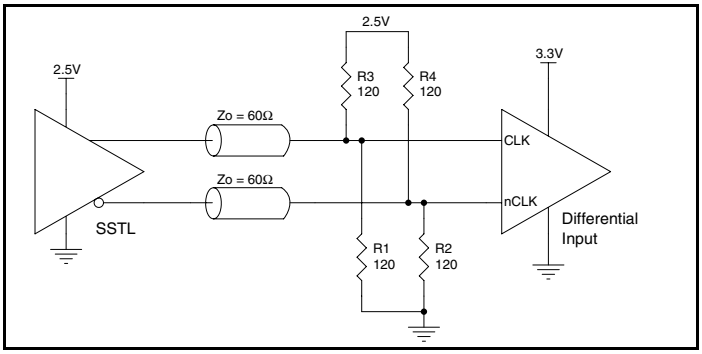


Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 24 Lead TSSOP

θ_{JA} vs. Air Flow			
Linear Feet per Minute	**0**	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	63°C/W	60°C/W

Transistor Count

The transistor count for ICS87004 is: 2578

Package Outline and Package Dimensions

Package Outline - G Suffix for 24 Lead TSSOP

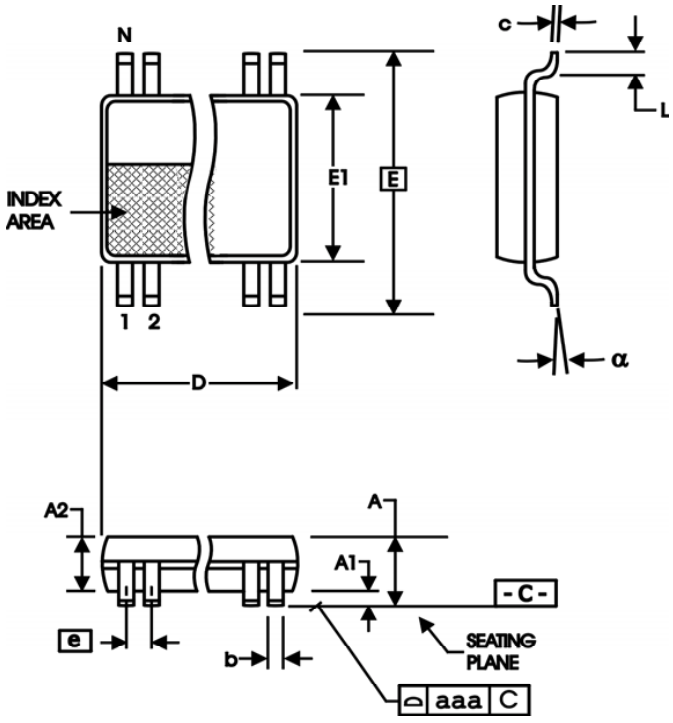


Table 7. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	24	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
87004AG	ICS87004AG	24 Lead TSSOP	Tube	0°C to 70°C
87004AGT	ICS87004AG	24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
87004AGLF	ICS87004AGLF	“Lead-Free” 24 Lead TSSOP	Tube	0°C to 70°C
87004AGLFT	ICS87004AGLF	“Lead-Free” 24 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	13	Ordering Information Table - added Lead-Free marking.	6/16/04
A	T8	13	Ordering Information Table - corrected Lead-Free part number. Added Lead-Free note.	5/17/05
B	T5A T5B	6 6 10	3.3V AC Characteristics Table - adjusted t_{PD} parameter from 6ns max. to 6.2ns max. 2.5V AC Characteristics Table - adjusted t_{PD} parameter from 6.7ns max. to 6.9ns max. Added Recommendations for Unused Input and Output Pins section.	10/7/05
C	T4D T5A, T5B T8	6 7 11 13	Differential DC Characteristics Table - updated NOTES 1, 2. AC Characteristics Tables - Static Phase Offset, split CLKx into 2 rows. Specs changed for CLK1/nCLK1. Added Thermal note. Updated Differential Clock Input Interface section. Ordering Information Table - deleted “ICS” prefix from Part/Order Number column. Converted datasheet format.	10/6/09
C		1	Features section - corrected output skew from 465ps ot 50ps (maximum)	12/1/09

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