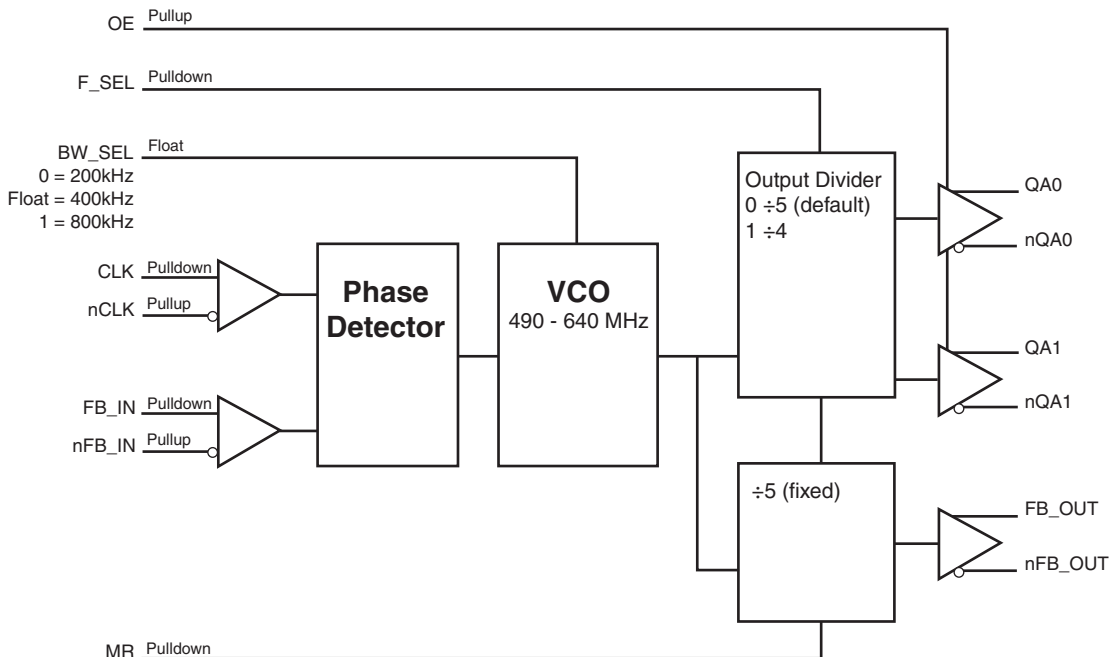


## GENERAL DESCRIPTION

The 874002 is a high performance Differential-to-LVDS Jitter Attenuator designed for use in PCI Express systems. In some PCI Express systems, such as those found in desktop PCs, the PCI Express clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter attenuator may be required to attenuate high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The 874002 has 3 PLL bandwidth modes: 200kHz, 400kHz, and 800kHz. The 200kHz mode will provide maximum jitter attenuation, but with higher PLL tracking skew and spread spectrum modulation from the motherboard synthesizer may be attenuated. The 400kHz provides an intermediate bandwidth that can easily track triangular spread profiles, while providing good jitter attenuation. The 800kHz bandwidth provides the best tracking skew and will pass most spread profiles, but the jitter attenuation will not be as good as the lower bandwidth modes. Because some 2.5Gb serdes have x20 multipliers while others have than x25 multipliers, the 874002 can be set for 1:1 mode or 5/4 multiplication mode (i.e. 100MHz input/125MHz output) using the F\_SEL pin.

The 874002 uses IDT's 3<sup>rd</sup> Generation FemtoClock™ PLL technology to achieve the lowest possible phase noise. The device is packaged in a 20 Lead TSSOP package, making it ideal for use in space constrained applications such as PCI Express add-in cards.

## BLOCK DIAGRAM



## FEATURES

- Two differential LVDS output pair
- One differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Output frequency range: 98MHz - 160MHz
- Input frequency range: 98MHz - 128MHz
- VCO range: 490MHz - 640MHz
- Cycle-to-cycle jitter: 35ps (maximum)
- 3.3V operating supply
- Three bandwidth modes allow the system designer to make jitter attenuation/tracking skew design trade-offs
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

### PLL BANDWIDTH (TYPICAL)

BW\_SEL  
 0 = PLL Bandwidth: 200kHz  
 Float = PLL Bandwidth: 400kHz (Default)  
 1 = PLL Bandwidth: 800kHz

## PIN ASSIGNMENT

nQA0	1	20	QA0
V <sub>DD</sub>	2	19	V <sub>DD</sub>
FB_OUT	3	18	QA1
nFB_OUT	4	17	nQA1
MR	5	16	nFB_IN
BW_SEL	6	15	FB_IN
nc	7	14	GND
V <sub>DDA</sub>	8	13	nCLK
F_SEL	9	12	CLK
V <sub>DD</sub>	10	11	OE

### 874002

20-Lead TSSOP  
 6.5mm x 4.4mm x 0.92mm  
 package body  
**G Package**  
 Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1, 20	nQA0, QA0	Output		Differential output pair. LVDS interface levels.
2, 19	V <sub>DDO</sub>	Power		Output supply pins.
3, 4	FB_OUT, nFB_OUT	Output		Differential feedback output pair. LVDS interface levels.
5	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs (Qx, FB_OUT) to go low and the inverted outputs (nQx, nFB_OUT) to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
6	BW_SEL	Input	Pullup/Pulldown	PLL Bandwidth select input. 0 = 200kHz, Float = 400kHz, 1 = 800kHz. See Table 3B.
7	nc	Unused		No connect.
8	V <sub>DDA</sub>	Power		Analog supply pin.
9	F_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels. See Table 3C.
10	V <sub>DD</sub>	Power		Core supply pin.
11	OE	Input	Pullup	Output enable pin. When HIGH, the outputs are active. When LOW, the outputs are in a high impedance state. LVCMOS/LVTTL interface levels. See Table 3A.
12	CLK	Input	Pulldown	Non-inverting differential clock input.
13	nCLK	Input	Pullup	Inverting differential clock input.
14	GND	Power		Power supply ground.
15	FB_IN	Input	Pulldown	Non-inverting differential feedback input.
16	nFB_IN	Input	Pullup	Inverting differential feedback input.
17, 18	nQA1, QA1	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**TABLE 3A. OUTPUT ENABLE FUNCTION TABLE**

Input	Outputs	
	QAx/nQAx	FB_OUT/nFB_OUT
0	HiZ	Enabled
1	Enabled	Enabled

**TABLE 3B. PLL BANDWIDTH/PLL BYPASS CONTROL**

Input	PLL Bandwidth (Typical)
BW_SEL	
0	200kHz
1	800kHz
Float	400kHz

**TABLE 3C. FREQUENCY SELECT FUNCTION TABLE**

Input	Outputs	
	QA[0:1]/nQA[0:1]	FB_OUT/nFB_OUT
0 (default)	÷5	÷5
1	÷4	÷5

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	73.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.12$	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{DD}$	Power Supply Current				80	mA
$I_{DDA}$	Analog Supply Current				12	mA
$I_{DDO}$	Output Supply Current				110	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	F_SEL, OE, MR			$V_{DD} + 0.3$	V
		BW_SEL	$V_{DD} - 0.4$			V
$V_{IL}$	Input Low Voltage	F_SEL, OE, MR	-0.3		0.8	V
		BW_SEL			$V_{DD} + 0.4$	V
$V_{IM}$	Input Mid Voltage	BW_SEL	$V_{DD}/2 - 0.1$		$V_{DD}/2 + 0.1$	V
$I_{IH}$	Input High Current	OE	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
		BW_SEL, F_SEL, MR	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
$I_{IL}$	Input Low Current	OE, BW_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
		F_SEL, MR	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, FB_IN	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK, nFB_IN	$V_{DD} = V_{IN} = 3.465V$	5		$\mu A$
$I_{IL}$	Input Low Current	CLK, FB_IN	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK, nFB_IN	$V_{DD} = V_{IN} = 3.465V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK and FB\_IN, nFB\_IN is  $V_{DD} + 0.3V$ .

**TABLE 4D. LVDS DC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OD}$	Differential Output Voltage		250	370	485	mV
$\Delta V_{OD}$	$V_{OD}$ Magnitude Change				50	mV
$V_{OS}$	Offset Voltage		1.0	1.30	1.60	V
$\Delta V_{OS}$	$V_{OS}$ Magnitude Change				50	mV

**TABLE 5. AC CHARACTERISTICS,  $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency		98		160	MHz
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 1				35	ps
$tsk(o)$	Output Skew; NOTE 2, 3				40	ps
$tsk(\emptyset)$	Static Phase Offset; NOTE 4		-150	-20	110	ps
$t_r / t_f$	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: This parameter is defined in accordance with JEDEC Standard 65.

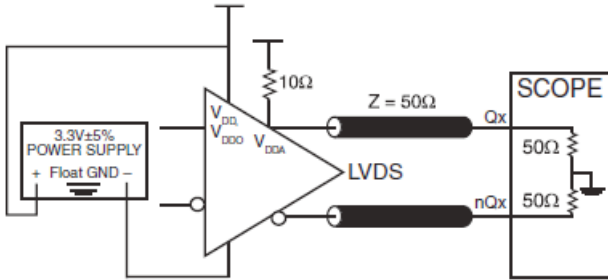
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

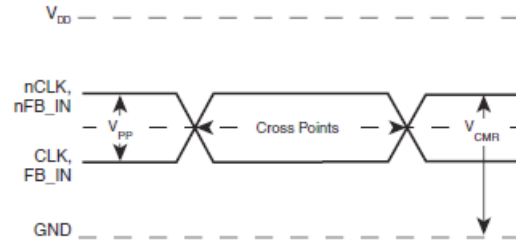
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 4: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

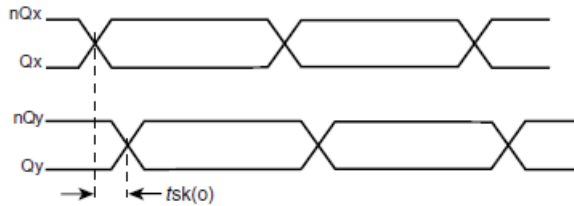
# PARAMETER MEASUREMENT INFORMATION



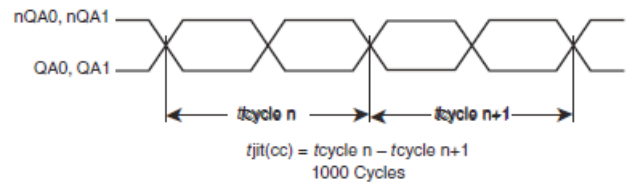
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



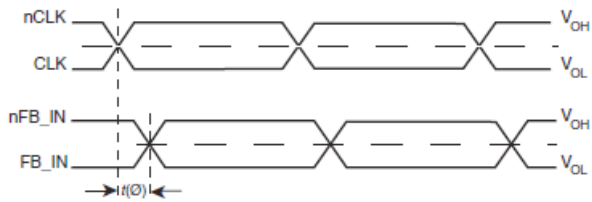
DIFFERENTIAL INPUT LEVEL



OUTPUT SKEW

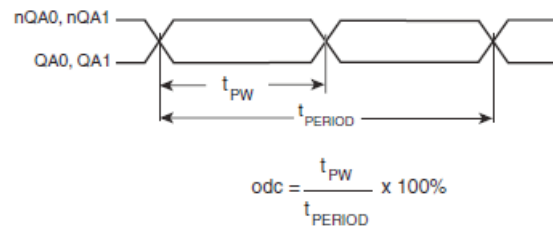


CYCLE-TO-CYCLE JITTER

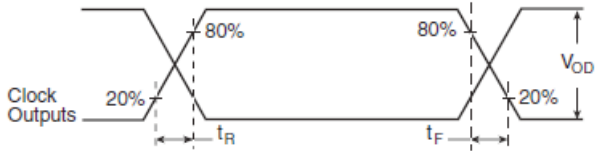


$t(\emptyset)_{\text{mean}}$  = Static Phase Offset  
 (where  $t(\emptyset)$  is any random sample, and  $t(\emptyset)_{\text{mean}}$  is the average of the sampled cycles measured on controlled edges)

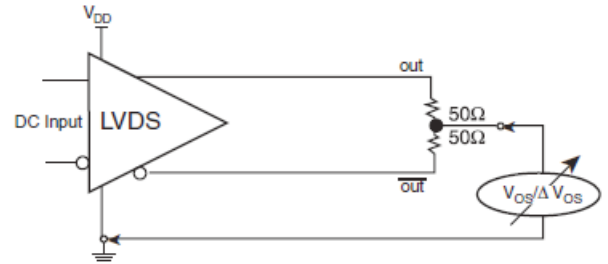
OUTPUT RISE/FALL TIME



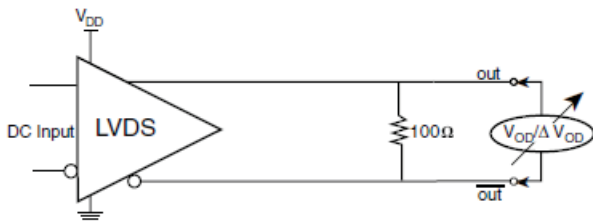
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 874002 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$ , and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{DDA}$  pin.

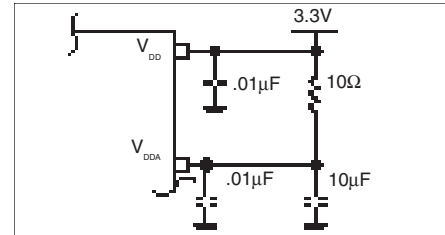


FIGURE 1. POWER SUPPLY FILTERING

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors  $R1$ ,  $R2$  and  $C1$ . This bias circuit should be located as close as possible

to the input pin. The ratio of  $R1$  and  $R2$  might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only  $2.5\text{V}$  and  $V_{DD} = 3.3\text{V}$ ,  $V_{REF}$  should be  $1.25\text{V}$  and  $R2/R1 = 0.609$ .

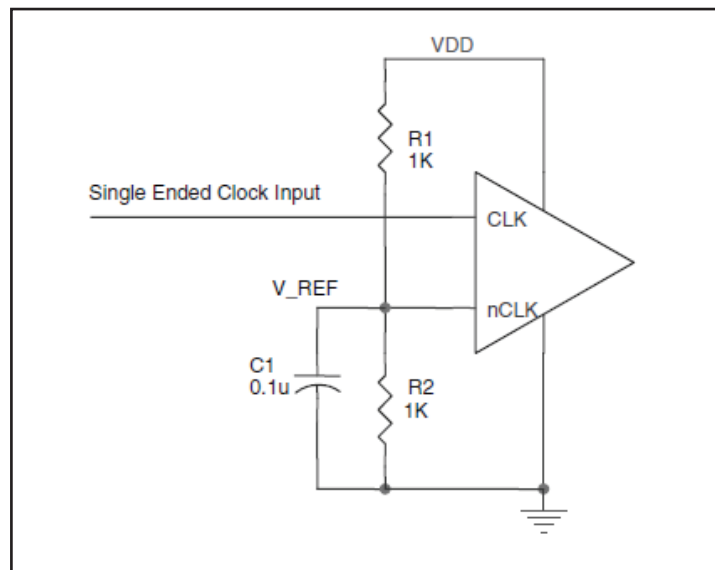
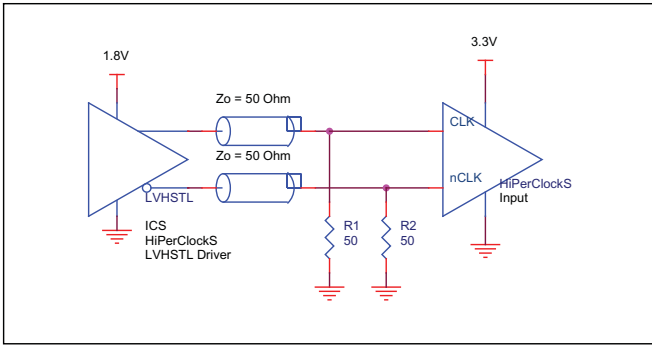


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

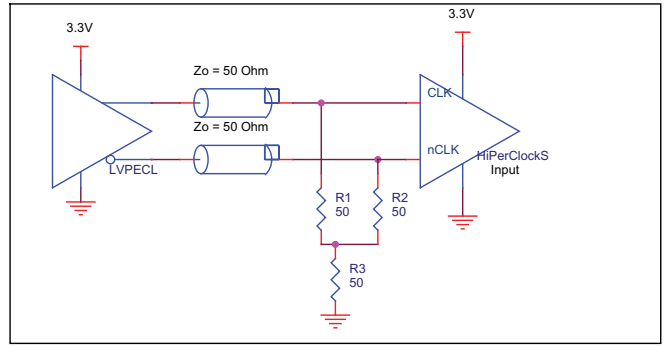
**DIFFERENTIAL CLOCK INPUT INTERFACE**

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

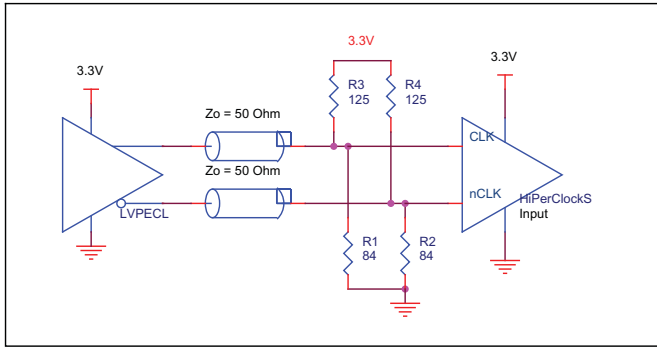
Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 3A, the input termination applies for IDT HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



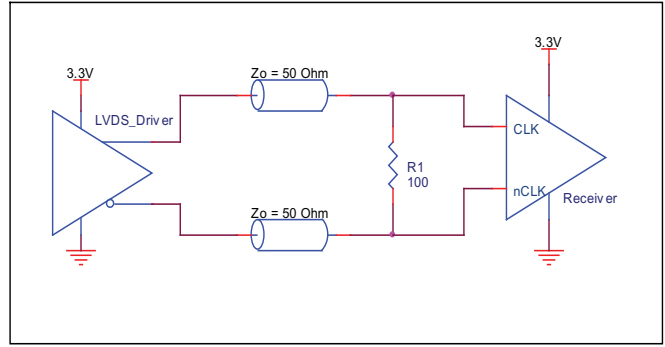
**FIGURE 3A. HiPerClockS CLK/nCLK INPUT DRIVEN BY IDT HiPerClockS LVHSTL DRIVER**



**FIGURE 3B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

**RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS**

**INPUTS:**

**LVC MOS CONTROL PINS:**

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

**OUTPUTS:**

**LVDS**

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.



### 3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

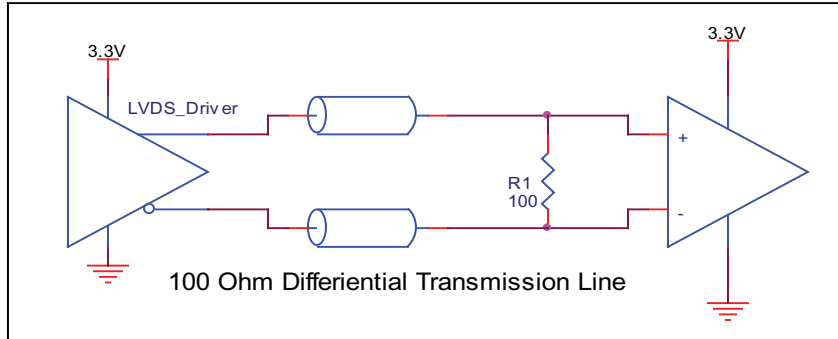


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 874002. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 874002 is the sum of the core power plus the power dissipated in the load(s).

The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (80mA + 12mA) = \mathbf{318.78mW}$
- Power (outputs)<sub>MAX</sub> =  $V_{DDO\_MAX} * I_{DDO\_MAX} = 3.465V * 110mA = \mathbf{381.15mW}$

$$\mathbf{Total\ Power_{MAX} = 318.78mW + 381.15mW = 699.93mW}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.700\text{W} * 66.6^\circ\text{C/W} = 116.6^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 6. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-LEAD TSSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

## RELIABILITY INFORMATION

TABLE 7.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for 874002 is: 1216

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

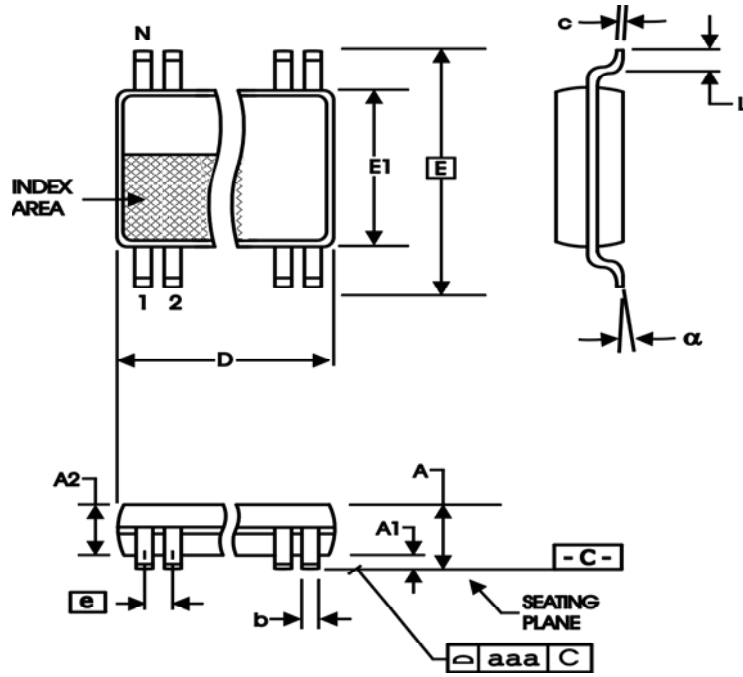


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	MIN	MAX
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 9. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
874002AGLF	ICS874002AGL	20 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
874002AGLFT	ICS874002AGL	20 Lead "Lead-Free" TSSOP	tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

**REVISION HISTORY SHEET**

<b>Rev</b>	<b>Table</b>	<b>Page</b>	<b>Description of Change</b>	<b>Date</b>
A	T3C	2	Added T3C F_SEL Function Table.	12/06/06
A	T9	13	Ordering Information - removed leaded devices. Updated data sheet format.	7/16/15



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(Rev.1.0 Mar 2020)

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