

## GENERAL DESCRIPTION

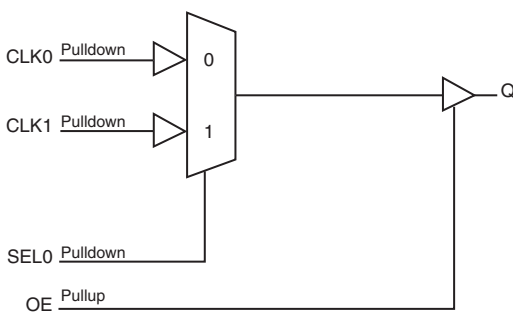
The 8CA3052I is a low skew, 2:1, Single-ended Multiplexer. The 8CA3052I has two selectable single-ended clock inputs and one single-ended clock output. The output has a  $V_{DDO}$  pin which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug. The device operates up to 250MHz and is packaged in an 8 TSSOP.

## FEATURES

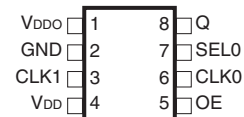
- 2:1 single-ended multiplexer
- Q nominal output impedance:  $15\Omega$  ( $V_{DDO} = 3.3V$ )
- Maximum output frequency: 250MHz
- Propagation delay: 2.7ns (maximum), ( $V_{DD} = V_{DDO} = 3.3V$ )
- Input skew: 160ps (maximum), ( $V_{DD} = V_{DDO} = 3.3V$ )
- Part-to-part skew: 490ps (maximum), ( $V_{DD} = V_{DDO} = 3.3V$ )
- Additive phase jitter, RMS at 155.52MHz (12kHz - 20MHz): 0.18ps (typical), ( $V_{DD} = V_{DDO} = 3.3V$ )
- Operating supply modes:  

$V_{DD} / V_{DDO}$
3.3V/3.3V
3.3V/2.5V
3.3V/1.8V
2.5V/2.5V
2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## BLOCK DIAGRAM



## PIN ASSIGNMENT



**8CA3052I**  
**8-Lead TSSOP**  
 4.40mm x 3.0mm x 0.925mm  
 package body  
**PG8 Package**  
 Top View

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	V <sub>DDO</sub>	Power		Output supply pin.
2	GND	Power		Power supply ground.
3, 6	CLK1, CLK0	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
4	V <sub>DD</sub>	Power		Positive supply pin.
5	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
7	SEL0	Input	Pulldown	Clock select input. See <i>Table 3. Control Input Function Table</i> . LVCMOS / LVTTL interface levels.
8	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)	V <sub>DDO</sub> = 3.465V		18		pF
		V <sub>DDO</sub> = 2.625V		19		pF
		V <sub>DDO</sub> = 1.89V		19		pF
R <sub>OUT</sub>	Output Impedance			15		Ω

**TABLE 3. CONTROL INPUT FUNCTION TABLE**

Control Inputs	Input Selected to Q
SEL0	
0	CLK0
1	CLK1

### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	101.7°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$  OR  $1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
$I_{DD}$	Power Supply Current			40	mA	
$I_{DDO}$	Output Supply Current			5	mA	

**TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$  OR  $1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Voltage		2.375	2.5	2.625	V
			1.71	1.8	1.89	V
$I_{DD}$	Power Supply Current			36	mA	
$I_{DDO}$	Output Supply Current			5	mA	

**TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS,  $T_A = -40^{\circ}\text{C}$  TO  $85^{\circ}\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3\text{V} \pm 5\%$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5\text{V} \pm 5\%$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3\text{V} \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5\text{V} \pm 5\%$	-0.3		0.7	V
$I_{IH}$	Input High Current	CLK0, CLK1, SELO $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$			150	$\mu\text{A}$
		OE $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$			5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK0, CLK1, SELO $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$	-5			$\mu\text{A}$
		OE $V_{DD} = 3.3\text{V}$ or $2.5\text{V} \pm 5\%$	-150			$\mu\text{A}$
$V_{OH}$	Output High Voltage	$V_{DDO} = 3.3\text{V} \pm 5\%$ ; NOTE 1	2.6			V
		$V_{DDO} = 2.5\text{V} \pm 5\%$ ; NOTE 1	1.8			V
		$V_{DDO} = 1.8\text{V} \pm 5\%$ ; NOTE 1	$V_{DD} - 0.3$			V
$V_{OL}$	Output Low Voltage	$V_{DDO} = 3.3\text{V} \pm 5\%$ ; NOTE 1			0.5	V
		$V_{DDO} = 2.5\text{V} \pm 5\%$ ; NOTE 1			0.45	V
		$V_{DDO} = 1.8\text{V} \pm 5\%$ ; NOTE 1			0.35	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{DDO}/2$ . See Parameter Measurement section, "Load Test Circuit" diagrams.

**TABLE 5A. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 3.3\text{V} \pm 5\%$ ,  $T_A = -40^{\circ}\text{C}$  TO  $85^{\circ}\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$t_{pLH}$	Propagation Delay, Low to High; NOTE 1		2.0	2.4	2.7	ns
$t_{pHL}$	Propagation Delay, High to Low; NOTE 1		2.0	2.5	2.9	ns
$t_{sk(i)}$	Input Skew; NOTE 4			36	160	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 2, 4				490	ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.18		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: Driving only one input clock.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**TABLE 5B. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$tp_{LH}$	Propagation Delay, Low to High; NOTE 1		2.3	2.6	2.9	ns
$tp_{HL}$	Propagation Delay, High to Low; NOTE 1		2.3	2.6	2.9	ns
$tsk(i)$	Input Skew; NOTE 4			23	106	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				350	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.14		ps
$t_r / t_f$	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: Driving only one input clock.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**TABLE 5C. AC CHARACTERISTICS,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 5\%$ ,  $T_A = -40^\circ C$  TO  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$tp_{LH}$	Propagation Delay, Low to High; NOTE 1		2.3	3.1	3.9	ns
$tp_{HL}$	Propagation Delay, High to Low; NOTE 1		2.3	3.1	3.9	ns
$tsk(i)$	Input Skew; NOTE 4			19	66	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				350	ps
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.16		ps
$t_r / t_f$	Output Rise/Fall Time	20% to 80%	350		850	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: Driving only one input clock.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**TABLE 5D. AC CHARACTERISTICS,  $V_{DD} = V_{DDO} = 2.5V \pm 5\%$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$tp_{LH}$	Propagation Delay, Low to High; NOTE 1		2.2	2.7	3.2	ns
$tp_{HL}$	Propagation Delay, High to Low; NOTE 1		2.2	2.7	3.2	ns
$tsk(i)$	Input Skew; NOTE 4			28	123	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				400	ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.22		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: Driving only one input clock.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**TABLE 5E. AC CHARACTERISTICS,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 5\%$ ,  $T_A = -40^{\circ}C$  TO  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				250	MHz
$tp_{LH}$	Propagation Delay, Low to High; NOTE 1		2.1	3.1	4.1	ns
$tp_{HL}$	Propagation Delay, High to Low; NOTE 1		2.1	3.1	4.2	ns
$tsk(i)$	Input Skew; NOTE 4			19	73	ps
$tsk(pp)$	Part-to-Part Skew; NOTE 2, 4				350	ps
$t_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.19		ps
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	350		850	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from  $V_{DD}/2$  of the input to  $V_{DDO}/2$  of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at  $V_{DDO}/2$ .

NOTE 3: Driving only one input clock.

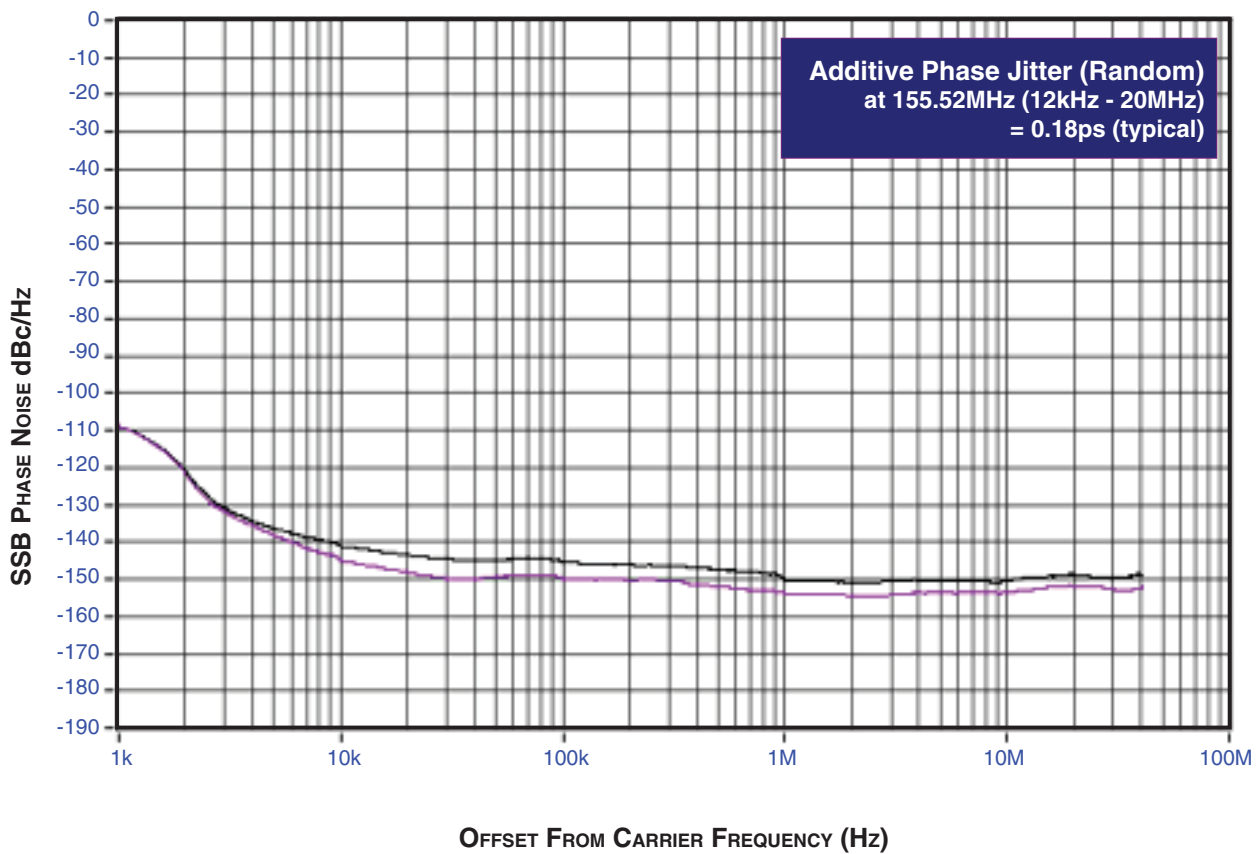
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels

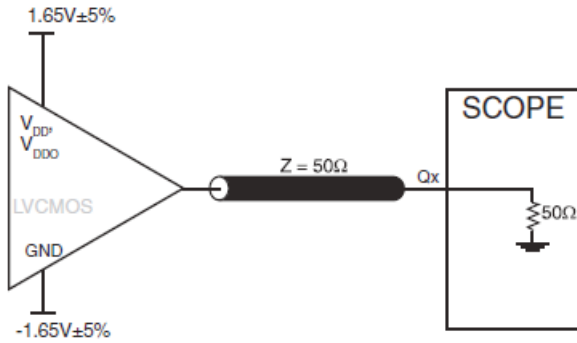
(dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



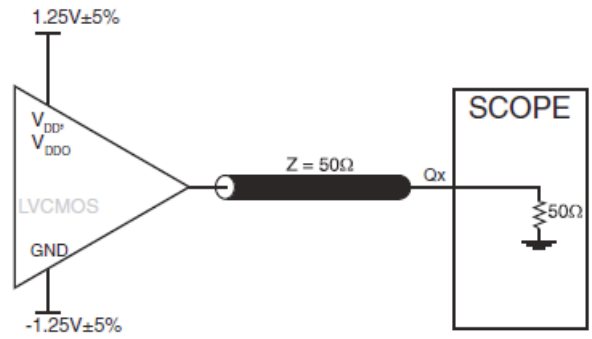
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device.

This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

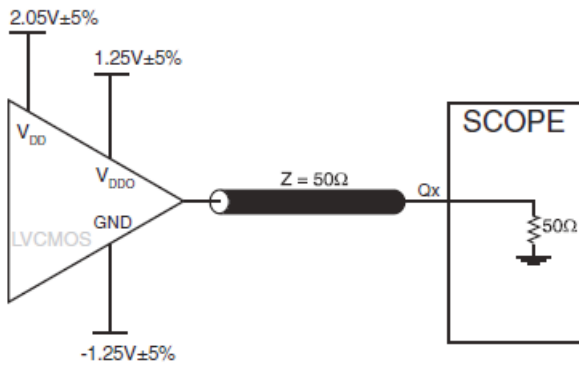
## PARAMETER MEASUREMENT INFORMATION



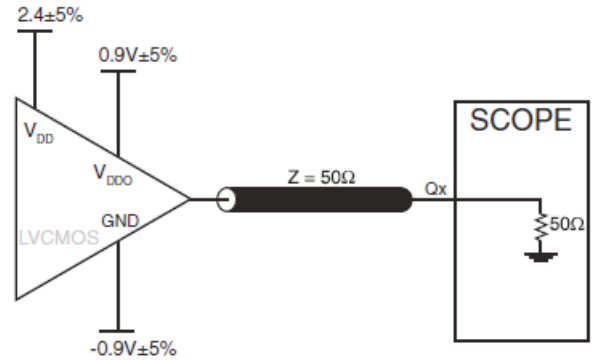
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



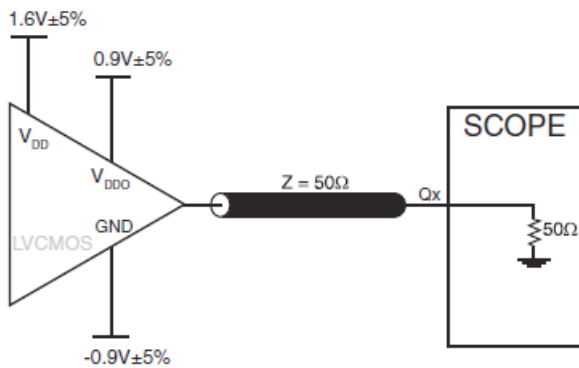
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT

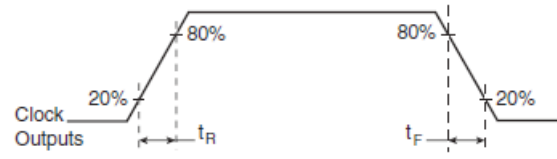
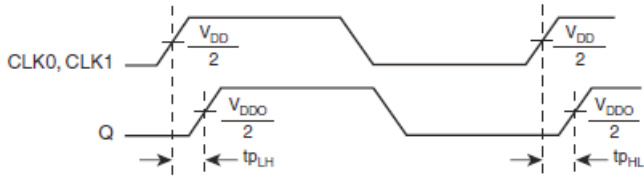


2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



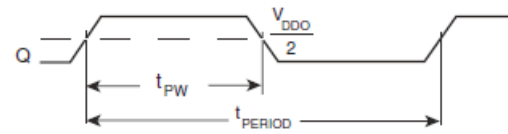
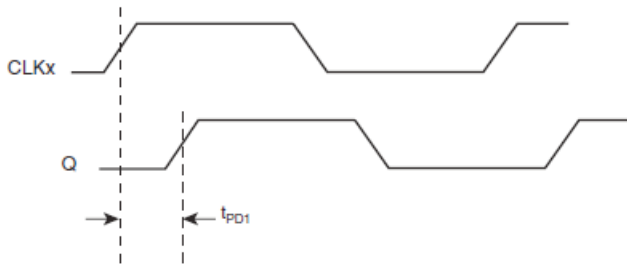
PART-TO-PART SKEW





**PROPAGATION DELAY**

**OUTPUT RISE/FALL TIME**



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

$$tsk(l) = |t_{PD2} - t_{PD1}|$$

**INPUT SKEW**

**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**

## APPLICATIONS INFORMATION

### RECOMMENDATIONS FOR UNUSED INPUT PINS

#### INPUTS:

##### CLK INPUT:

For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the CLK input to ground.

##### CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8CA3052I. Equations and example calculations are also provided.

### 1. Power Dissipation

The total power dissipation for the 8CA3052I is the sum of the core power plus the analog power plus the power dissipated in the load(s).

The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

#### Core and LVDS Output Power Dissipation

- Power (core)<sub>MAX</sub> -  $V_{DD\_MAX} * (I_{DD} + I_{DDO}) = 3.465V * (40mA + 5mA) = \mathbf{155.93mW}$

- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DD}/2$

$$\text{Output Current } I_{OUT} = V_{DDO\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465 / [2 * (50\Omega + 15\Omega)] = \mathbf{26.7mA}$$

- Power Dissipation on the  $R_{OUT}$  per LVCMOS output

$$\text{Power } (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 15\Omega * (26.7mA)^2 = \mathbf{10.7mW}$$

#### Dymanic Power Dissipation at 250MHz

- Power (250MHz) =  $C_{PD} * \text{frequency} * (V_{DD})^2 = 18pF * 250MHz * (3.465V)^2 = \mathbf{54.0mW}$

#### Total Power Dissipation

- Total Power

$$= \text{Power (core)}_{MAX} + \text{Power } (R_{OUT}) \text{ Total Power} + \text{Power (250MHz)}$$

$$= 155.93mW + 10.7mW + 54.0mW$$

$$= \mathbf{220.6mW}$$

## 2. Junction Temperature

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1, above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 101.7°C/W per Table 6.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.221\text{W} * 101.7^\circ\text{C}/\text{W} = 107.4^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

## RELIABILITY INFORMATION

TABLE 6.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 8 LEAD TSSOP

$\theta_{JA}$ by Velocity			
Meters per second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

### TRANSISTOR COUNT

The transistor count for 8CA3052I is: 967

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

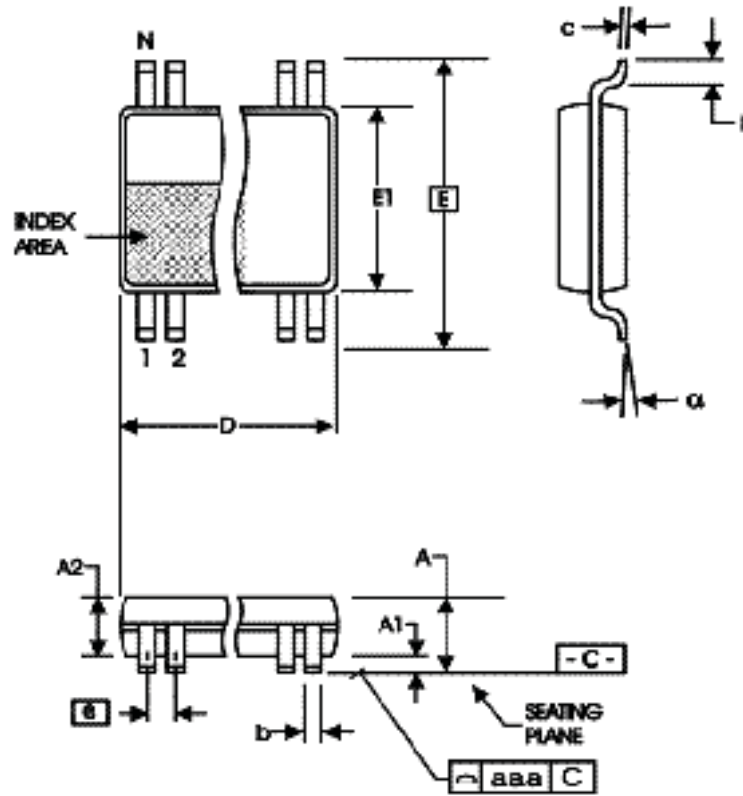


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
$\alpha$	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 8. ORDERING INFORMATION**

<b>Part/Order Number</b>	<b>Marking</b>	<b>Package</b>	<b>Shipping Packaging</b>	<b>Temperature</b>
8CA3052APGGI	52AGI	8-lead "Lead Free" TSSOP	Tube	-40°C to +85°C
8CA3052APGGI8	52AGI	8-lead "Lead Free" TSSOP	Tape and Reel	-40°C to +85°C

**REVISION HISTORY SHEET**

<b>Rev</b>	<b>Table</b>	<b>Page</b>	<b>Description of Change</b>	<b>Date</b>
A			Initial Release by Willner	6/15/12
A	T8	1 15	Removed IDT from part numbers where needed. Features section - removed reference to leaded packages. Ordering Information - deleted G note below table. Updated header and footer.	1/27/16





## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.