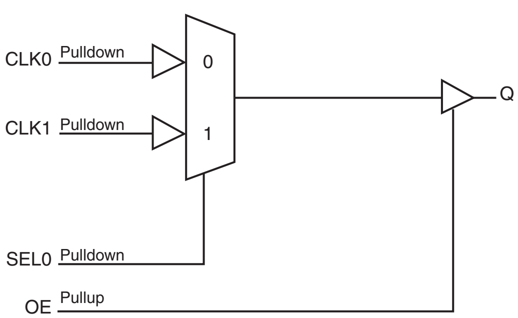
General Description

The 8CA3052I is a low skew, 2:1, Single-ended Multiplexer. The 8CA3052I has two selectable single-ended clock inputs and one single-ended clock output. The output has a V_{DDO} pin which may be set at 3.3V, 2.5V, or 1.8V, making the device ideal for use in voltage translation applications. An output enable pin places the output in a high impedance state which may be useful for testing or debug. The device operates up to 250MHz and is packaged in an 8 TSSOP.

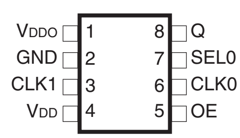
Features

- 2:1 single-ended multiplexer
- Q nominal output impedance: 15Ω (V_{DDO} = 3.3V)
- Maximum output frequency: 250MHz
- Propagation delay: 2.7ns (maximum), (V_{DD} = V_{DDO} = 3.3V)
- Input skew: 160ps (maximum), (V_{DD} = V_{DDO} = 3.3V)
- Part-to-part skew: 490ps (maximum), (V_{DD} = V_{DDO} = 3.3V)
- Additive phase jitter, RMS at 155.52MHz (12kHz - 20MHz): 0.18ps (typical), (V_{DD} = V_{DDO} = 3.3V)
- Operating supply modes:
  V_{DD}/V_{DDO}
  3.3V/3.3V
  3.3V/2.5V
  3.3V/1.8V
  2.5V/2.5V
  2.5V/1.8V
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment



8CA3052I

8-Lead TSSOP
4.40mm x 3.0mm x 0.925mm
package body
PG8 Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	V_{DDO}	Power		Output supply pin.
2	GND	Power		Power supply ground.
3, 6	CLK1, CLK0	Input	Pulldown	Single-ended clock inputs. LVCMOS/LVTTL interface levels.
4	V_{DD}	Power		Positive supply pin.
5	OE	Input	Pullup	Output enable. When LOW, outputs are in HIGH impedance state. When HIGH, outputs are active. LVCMOS / LVTTL interface levels.
7	SEL0	Input	Pulldown	Clock select input. See *Table 3. Control Input Function Table.* LVCMOS / LVTTL interface levels.
8	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
C_{PD}	Power Dissipation Capacitance (per output)	V_{DDO} = 3.465V		18		pF
		V_{DDO} = 2.625V		19		pF
		V_{DDO} = 1.89V		19		pF
R_{OUT}	Output Impedance			15		Ω

TABLE 3. CONTROL INPUT FUNCTION TABLE

Control Inputs	Input Selected to Q
SEL0	
0	CLK0
1	CLK1

Absolute Maximum Ratings

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	101.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V±5%, V_{DDO} = 3.3V±5%, 2.5V±5% or 1.8V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current				40	mA
I_{DDO}	Output Supply Current				5	mA

Table 4B. Power Supply DC Characteristics, V_{DD} = 2.5V±5%, V_{DDO} = 2.5V±5% or 1.8V±5%, TA = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
			1.71	1.8	1.89	V
I_{DD}	Power Supply Current				36	mA
I_{DDO}	Output Supply Current				5	mA

TABLE 4C. LVCMOS/LVTTL DC CHARACTERISTICS, T_A = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V ± 5%	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V ± 5%	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V ± 5%	-0.3		0.8	V
			V_{DD} = 2.5V ± 5%	-0.3		0.7	V
I_{IH}	Input High Current	CLK0, CLK1, SEL0	V_{DD} = 3.3V or 2.5V ± 5%			150	µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%			5	µA
I_{IL}	Input Low Current	CLK0, CLK1, SEL0	V_{DD} = 3.3V or 2.5V ± 5%	-5			µA
		OE	V_{DD} = 3.3V or 2.5V ± 5%	-150			µA
V_{OH}	Output HighVoltage		V_{DDO} = 3.3V ± 5%; NOTE 1	2.6			V
			V_{DDO} = 2.5V ± 5%; NOTE 1	1.8			V
			V_{DDO} = 1.8V ± 5%; NOTE 1	V_{DD} - 0.3			V
V_{OL}	Output Low Voltage		V_{DDO} = 3.3V ± 5%; NOTE 1			0.5	V
			V_{DDO} = 2.5V ± 5%; NOTE 1			0.45	V
			V_{DDO} = 1.8V ± 5%; NOTE 1			0.35	V

NOTE 1: Outputs terminated with 50Ω to V_{DDO}/2. See Parameter Measurement section, "Load Test Circuit" diagrams.

TABLE 5A. AC CHARACTERISTICS, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.0	2.4	2.7	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.0	2.5	2.9	ns
*t*sk(i)	Input Skew; NOTE 4			36	160	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				490	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.18		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: Driving only one input clock.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

TABLE 5B. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.3	2.6	2.9	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.3	2.6	2.9	ns
*t*sk(i)	Input Skew; NOTE 4			23	106	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				350	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.14		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: Driving only one input clock.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

TABLE 5C. AC CHARACTERISTICS, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.3	3.1	3.9	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.3	3.1	3.9	ns
*t*sk(i)	Input Skew; NOTE 4			19	66	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				350	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.16		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		850	ps
odc	Output Duty Cycle		46		54	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: Driving only one input clock.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

TABLE 5D. AC CHARACTERISTICS, $V_{DD} = V_{DDO}$ = 2.5V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.2	2.7	3.2	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.2	2.7	3.2	ns
*t*sk(i)	Input Skew; NOTE 4			28	123	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				400	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.22		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		700	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: Driving only one input clock.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

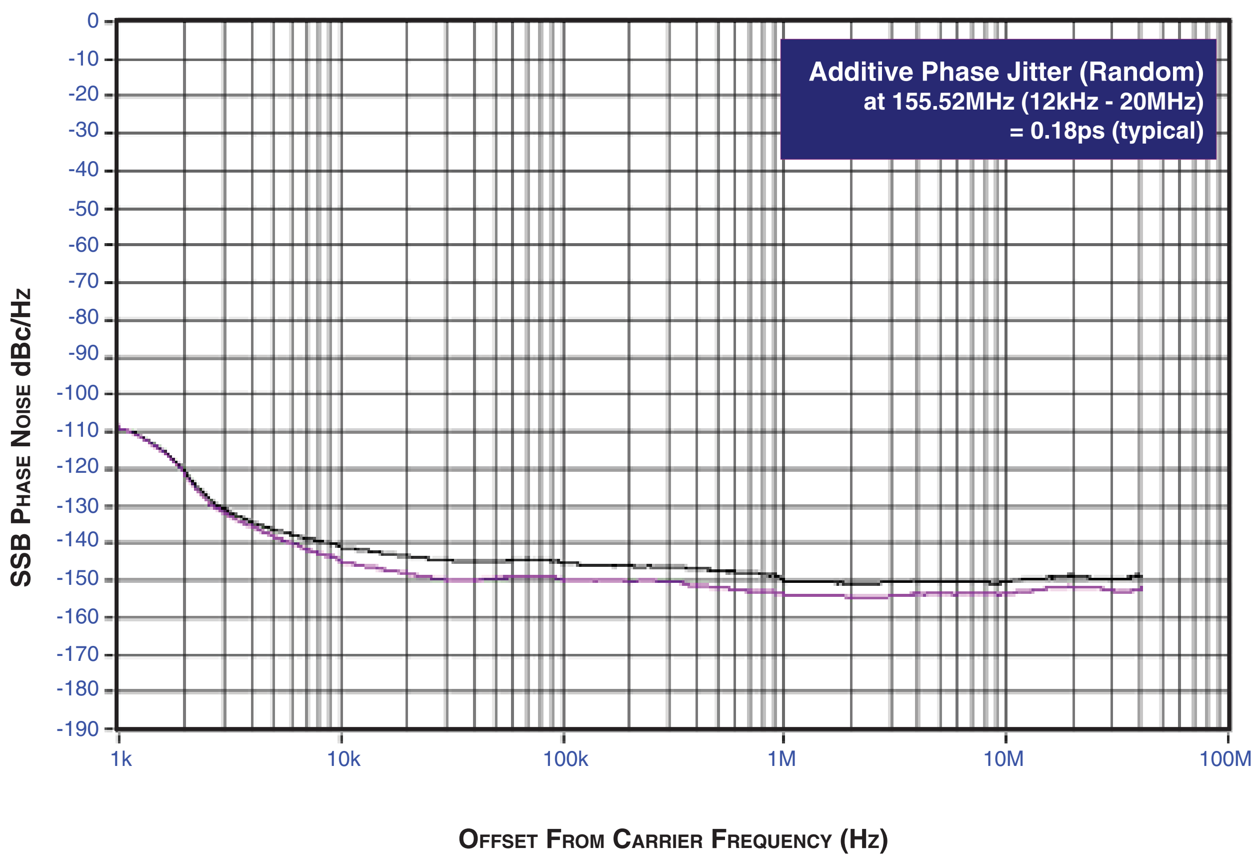
TABLE 5E. AC CHARACTERISTICS, V_{DD} = 2.5V ± 5%, V_{DDO} = 1.8V ± 5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
tp_{LH}	Propagation Delay, Low to High; NOTE 1		2.1	3.1	4.1	ns
tp_{HL}	Propagation Delay, High to Low; NOTE 1		2.1	3.1	4.2	ns
*t*sk(i)	Input Skew; NOTE 4			19	73	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 2, 4				350	ps
*t*jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section, NOTE 3	155.52MHz, Integration Range: 12kHz - 20MHz		0.19		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	350		850	ps
odc	Output Duty Cycle		45		55	%
$MUX_{ISOLATION}$	MUX Isolation			45		dB

NOTE 1: Measured from V_{DD}/2 of the input to V_{DDO}/2 of the output.
NOTE 2: Defined as skew between outputs on different devices operating a the same supply voltages and with equal load conditions. Using the same type of input on each device, the output is measured at V_{DDO}/2.
NOTE 3: Driving only one input clock.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.
NOTE: Electrical parameters are guaranteed over the specified ambient operating range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

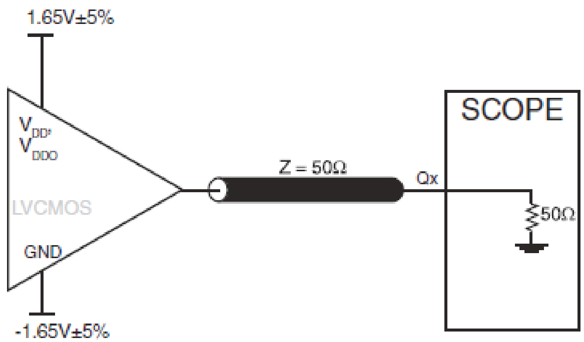
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

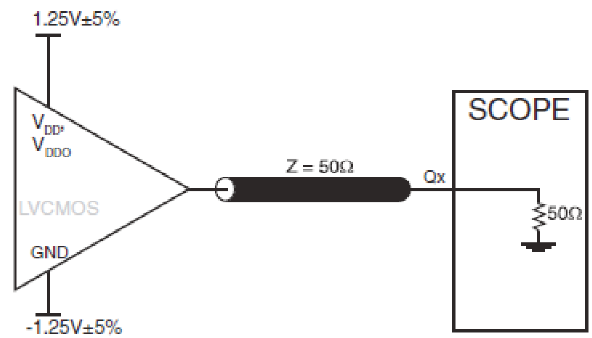


As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

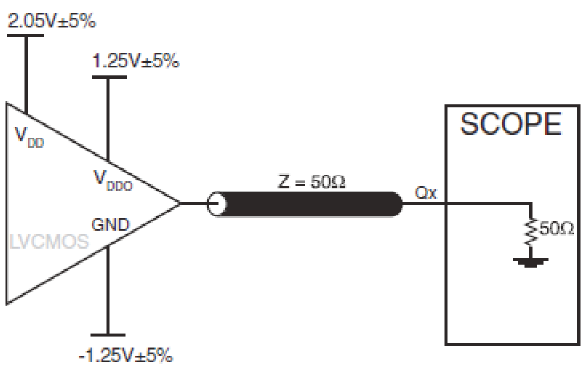
PARAMETER MEASUREMENT INFORMATION



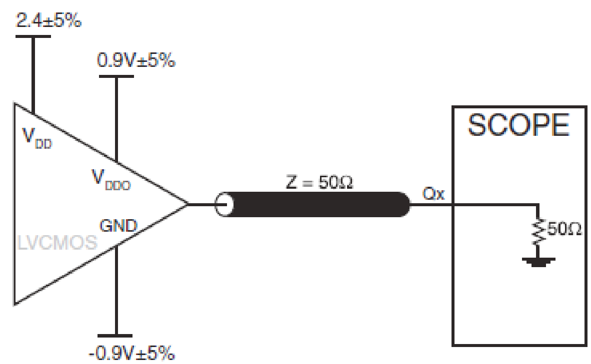
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



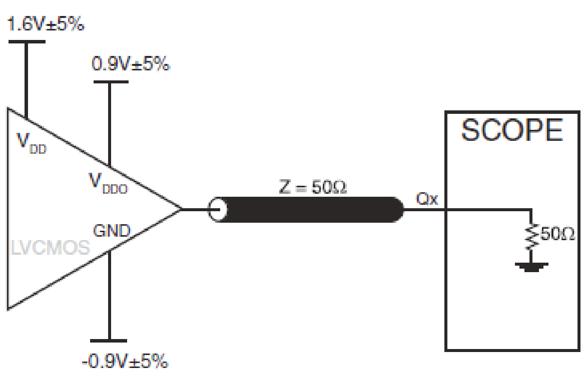
2.5V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



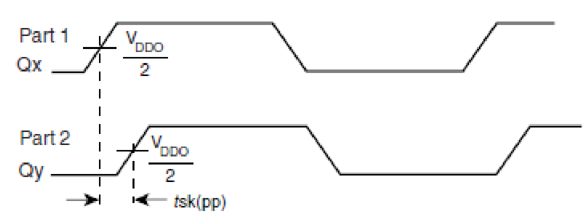
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



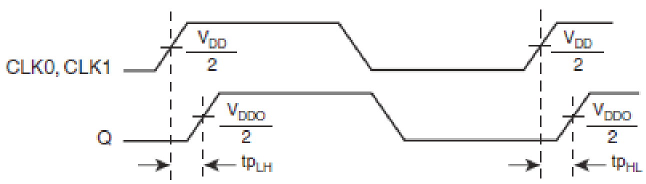
3.3V CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



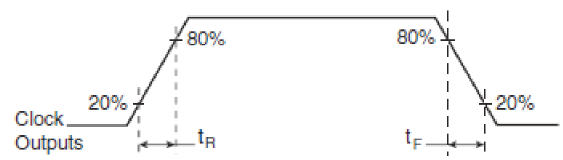
2.5 CORE/1.8V OUTPUT LOAD AC TEST CIRCUIT



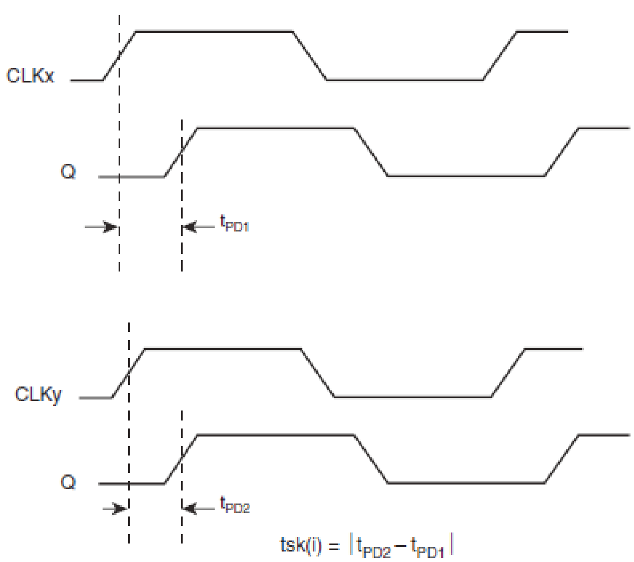
PART-TO-PART SKEW



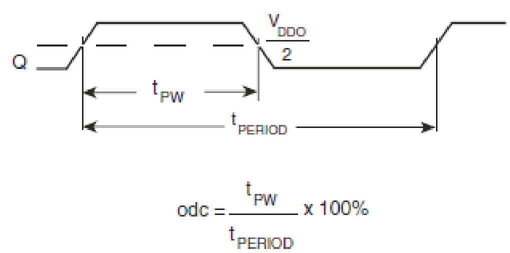
Propagation Delay



Output Rise/Fall Time



Input Skew



Output Duty Cycle/Pulse Width/Period

Applications Information

Recommendations for Unused Input Pins

Inputs:

CLK Input:
For applications not requiring the use of the test clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK input to ground.

Control Pins:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 8CA3052I. Equations and example calculations are also provided.

1. Power Dissipation

The total power dissipation for the 8CA3052I is the sum of the core power plus the analog power plus the power dissipated in the load(s).

The following is the power dissipation for V_{DD} = 3.3V + 5% =3.465V, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power $(core)_{MAX}$ - V_{DD_MAX} * (I_{DD} + I_{DDO}) = 3.4565V * (40mA + 5mA) = **155.93mW**

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DD}/2

  Output Current I_{OUT} = V_{DDO_MAX}/[2 * (50Ω + R_{OUT})] = 3.465 / [2 * (50Ω +15Ω)] = **26.7mA**

- Power Dissipation on the R_{OUT} per LVCMOS output

  Power (R_{OUT}) = R_{OUT} * $(I_{OUT})^2$ = 15Ω * $(26.7mA)^2$ = **10.7mW**

Dymanic Power Dissipation at 250MHz

- **Power (250MHz)** = C_{PD} * frequency * $(V_{DD})^2$ = 18pF * 250MHz * $(3.465V)^2$ = **54.0mW**

Total Power Dissipation

- **Total Power**

  = Power $(core)_{MAX}$ + Power (R_{OUT}) Total Power + Power (250MHz)

  = 155.93mW + 10.7mW + 54.0mW

  = **220.6mW**

2. Junction Temperature

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction, TJ, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1, above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 101.7°C/W per Table 6.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.221W * 101.7°C/W = 107.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for 8 Lead TSSOP

θ_{JA} by Velocity			
Meters per second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

Transistor Count

The transistor count for 8CA3052I is: 967

PACKAGE OUTLINE - G SUFFIX FOR 8 LEAD TSSOP

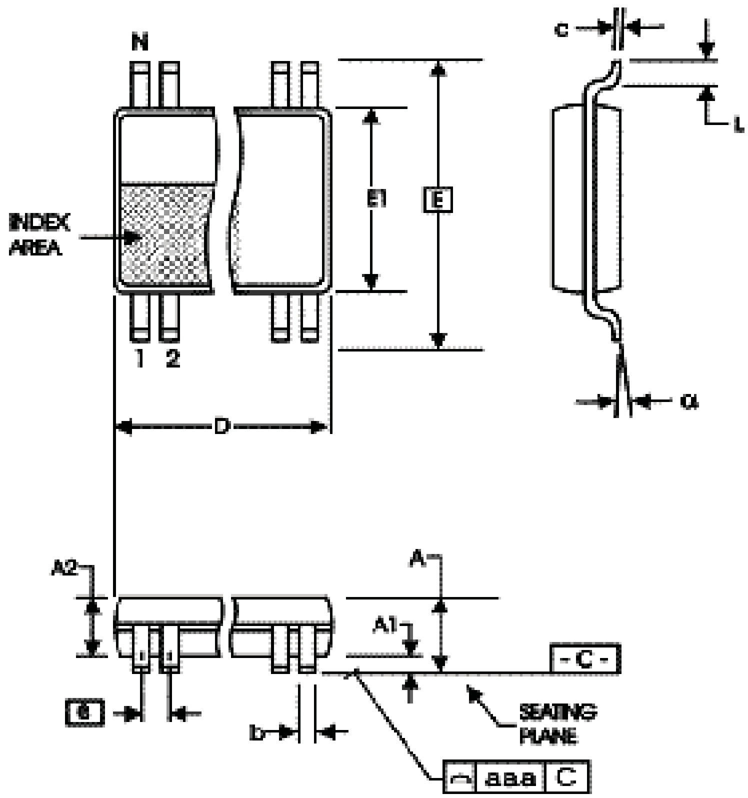


TABLE 7. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	8	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8CA3052APGGI	52AGI	8-lead “Lead Free” TSSOP	Tube	-40°C to +85°C
8CA3052APGGI8	52AGI	8-lead “Lead Free” TSSOP	Tape and Reel	-40°C to +85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A			Initial Release by Willner	6/15/12
A	T8	1 15	Removed IDT from part numbers where needed. Features section - removed reference to leaded packages. Ordering Information - deleted G note below table. Updated header and footer.	1/27/16

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