

## Description

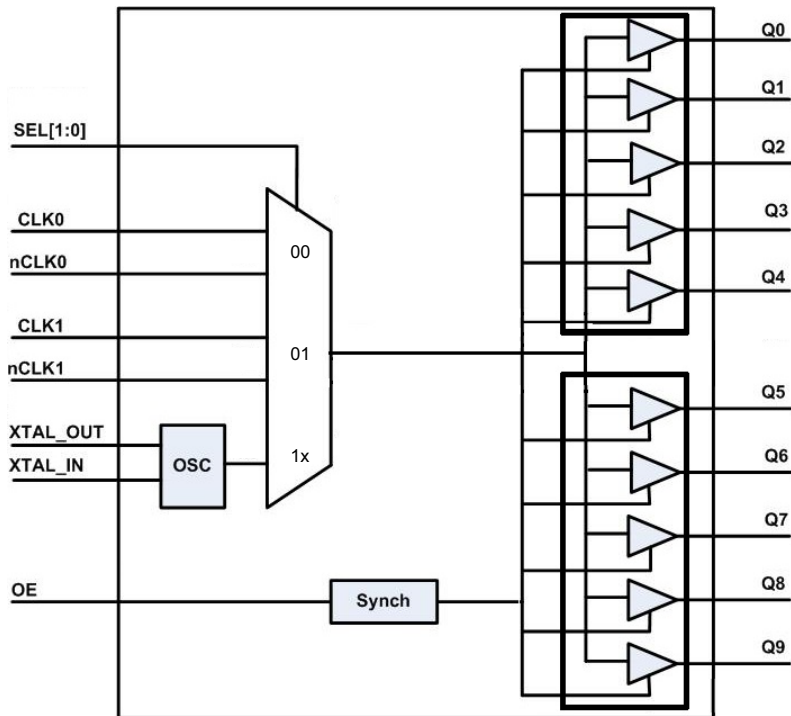
The 8L30210 is a low skew, 1-to-10 LVCMOS / LVTTTL Fanout Buffer. The low impedance LVCMOS/LVTTTL outputs are designed to drive 50Ω series, or parallel terminated transmission lines.

The 8L30210 is characterized at full 3.3V, 2.5V, and mixed 3.3V/2.5V, 3.3V/1.8V, 3.3V/1.5V, 2.5V/1.8V and 2.5V/1.5V output operating supply modes. The input clock is selected from two differential clock inputs or a crystal input. The differential inputs can be wired to accept a single-ended input. The internal oscillator circuit is automatically disabled when the crystal input is de-selected.

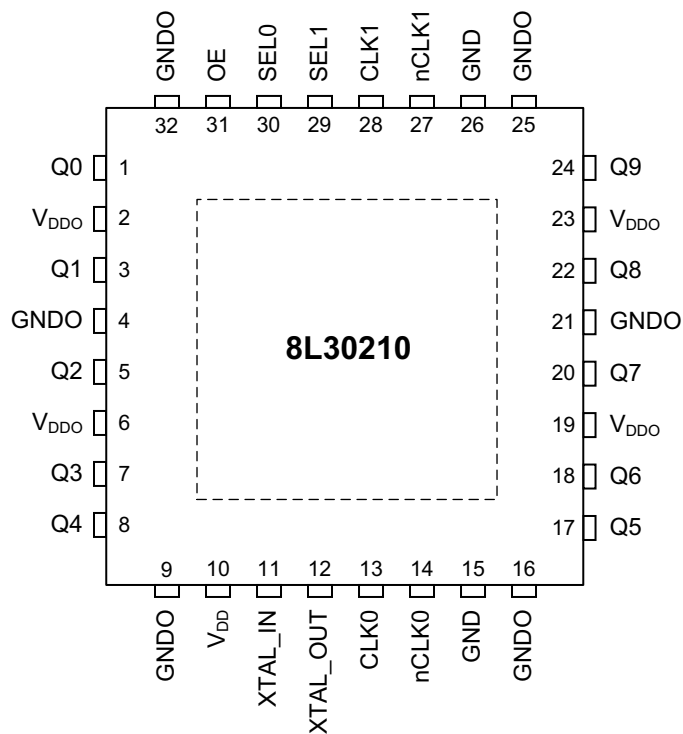
## Features

- Ten LVCMOS / LVTTTL outputs up to 200MHz
- Differential input pairs can accept the following differential input levels: LVPECL, LVDS, HCSL
- Crystal oscillator interface
- Crystal input frequency range: 10MHz to 40MHz
- Additive RMS phase jitter: 30fs (typical)
- Synchronous output enable to avoid clock glitch
- Power supply modes:  
Core / Output  
3.3V / 3.3V  
2.5V / 2.5V  
3.3V / 2.5V  
3.3V / 1.8V  
3.3V / 1.5V  
2.5V / 1.8V  
2.5V / 1.5V
- Supports case temperature up to 105°C
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignments



**32-pin, 5mm x 5mm VFQFN Package**

## Pin Characteristics

**Table 1. Pin Descriptions<sup>[a]</sup>**

Number	Name	Type		Description
1	Q0	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
2	V <sub>DDO</sub>	Power		Output power supply pin for Bank A.
3	Q1	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
4	GND0	Power		Power supply output ground.
5	Q2	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
6	V <sub>DDO</sub>	Power		Output power supply pin for Bank A.
7	Q3	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	Q4	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
9	GND0	Power		Power supply output ground.
10	V <sub>DD</sub>	Power		Power supply pin.
11	XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input.
12	XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output.
13	CLK0	Input	Pulldown	Non-inverting differential clock.
14	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to V <sub>DD</sub> /2.
15	GND	Power		Power supply core ground.

**Table 1. Pin Descriptions<sup>[a]</sup> (Cont.)**

Number	Name	Type		Description
16	GNDO	Power		Power supply output ground.
17	Q5	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
18	Q6	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
19	V <sub>DDO</sub>	Power		Output power supply pin for Bank B.
20	Q7	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
21	GNDO	Power		Power supply output ground.
22	Q8	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
23	V <sub>DDO</sub>	Power		Output power supply pin for Bank B.
24	Q9	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
25	GNDO	Power		Power supply output ground.
26	GND	Power		Power supply core ground.
27	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock. Internal resistor bias to V <sub>DD</sub> /2.
28	CLK1	Input	Pulldown	Non-inverting differential clock.
29	SEL1	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See <a href="#">Table 3A</a> .
30	SEL0	Input	Pulldown	Input clock selection. LVCMOS/LVTTL interface levels. See <a href="#">Table 3A</a> .
31	OE	Input	Pulldown	Output enable. LVCMOS/LVTTL interface levels. See <a href="#">Table 3B</a> .
32	GNDO	Power		Power supply output ground.
ePad	Exposed Pad	Power		Must be connected to GND.

[a] *Pullup and Pulldown* refer to internal input resistors. See [Table 2, Pin Characteristics](#), for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance	CLK[0:1], nCLK[0:1], SEL[1:0], OE			2		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor				51		kΩ
R <sub>PULLUP</sub>	Input Pullup Resistor				51		kΩ
C <sub>PD</sub>	Power Dissipation Capacitance (per output)		V <sub>DDO</sub> = 3.465V		11		pF
			V <sub>DDO</sub> = 2.625V		9		pF
			V <sub>DDO</sub> = 1.95V		8		pF
			V <sub>DDO</sub> = 1.6V		8		pF
R <sub>OUT</sub>	Output Impedance		V <sub>DDO</sub> = 3.3V ± 5%		40		Ω
			V <sub>DDO</sub> = 2.5V ± 5%		40		Ω
			V <sub>DDO</sub> = 1.8V ± 0.15V		50		Ω
			V <sub>DDO</sub> = 1.5V ± 0.1V		55		Ω

## Function Tables

**Table 3A. SELx Function Table**

Control Input	Selected Input Clock
SEL[1:0]	
00 (default)	CLK0, nCLK0
01	CLK1, nCLK1
11 or 10	XTAL

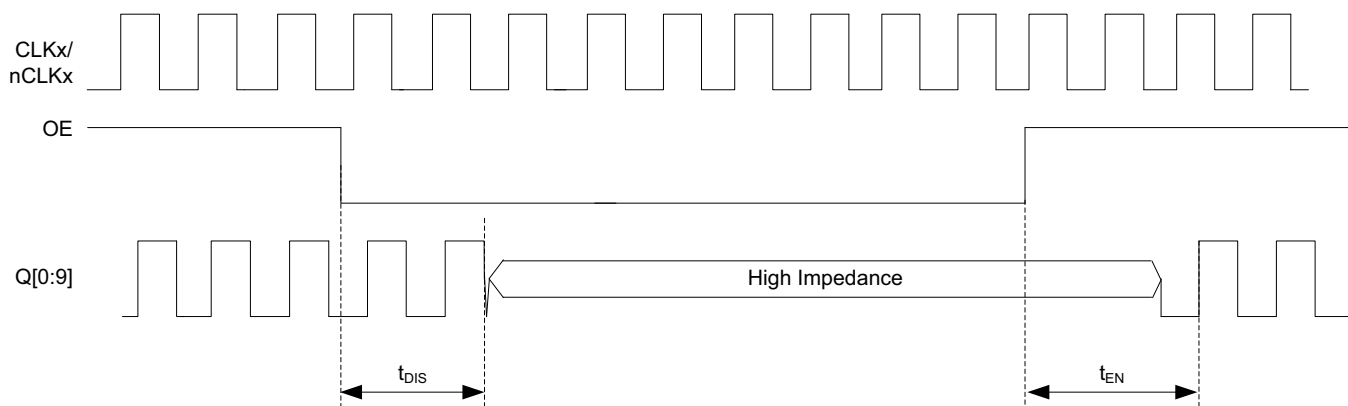
**Table 3B. OE Function Table**

Control Input	Function
OE	Q[0:9]
0 (default)	High-Impedance
1	Enabled

**Table 3C. Input/Output Operation Table<sup>[a]</sup>**

Input State			Output State
OE	SEL[1:0]	CLK[0:1], nCLK[0:1]	Q[0:9]
0	X	Do Not Care	High-Impedance
1	10 or 11	Do Not Care	Active
1	00	CLK0 = nCLK0 = Open	LOW
		CLK0 = HIGH, nCLK0 = LOW	HIGH
		CLK0 = LOW, nCLK0 = HIGH	LOW
1	01	CLK1 = nCLK1 = Open	LOW
		CLK1 = HIGH, nCLK1 = LOW	HIGH
		CLK1 = LOW, nCLK1 = HIGH	LOW

[a] The device must have switching edge to obtain output states.



**Figure 1. OE Timing Diagram**

NOTE: The outputs will enable or disable 2 to 3 clock cycles after the transition on the OE input.

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	3.6V
Inputs, $V_I$ CLK <sub>X</sub> , nCLK <sub>X</sub> XTAL_IN Other Inputs	3.6V 0V to 2V -0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Junction Temperature, $T_J$	125°C
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$  or  $1.8V \pm 0.15V$  or  $1.5V \pm 0.1V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		3.135	3.3	3.465	V
			2.375	2.5	2.625	V
			1.65	1.8	1.95	V
			1.4	1.5	1.6	V
$I_{DD}$	Power Supply Current	No Clock Input, Outputs Unloaded			19	mA
$I_{DDO}$	Output Supply Current	OE = 1, $V_{DDO} = 3.3V \pm 5\%$ , Outputs Unloaded			3	mA
		OE = 1, $V_{DDO} = 2.5V \pm 5\%$ , Outputs Unloaded			2	mA
		OE = 1, $V_{DDO} = 1.8V \pm 0.15V$ , Outputs Unloaded			2	mA
		OE = 1, $V_{DDO} = 1.5V \pm 0.1V$ , Outputs Unloaded			2	mA

**Table 4B. Power Supply DC Characteristics,  $V_{DD} = 2.5V \pm 5\%$ ,  $V_{DDO} = 2.5V \pm 5\%$  or  $1.8V \pm 0.15V$  or  $1.5V \pm 0.1V$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		2.375	2.5	2.625	V
$V_{DDO}$	Output Supply Current		2.375	2.5	2.625	V
			1.65	1.8	1.95	V
			1.4	1.5	1.6	V
$I_{DD}$	Power Supply Current	No Clock Input, Outputs Unloaded			19	mA
$I_{DDO}$	Output Supply Current	OE = 1, $V_{DDO} = 2.5V \pm 5\%$ , Outputs Unloaded			2	mA
		OE = 1, $V_{DDO} = 1.8V \pm 0.15V$ , Outputs Unloaded			2	mA
		OE = 1, $V_{DDO} = 1.5V \pm 0.1V$ , Outputs Unloaded			2	mA

**Table 4C. LVCMOS/LVTTL DC Characteristics,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V \pm 5\%$	2.2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V \pm 5\%$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V \pm 5\%$	-0.3		0.8	V
		$V_{DD} = 2.5V \pm 5\%$	-0.3		0.7	V
$I_{IH}$	Input High Current	OE, SEL[1:0] $V_{DD} = V_{IN} = 3.465V$			150	$\mu\text{A}$
$I_{IL}$	Input Low Current	OE, SEL[1:0] $V_{DD} = 3.465V, V_{IN} = 0V$	-5			$\mu\text{A}$
$V_{OH}$	Output High Voltage	$I_{OH} = -100\mu\text{A}$	$V_{DDO} - 0.1$			V
$V_{OL}$	Output Low Voltage	$I_{OL} = 100\mu\text{A}$			0.1	V

**Table 4D. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK[0:1], nCLK[0:1]	$V_{DD} = V_{IN} = 3.465V$ or $2.625V$		150	$\mu A$
$I_{IL}$	Input Low Current	CLK[0:1]	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5		$\mu A$
		nCLK[0:1]	$V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage <sup>[a]</sup>		0.15		1.5	V
$V_{CMR}$	Common Mode Input Voltage <sup>[a], [b]</sup>		0.5		$V_{DD} - 0.85$	V

[a]  $V_{IL}$  should not be less than  $-0.3V$ .

[b] Common mode voltage is defined at the crosspoint.

**Table 5. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		10		40	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Load Capacitance			12	18	pF

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $V_{DDO} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$  or  $1.8V \pm 0.15V$  or  $1.5V \pm 0.1V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$ <sup>[a], [b]</sup>**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	Using External Crystal		10		40	MHz
		Using External Clock Source				200	MHz
$t_{PD}$	Propagation Delay <sup>[c]</sup>		$V_{DDO} = 3.3V \pm 5\%$	1.3		2.7	ns
			$V_{DDO} = 2.5V \pm 5\%$	1.4		3.0	ns
			$V_{DDO} = 1.8V \pm 0.15V$	1.7		4.0	ns
			$V_{DDO} = 1.5V \pm 0.1V$	2.0		5.0	ns
$t_{sk(o)}$	Output Skew <sup>[d], [e]</sup>		Referenced to Q0			55	ps
$t_{sk(b)}$	Bank Skew <sup>[e], [f]</sup>	Bank A				25	ps
		Bank B				40	ps
$t_{jit}$	Buffer Additive Phase Jitter	Input Clock from CLK0, nCLK0 or CLK1, nCLK1	$f_{OUT} = 156.25MHz$ , Integration Range: 12kHz - 20MHz		30		fs
$t_{jit}(\emptyset)$	RMS Phase Jitter	Input Clock from 25MHz Crystal	Integration Range: 12kHz - 5MHz		175		fs
$t_R / t_F$	Output Rise/Fall Time		$f_{OUT} = 156.25MHz$ , 20% - 80%			700	ps
odc	Output Duty Cycle		50% Input Duty Cycle, $f_{OUT} = 156.25MHz$	45		55	%
MUX_ISOLATION	MUX Isolation <sup>[g]</sup>		@ 156.25MHz		-84		dB
PSRR	Power Supply Rejection Ratio <sup>[h]</sup>				-70		dBc

[a] Typical values represent the part performance at  $V_{DD} = V_{DDO} = 3.3V$ ,  $T_A = 25^\circ C$  unless otherwise stated.

[b] Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

[c] Measured from the differential input crossing point to  $V_{DDO}/2$  of the output.

[d] Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at  $V_{DDO}/2$ .

[e] This parameter is defined in accordance with JEDEC Standard 65.

[f] Defined as skew within a bank with equal load conditions.

[g] These parameters are guaranteed by characterization. Not tested in production.

[h] 100kHz, 100mVpp Ripple Injected on  $V_{DDO} = 2.5V$ .



## Applications Information

### Recommendations for Unused Input and Output Pins

Inputs:

#### **CLK/nCLK Inputs**

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from CLK to ground.

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

#### LVC MOS Control Pins

All control pins have internal pulldowns; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

Outputs:

#### **LVC MOS Outputs**

All unused LVC MOS outputs can be left floating. IDT recommends that there be no trace attached.

## Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{DD} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_{REF}$  at 1.25V. The values below are for when both the single ended swing and  $V_{DD}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{DD} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

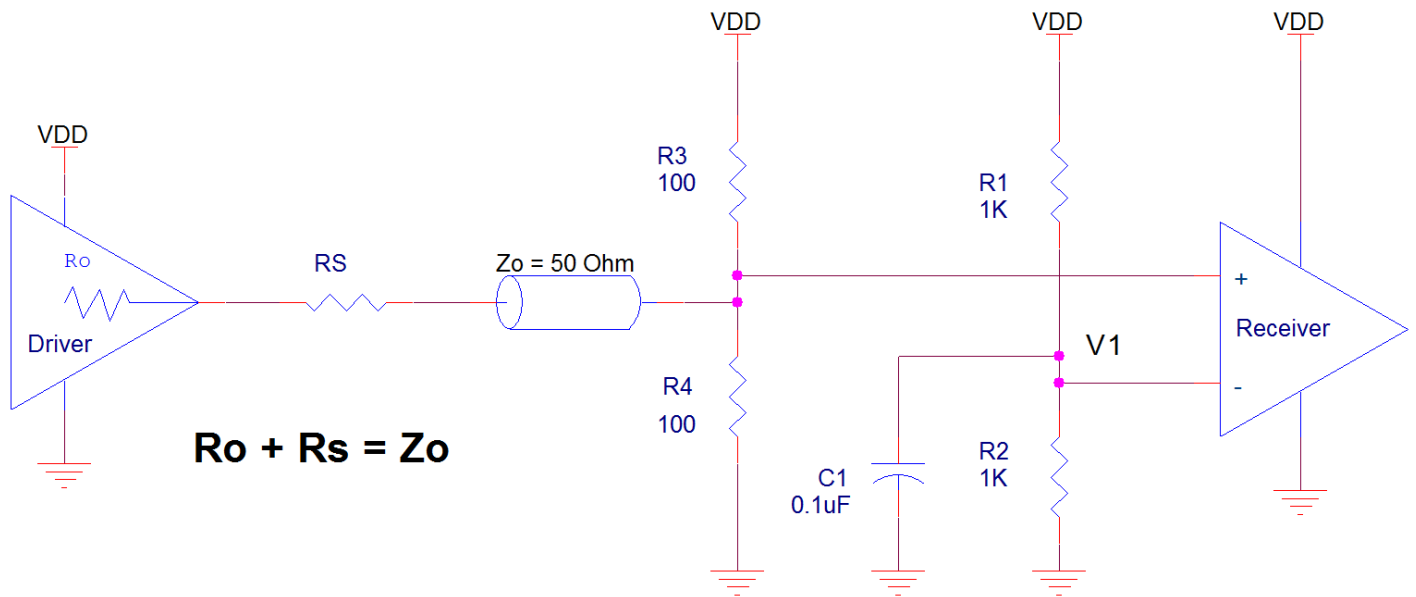


Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

## Crystal Input Interface

The 8L30210 has been characterized with 12pF parallel resonant crystals. The capacitor values, C1 and C2, shown in Figure 3 below was determined using a 12pF parallel resonant crystal, and was chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

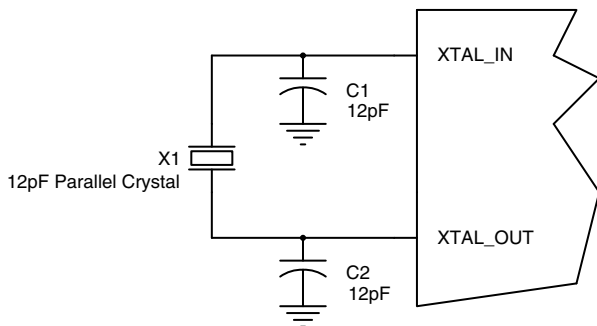


Figure 3. Crystal Input Interface

## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 4A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 4B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

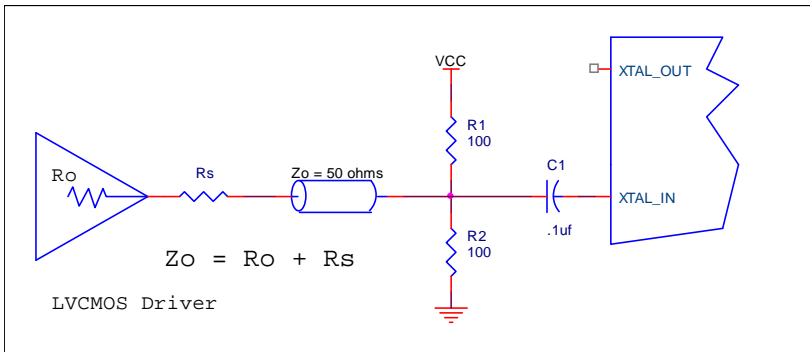


Figure 4A. General Diagram for LVCMOS Driver to XTAL Input Interface

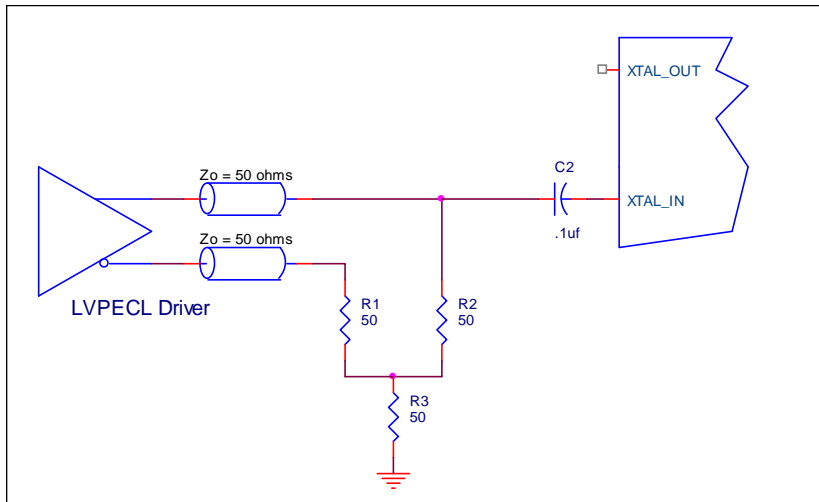


Figure 4B. General Diagram for LVPECL Driver to XTAL Input Interface

## Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both signals must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 5A to 5D show interface examples for the CLK /nCLK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

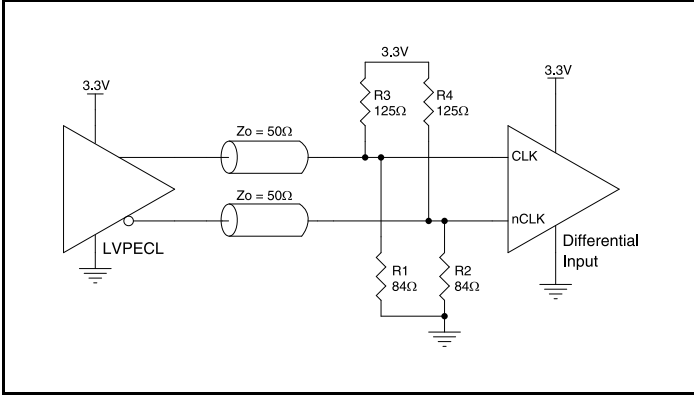


Figure 5A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

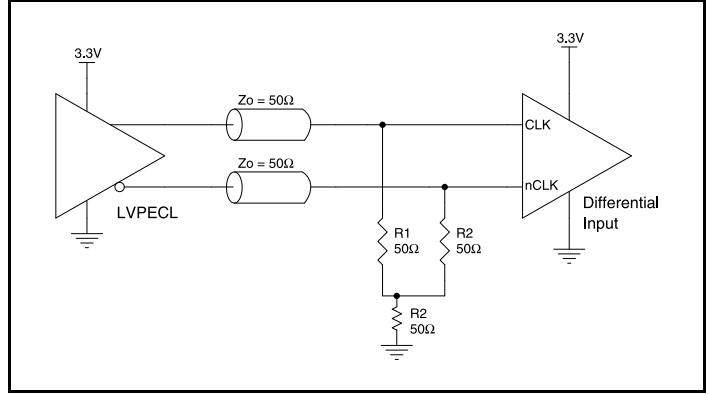


Figure 5B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

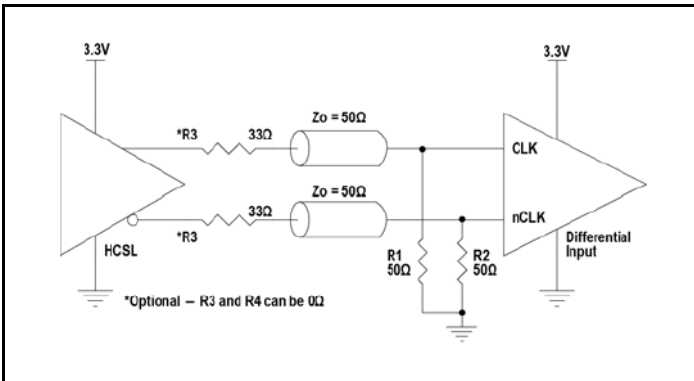


Figure 5C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

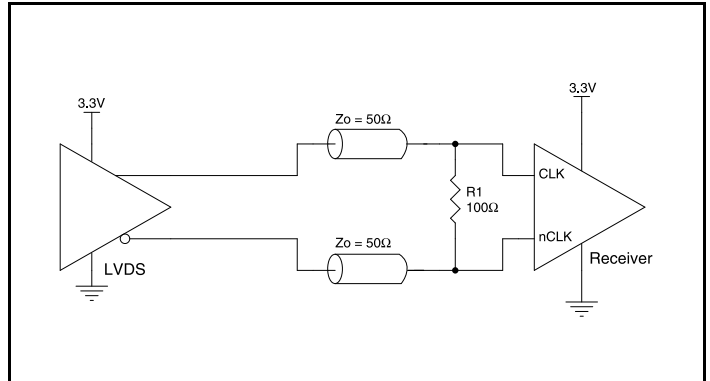
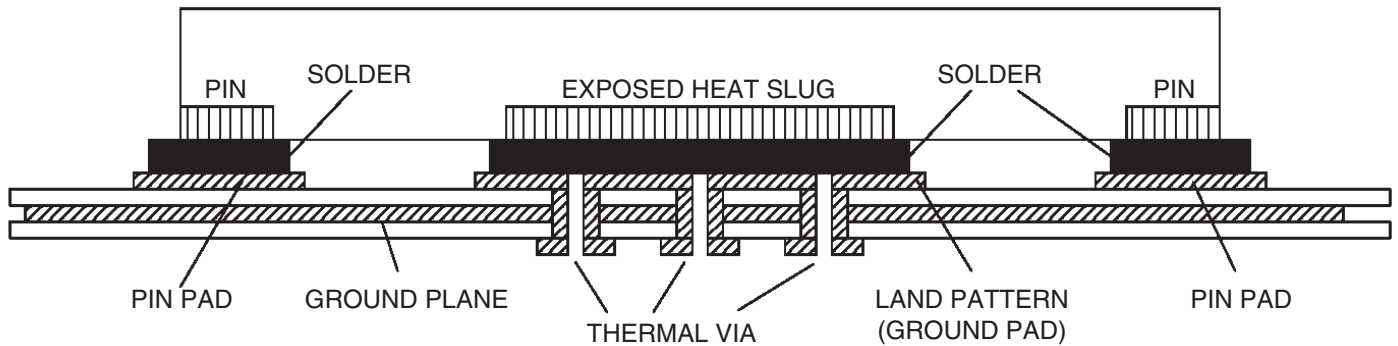


Figure 5D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 6*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead-frame Base Package, Amkor Technology.



**Figure 6. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Power Considerations

This section provides information on power dissipation and junction temperature for the 8L30210. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the 8L30210 is the sum of the core power plus the power dissipation in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

#### Total Static Power:

$$\text{Power (core)}_{MAX} = V_{DD\_MAX} * I_{DD} = 3.465V * 19mA = \mathbf{65.835mW}$$

#### Dynamic Power Dissipation at $F_{OUT}$ (200MHz)

$$\text{Total Power (F}_{OUT\_MAX}) = [(C_{PD} * N) * \text{Frequency} * (V_{DDO})^2] = [(11pF * 10) * 200MHz * (3.465V)^2] = \mathbf{265mW}$$

**N = number of outputs**

#### Total Power

$$\begin{aligned} &= \text{Static Power} + \text{Dynamic Power Dissipation} \\ &= 65.835mW + 265mW \\ &= \mathbf{330.835mW} \end{aligned}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

$$\text{The equation for } T_j \text{ is as follows: } T_j = \theta_{JA} * Pd\_total + T_A$$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 35.23°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.331 * 35.23^\circ\text{C/W} = 96.7^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance for 32-VFQFN, Forced Convection**

Thermal Parameters by Velocity <sup>[a]</sup>			
Meters per Second	0 m/s	1 m/s	2 m/s
$\theta_{JA}$ (Junction to Ambient)	35.23°C/W	31.6°C/W	30.0°C/W
$\theta_{JB}$ (Junction to Board)	1.5°C/W		
$\theta_{JC}$ (Junction to Case)	28.4°C/W		

[a] Multi-Layer PCB, JEDEC Standard Test Boards

## Case Temperature Considerations

This device supports applications in a natural convection environment which does not have any thermal conductivity through ambient air. The printed circuit board (PCB) is typically in a sealed enclosure without any natural or forced air flow and is kept at or below a specific temperature. The device package design incorporates an exposed pad (ePad) with enhanced thermal parameters which is soldered to the PCB where most of the heat escapes from the bottom exposed pad. For this type of application, it is recommended to use the junction-to-board thermal characterization parameter  $\Psi_{JB}$  (Psi-JB) to calculate the junction temperature ( $T_J$ ) and ensure it does not exceed the maximum allowed junction temperature in the Absolute Maximum Rating table.

The junction-to-board thermal characterization parameter,  $\Psi_{JB}$ , is calculated using the following equation:

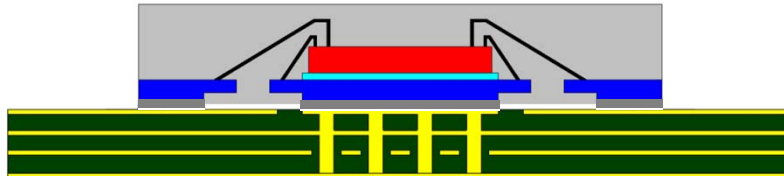
**$T_J = T_{CB} + \Psi_{JB} \times P_d$ , Where**

$T_J$  = Junction temperature at steady state condition in ( $^{\circ}\text{C}$ ).

$T_{CB}$  = Case temperature (Bottom) at steady state condition in ( $^{\circ}\text{C}$ ).

$\Psi_{JB}$  = Thermal characterization parameter to report the difference between junction temperature and the temperature of the board measured at the top surface of the board.

$P_d$  = power dissipation (W) in desired operating configuration.



The ePad provides a low thermal resistance path for heat transfer to the PCB and represents the key pathway to transfer heat away from the IC to the PCB. It's critical that the connection of the exposed pad to the PCB is properly constructed to maintain the desired IC case temperature ( $T_{CB}$ ). A good connection ensures that temperature at the exposed pad ( $T_{CB}$ ) and the board temperature ( $T_B$ ) are relatively the same. An improper connection can lead to increased junction temperature, increased power consumption and decreased electrical performance. In addition, there could be long-term reliability issues and increased failure rate.

Example Calculation for Junction Temperature ( $T_J$ ):  $T_J = T_{CB} + \Psi_{JB} \times P_d$

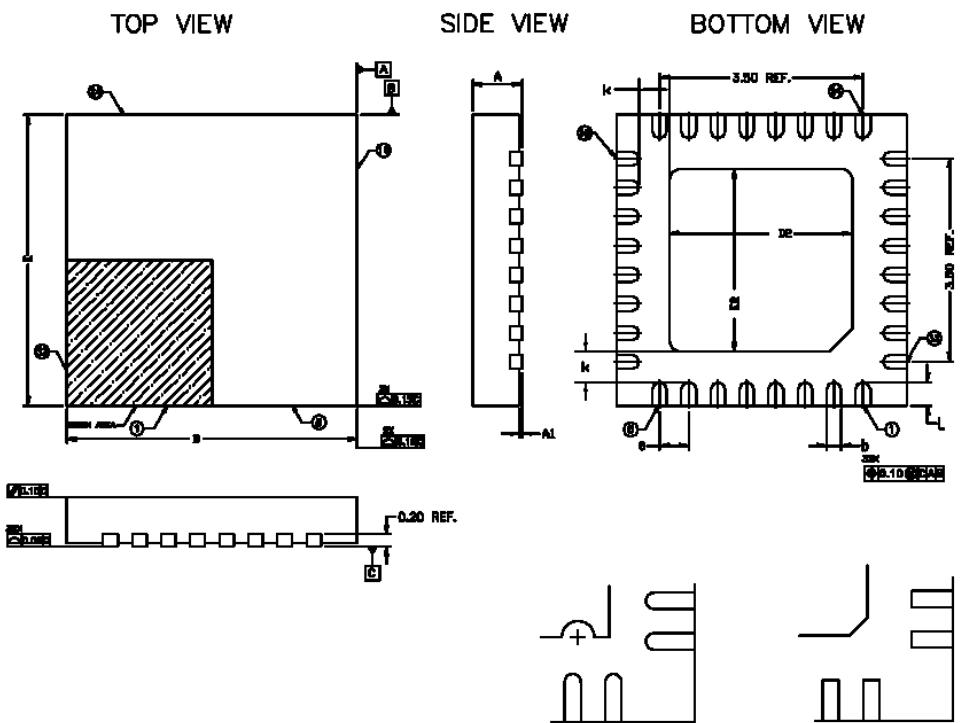
Package type:	32-Lead VFQFN
Body size:	5mm x 5mm x 0.9mm
ePad size:	3.1mm x 3.1mm
Thermal Via:	4 x 4 matrix
$\Psi_{JB}$	0.62 C/W
$T_{CB}$	105 $^{\circ}\text{C}$
$P_d$	0.331 W

For the variables above, the junction temperature is equal to 105.2 $^{\circ}\text{C}$ . Since this is below the maximum junction temperature of 125 $^{\circ}\text{C}$ , there are no long term reliability concerns. In addition, since the junction temperature at which the device was characterized using forced convection is 107.7 $^{\circ}\text{C}$ , this device can function without the degradation of the specified AC or DC parameters.

## Transistor Count

The transistor count for 8L30210 is: 1,638


REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2/1/16	JH
01	ADD "k" VALUE MIN 0.20	2/8/16	JH



SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
D2	3.00	3.15	3.30
E2	3.00	3.15	3.30
L	0.30	0.40	0.50
e	0.50 BSC		
N	32		
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	0.2 REF		
k	0.20	0.53 REF	

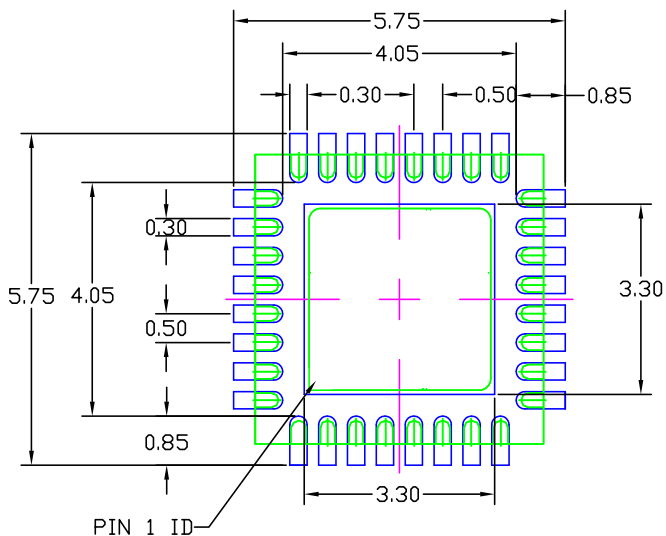
DIMENSIONS ARE IN mm. ANGLES IN DEGREES.  
 VARIATION APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.  
 VARIATION SHALL NOT EXCEED 0.08 mm.  
 TOLERANCE SHALL NOT EXCEED 0.10 mm.

PIN #1 ID OPTION

<b>TOLERANCES UNLESS SPECIFIED</b> DECIMAL ANGULAR X± .1 ±1° XX± .05 XXX± .030		 8024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572 www.IDT.com	TITLE NL/NLG 32 PACKAGE OUTLINE 5.0 x 5.0 mm BODY EPAD 3.15 x 3.15 0.50 mm PITCH QFN	
APPROVALS DRAWN <i>gac</i> CHECKED	DATE 2/1/16		SIZE C	DRAWING No. PSC-4171-01
DO NOT SCALE DRAWING			SHEET 1 OF 2	




REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	2/1/16	JH
01	ADD "k" VALUE MIN 0.20	2/8/16	JH



RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED		 <b>6024 Silver Creek Valley Rd</b> San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572 <a href="http://www.IDT.com">www.IDT.com</a>		
DECIMAL	ANGULAR			
X± .1	±1°			
XX± .05				
XXX± .030				
APPROVALS	DATE	<b>TITLE NL/NLG 32 PACKAGE OUTLINE</b> 5.0 x 5.0 mm BODY EPAD 3.15 x 3.15 0.50 mm PITCH QFN		
DRAWN <i>pac</i>	2/1/16			
CHECKED				
		SIZE	DRAWING No.	REV
		C	PSC-4171-01	01
DO NOT SCALE DRAWING			SHEET 2 OF 2	

## Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8L30210NLGI	IDT8L30210NLGI	32 Lead VFQFN, Lead-Free	Tray	-40°C to 85°C
8L30210NLGI8	IDT8L30210NLGI	32 Lead VFQFN, Lead-Free	Tape & Reel	-40°C to 85°C

## Revision History

Revision Date	Description of Change
July 27, 2017	Updated Table 7 with $\theta_{JB}$ and $\theta_{JC}$ values.
May 3, 2017	<ul style="list-style-type: none"> <li>▪ Table 4C - added <math>V_{IH}</math> max specs.</li> <li>▪ Updated <a href="#">Package Drawings</a> from ICS to IDT.</li> <li>▪ Updated datasheet header/footer.</li> </ul>
November 24, 2015	<a href="#">Features</a> section - updated case temperature bullet.

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