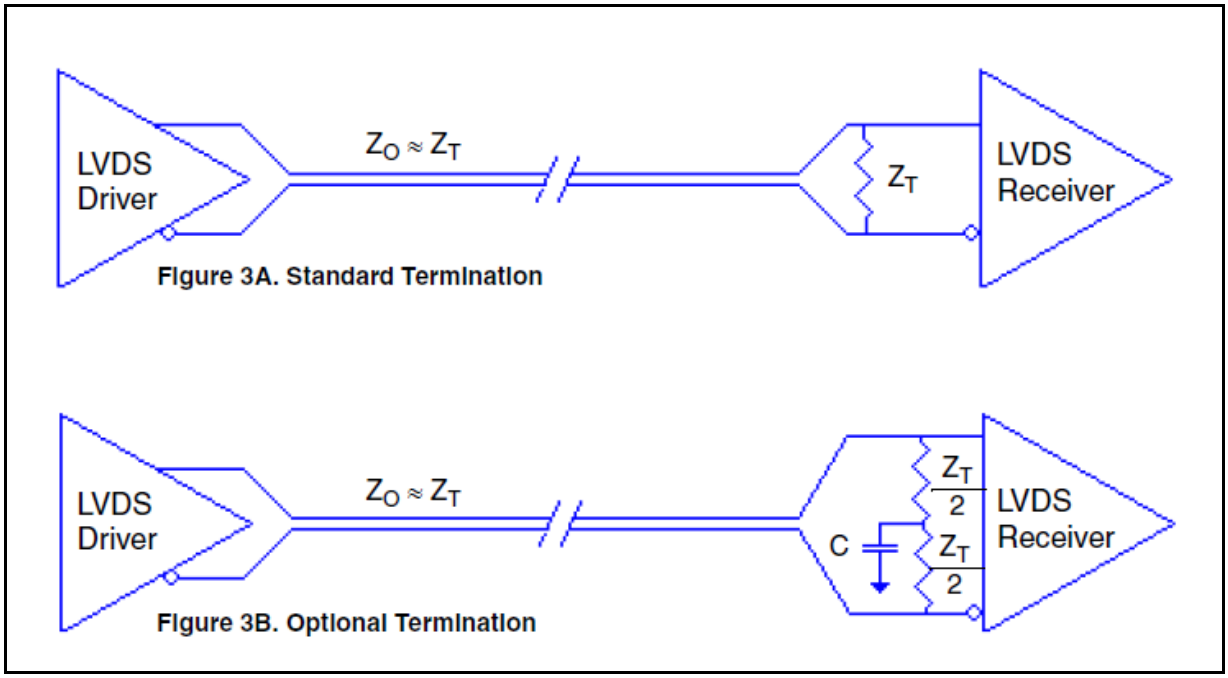
LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 3A* can be used with either type of output structure. *Figure 3B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



LVDS Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

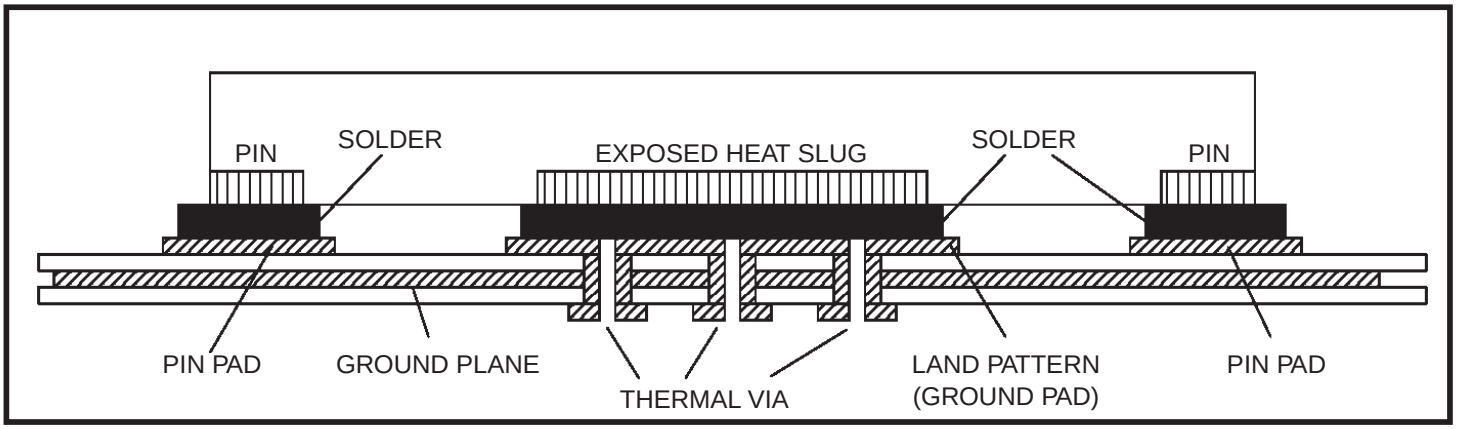


Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8P34S1106I. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8P34S1106I is the sum of the core power plus the output power dissipation due to the load. The following is the power dissipation for V_{DD} = 1.8V + 5% = 1.89V, which gives worst case results.

The maximum current at 85°C is as follows:

I_{DD_MAX} = 107mA

- Power $_{(core)MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 1.89V * 107mA = **202.23mW**

Total Power$_{_MAX}$ = 202.23mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + TA

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 62.2°C/W per Table 5 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.203W * 62.2°C/W = 97.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5. Thermal Resistance θ_{JA} for 20 Lead VFQFN

θ_{JA} **at 0 Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	62.2°C/W	54.4°C/W	48.8°C/W

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 20-lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	62.2°C/W	54.4°C/W	48.8°C/W

Transistor Count

The transistor count for the 8P34S1106I is: 976

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/20-vfqfpn-package-outline-drawing-40-x-40-x-090-mm-body-05mm-pitch-epad-21-x-21-mm-nlg20p1

Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8P34S1106NLGI	8P34S1106NLGI	“Lead-Free” 20-lead VFQFN	Tube	-40°C to 85°C
8P34S1106NLGI8	8P34S1106NLGI	“Lead-Free” 20-lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History

Revision Date	Description of Change
October 18, 2019	• Corrected the “shipping packaging” information for 8P34S1106NLGI in Ordering Information • Completed other minor changes
November 29, 2018	Updated the description of Absolute Maximum Ratings Added Recommended Operating Conditions Updated the Package Outline Drawings; however, no technical changes
December 17, 2015	Initial release.