

## Description

The IDT8S89873I is a high speed Differential-to-LVDS Buffer/Divider with Internal Termination. The IDT8S89873I has a selectable  $\div 2$ ,  $\div 4$ ,  $\div 8$ ,  $\div 16$  output dividers. The clock input has internal termination resistors, allowing it to interface with several differential signal types while minimizing the number of required external components.

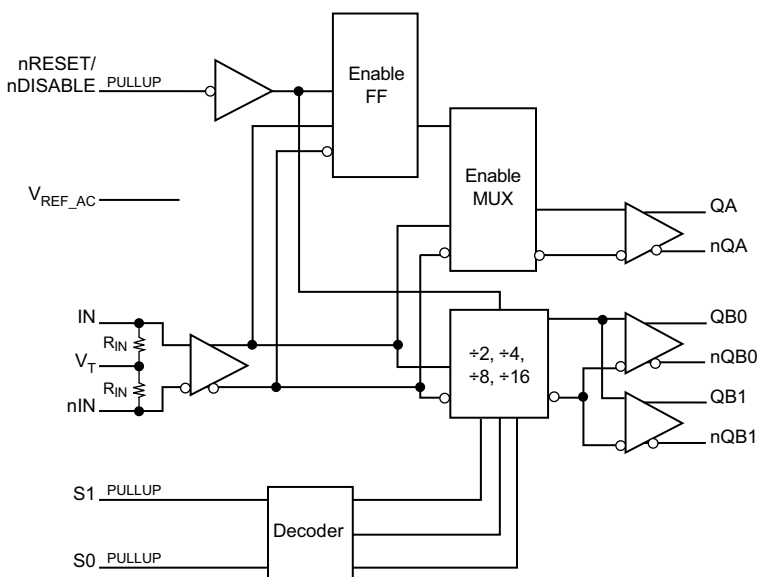
The nRESET/nDISABLE asynchronously resets the QB output bank. QA outputs are synchronously enabled or disabled on the next falling edge of IN, or rising edge of nIN. Please refer to the timing diagram for details.

The device is packaged in a small, 3 x 3 mm VFQFN package, making it ideal for use on space-constrained boards.

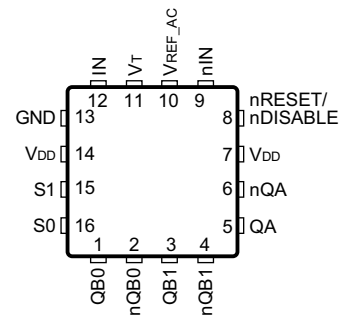
## Features

- Three LVDS outputs
- Frequency divide select options:  $\div 2$ ,  $\div 4$ ,  $\div 8$ ,  $\div 16$
- IN, nIN input can accept the following differential input levels: LVPECL, LVDS, CML
- Output frequency: 2GHz (maximum) in pass-through mode
- Additive phase jitter: 0.185ps (typical) RMS
- Output skew: 9ps (typical), QBx, nQBx outputs
- Propagation Delay: 540ps (typical)
- Full 3.3V supply mode
- $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  ambient operating temperature
- Available in lead-free (RoHS 6) package

## Block Diagram



## Pin Assignment



**IDT8S89873I**  
**16-Lead VFQFN**  
**3mm x 3mm x 0.925mm package body**  
**NL Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	QB0, nQB0	Output		Differential output pair. LVDS interface levels.
3, 4	QB1, nQB1	Output		Differential output pair. LVDS interface levels.
5, 6	QA, nQA	Output		Differential output pair. LVDS interface levels.
7, 14	V <sub>DD</sub>	Power		Power supply pins.
8	nRESET/ nDISABLE	Input	Pullup	Output reset and enable/disable pin. When LOW, resets the divider select, and align Bank A and Bank B edges. In addition, when LOW, Bank A and Bank B will be disabled. Input threshold is V <sub>DD</sub> /2V. Includes an internal 37kΩ pull-up resistor. LVTTTL/LVCMOS interface levels.
9	nIN	Input		Inverting differential LVPECL clock input. R <sub>IN</sub> = 50Ω termination to V <sub>T</sub> .
10	V <sub>REF_AC</sub>	Output		Reference voltage for AC-coupled applications. Equal to V <sub>DD</sub> – 1.4V (approx.).
11	V <sub>T</sub>	Input		Termination input.
12	IN	Input		Non-inverting LVPECL differential clock input. R <sub>IN</sub> = 50Ω termination to V <sub>T</sub> .
13	GND	Power		Power supply ground.
15, 16	S1, S0	Input	Pullup	Select pins. Logic HIGH if left unconnected (≠16 mode). S0 = LSB. Input threshold is V <sub>DD</sub> /2. 37kΩ internal pull-up resistor. LVCMOS/LVTTTL interface levels.

NOTE: *Pull-up* refers to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R <sub>PULLUP</sub>	Input Pullup Resistor			37		kΩ
C <sub>IN</sub>	Input Capacitance			2		pF

## Function Tables

Table 3. Truth Table

Inputs			Outputs	
nRESET/nDISABLE	S1	S0	Bank A	Bank B
1 (default)	0	0	Input Clock	Input Clock ÷2
1	0	1	Input Clock	Input Clock ÷4
1	1	0	Input Clock	Input Clock ÷8
1	1 (default)	1 (default)	Input Clock	Input Clock ÷16
0	X	X	QA = LOW, nQA = HIGH; NOTE 1	QBx = LOW, nQBx = HIGH; NOTE 2

NOTE 1: On the next negative transition of the input signal.

NOTE 2: Asynchronous reset/disable function.

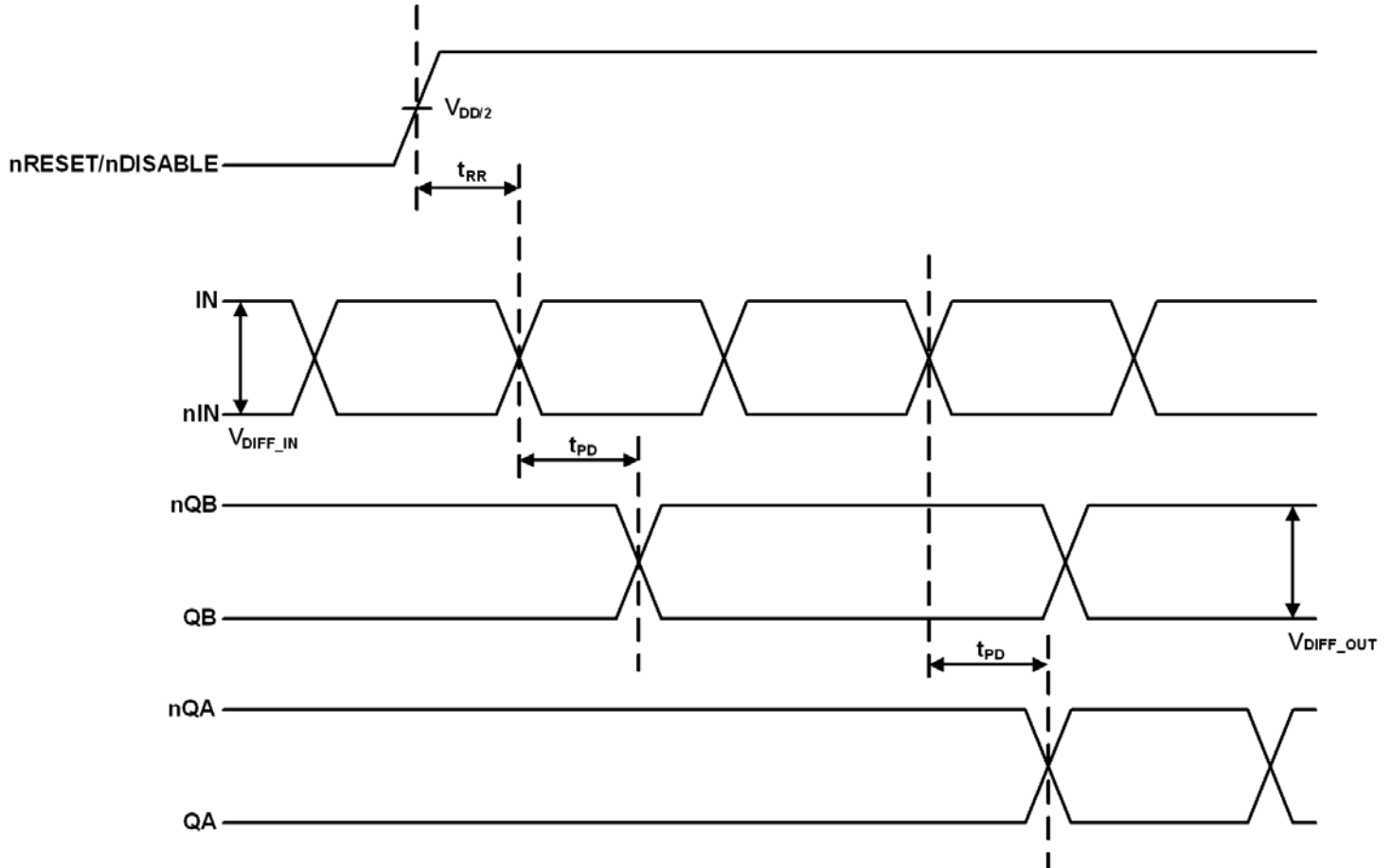


Figure 1. nRESET/nDISABLE Timing Diagram

## Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $I_O$ Continuous Current Surge Current	10mA 15mA
Input Current, $I_N$ , $nIN$	$\pm 50mA$
$V_T$ Current, $I_{VT}$	$\pm 100mA$
$V_{REF\_AC}$ Input Sink/Source, $I_{REF\_AC}$	$\pm 2mA$
Operating Temperature Range, $T_A$	-40°C to +85°C
Package Thermal Impedance, $\theta_{JA}$ , (Junction-to-Ambient)	74.7°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Power Supply Voltage		3.0	3.3	3.6	V
$I_{DD}$	Power Supply Current				100	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2.2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		0		0.8	V
$I_{IH}$	Input High Current	S[1:0], nRESET/nDISABLE $V_{DD} = V_{IN} = 3.6V$			10	$\mu A$
$I_{IL}$	Input Low Current	S[1:0], nRESET/nDISABLE $V_{DD} = 3.6V, V_{IN} = 0V$	-150			$\mu A$

**Table 4C. Differential DC Characteristics,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{IN}$	Input Resistance	IN, nIN		50		$\Omega$
$V_{IH}$	Input High Voltage	IN, nIN	0.15		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	IN, nIN	0		$V_{DD} - 0.15$	V
$V_{IN}$	Input Voltage Swing; NOTE 1		0.15		1.2	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing		0.3		2.4	V
$V_{REF\_AC}$	Bias Voltage		$V_{DD} - 1.4$	$V_{DD} - 1.425$	$V_{DD} - 1.34$	V

NOTE 1: Refer to Parameter Measurement Information, *Input Voltage Swing* diagram.

NOTE 2: Guaranteed by design.

**Table 4D. LVDS DC Characteristics,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OUT}$	Output Voltage Swing		370	470	570	mV
$V_{OH}$	Output High Voltage		1.366	1.500	1.690	V
$V_{OL}$	Output Low Voltage		0.860	1.040	1.226	V
$V_{OCM}$	Output Common Mode Voltage		1.125	1.27	1.400	V
$\Delta V_{OCM}$	Change in Common Mode Voltage				50	mV

## AC Electrical Characteristics

**Table 5. AC Characteristics,  $V_{DD} = 3.3V \pm 10\%$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$f_{OUT}$	Output Frequency; NOTE 5	Output Swing $\geq 200mV$			2	GHz	
$t_{PD}$	Propagation Delay; NOTE 1	IN-to-Q	Input Swing: $<400mV$	430	525	640	ps
			Input Swing: $\geq 400mV$	420	510	620	ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3	QB0-to-QB1		9	40	ps	
		QA-to-QBx		12	30	ps	
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps	
$f_{jit}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter section; NOTE 5	156.25MHz, Integration Range: 12kHz - 20MHz		0.185	0.220	ps	
$t_{RR}$	Reset Recovery Time		600			ps	
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	45	125	285	ps	

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: All parameters characterized at  $\leq 2GHz$  unless otherwise noted.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

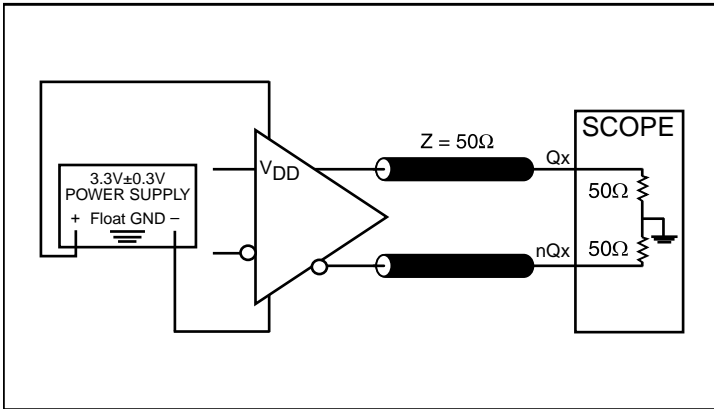
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.

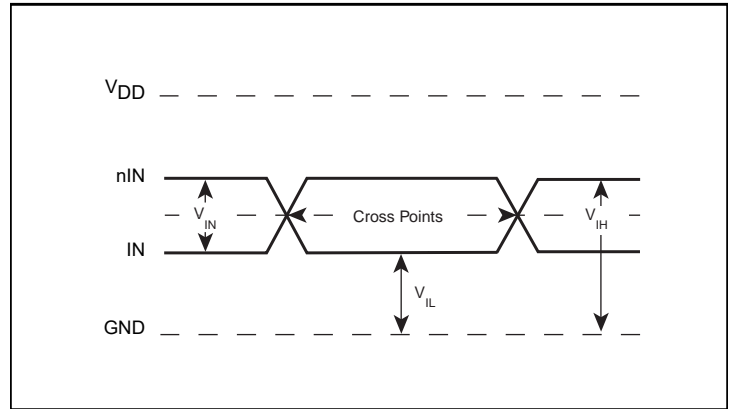
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: Device is in pass-through mode.

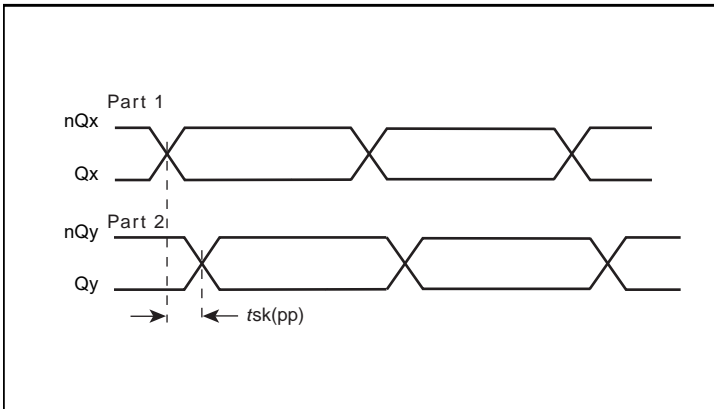
## Parameter Measurement Information



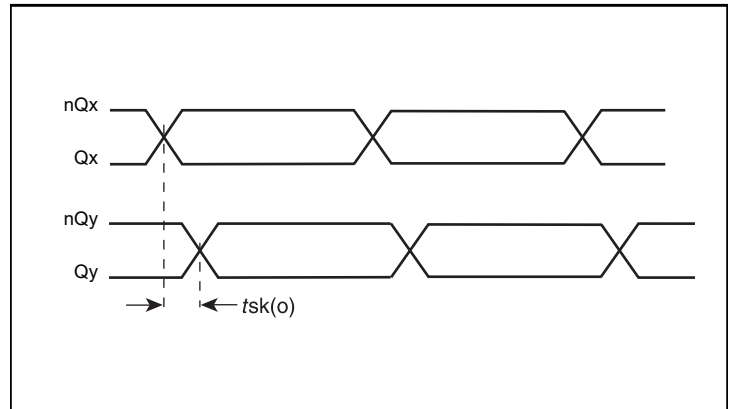
Output Load AC Test Circuit



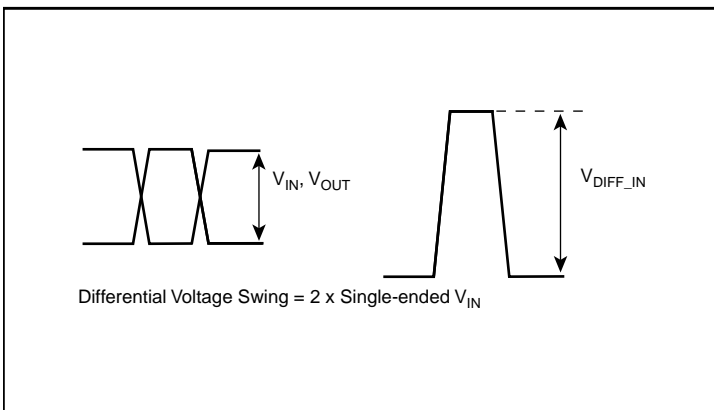
Differential Input Level



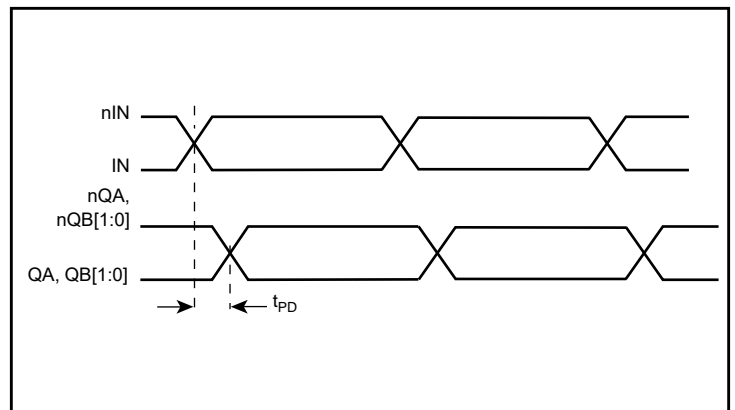
Part-to-Part Skew



Output Skew

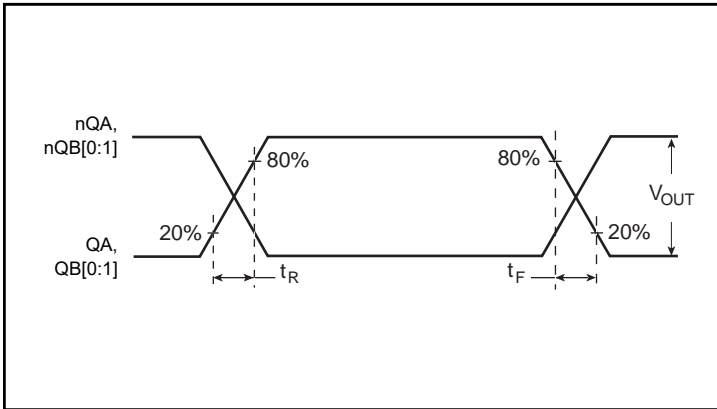


Single-Ended & Differential Voltage Swing

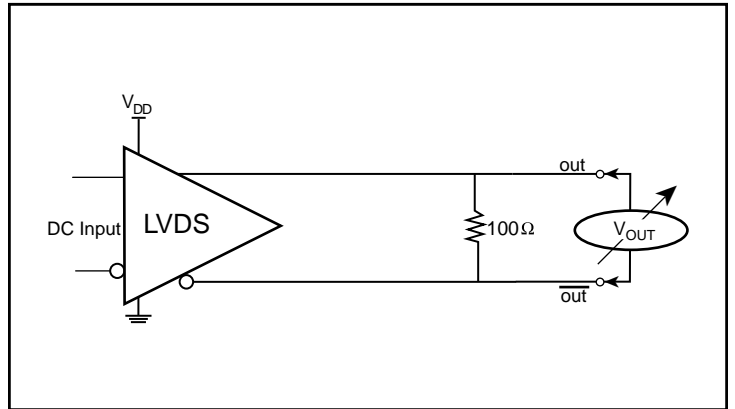


Propagation Delay

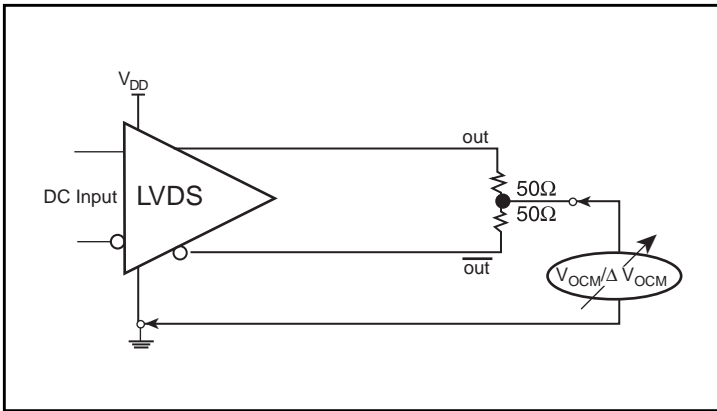
Parameter Measurement Information, continued



Output Rise/Fall Time



Differential Output Voltage Setup



Offset Voltage Setup

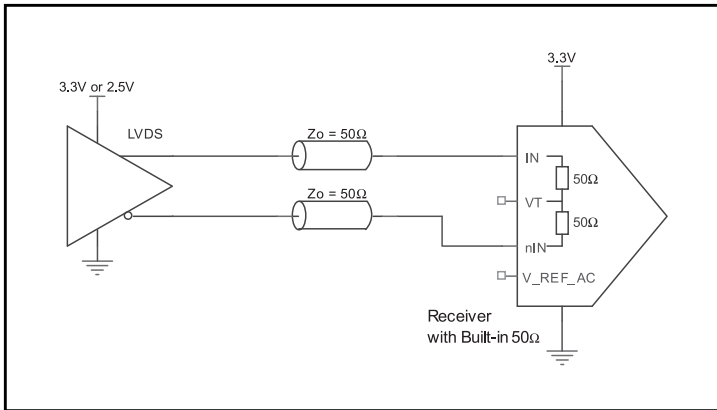


## Applications Information

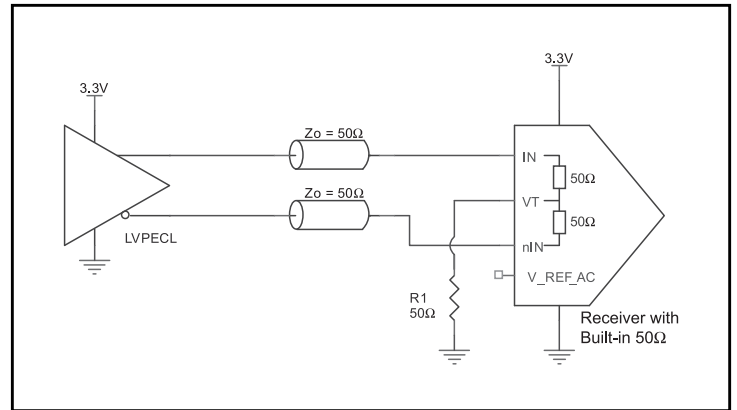
### 3.3V LVPECL Input with Built-In 50Ω Termination Interface

The IN/nIN with built-in 50Ω terminations accept LVDS, LVPECL, CML and other differential signals. Both signals must meet the  $V_{IN}$  and  $V_{IH}$  input requirements. Figures 2A to 2D show interface examples for the IN/nIN input with built-in 50Ω terminations driven by

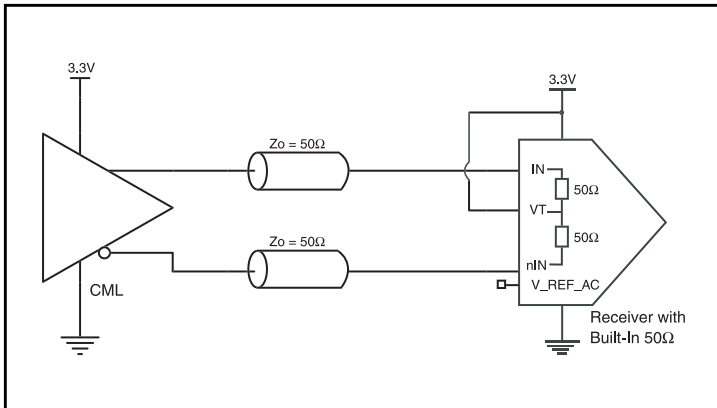
the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.



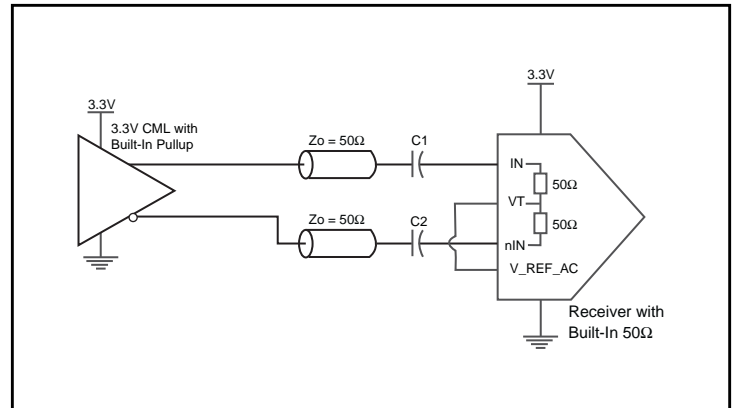
**Figure 2A. IN/nIN Input with Built-In 50Ω Driven by an LVDS Driver**



**Figure 2B. IN/nIN Input with Built-In 50Ω Driven by an LVPECL Driver**



**Figure 2C. IN/nIN Input with Built-In 50Ω Driven by a CML Driver**



**Figure 2D. IN/nIN Input with Built-In 50Ω Driven by a CML Driver with Built-In 50Ω Pullup**

## Recommendations for Unused Input and Output Pins

### Inputs:

#### LVCMOS Control Pins

All control pins have internal pullups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

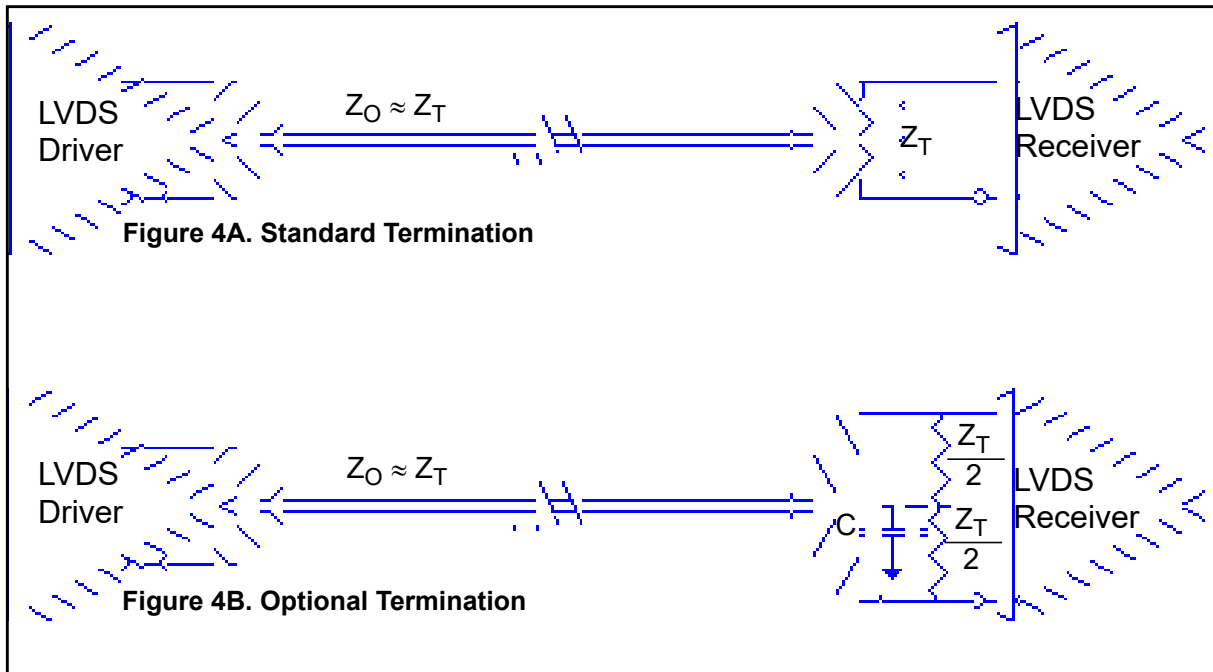
#### LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

## LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance ( $Z_T$ ) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ( $Z_0$ ) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The

standard termination schematic as shown in *Figure 4A* can be used with either type of output structure. *Figure 4B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



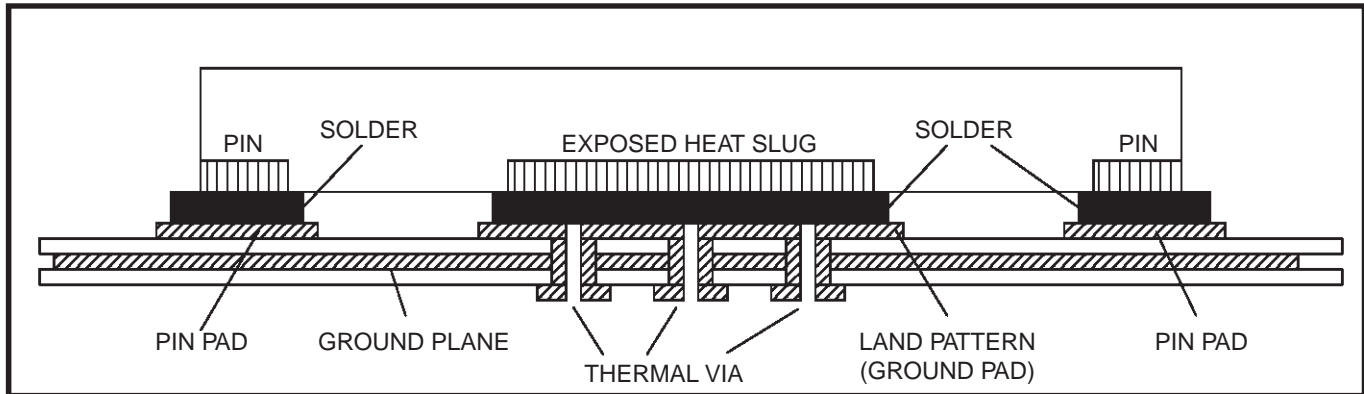
### LVDS Termination

## VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**

## Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8S89873I. Equations and example calculations are also provided.

The maximum current at 85°C is as follows

$$I_{DD\_MAX} = 96.32\text{mA}$$

### 1. Power Dissipation.

The total power dissipation for the IDT8S89873I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3\text{V} + 0.3\text{V} = 3.6\text{V}$ , which gives worst case results.

- $\text{Power}_{MAX} = V_{DD\_MAX} * I_{DD\_MAX} = 3.6\text{V} * 100\text{mA} = \mathbf{360\text{mW}}$
- Power Dissipation for internal termination  $R_T$   
 $\text{Power } (R_T)_{MAX} = (V_{IN\_MAX})^2 / R_{T\_MIN} = (1.2\text{V})^2 / 80\Omega = \mathbf{18\text{mW}}$

$$\text{Total Power}_{MAX} = 360\text{mW} + 18\text{mW} = \mathbf{378\text{mW}}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 74.7°C/W per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.378\text{W} * 74.7^\circ\text{C/W} = 113.2^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 16 Lead VFQFN, Forced Convection**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

## Reliability Information

**Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 16 Lead VFQFN**

$\theta_{JA}$ by Velocity			
Meters per Second	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	74.7°C/W	65.3°C/W	58.5°C/W

## Transistor Count

The transistor count for IDT8S89873I is: 415  
Pin compatible with ICS889873

## Package Outline Drawings

The package outline drawings are located at the end of this document. The package information is the most current data available and is subject to change without notice or revision of this document.

## Ordering Information

**Table 8. Ordering Information**

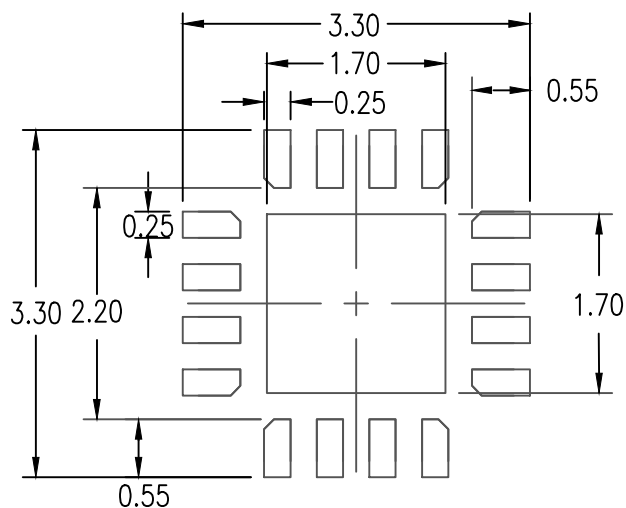
Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8S89873ANLGI	873AI	"Lead-Free" 16 Lead VFQFN	Tray	-40°C to 85°C
8S89873ANLG18	873AI	"Lead-Free" 16 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "G" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History

Revision Date	Description of Change
November 29, 2017	Updated the package outline drawings; however, no technical changes Completed other minor changes
July 10, 2012	Initial release.





RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. TOP DOWN VIEW-AS VIEWED ON PCB
3. LAND PATTERN RECOMMENDATION IS PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

Package Revision History		
Date Created	Rev No.	Description
Oct 25, 2017	Rev 04	Remove Bookmak at Pdf Format & Update Thickness Tolerance
Aug 15, 2017	Rev 03	Update Epad Range

## Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
  2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
  3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
  4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
  5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
    - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
    - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
  6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
  7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
  8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
  9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
  10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
  11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
  12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
- (Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
- (Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

## Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

## Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

## Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.