Low Skew, 1-to-4 Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer

IDT8T33FS314I

DATA SHEET

General Description

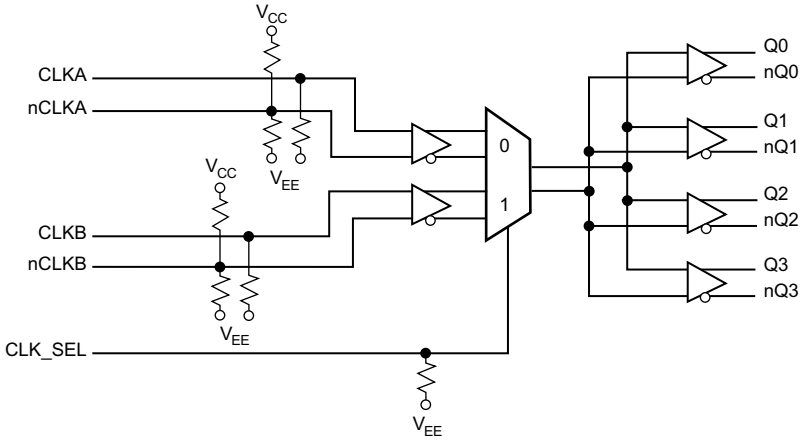
The IDT8T33FS314I is a low skew 1-to-4 Differential Fanout Buffer, designed with clock distribution in mind, accepting two clock sources into an input MUX. The MUX is controlled by a CLK_SEL pin. This makes the IDT8T33FS314I very versatile, in that, it can operate as both a differential clock buffer as well as a signal-level translator and fanout buffer.

The device is designed on a SiGe process and can operate at frequencies in excess of 2.7GHz. This ensures negligible jitter introduction to the timing budget which makes it an ideal choice for distributing high frequency, high precision clocks across back planes and boards in communication systems. Internal temperature compensation guarantees consistent performance across various platforms.

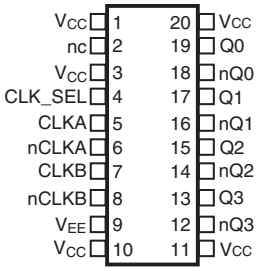
Features

- Four differential ECL/LVPECL level outputs
- One differential ECL/LVPECL or single-ended input (CLKA)
  One differential HSTL or single-ended input (CLKB)
- Maximum output frequency: 2.7GHz
- Additive phase jitter, RMS: 0.114ps (typical) @ 156.25MHz
- Output skew: 50ps (maximum)
- LVPECL and HSTL mode operating voltage supply range:
  V_{CC} = 2.5V±5% or 3.3V±5%, V_{EE} = 0V
- ECL mode operating voltage supply range:
  V_{EE} = -3.3V±5% or -2.5V±5%, V_{CC} = 0V
- -40°C to 85°C ambient operating temperature
- Lead-free (RoHS 6) packaging

Block Diagram



Pin Assignment



IDT8T33FS314I

20-Lead 209-MIL SSOP
5.3mm x 7.2mm x 1.75mm body package
PY Package
Top View

20-Lead TSSOP
4.4mm x 6.5mm x 0.925mm body package
PG Package
Top View

Pin Descriptions and Characteristics

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 3, 10 11, 20	V_{CC}	Power		Positive supply pins.
2	nc	Unused		No connect.
4	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLKB, nCLKB inputs. When LOW, selects CLKA, nCLKA inputs.
5	CLKA	Input	Pulldown	Default non-inverting differential clock input. LVPECL/ECL interface levels.
6	nCLKA	Input	Pullup/ Pulldown	Default inverting differential clock input. LVPECL/ECL interface levels.
7	CLKB	Input	Pulldown	Alternative non-inverting differential clock input. HSTL interface levels.
8	nCLKB	Input	Pullup/ Pulldown	Alternative inverting differential clock input. HSTL interface levels.
9	V_{EE}	Power		Negative supply pin.
12, 13	nQ3,Q3	Output		Differential output pair. LVPECL/ECL interface levels.
14, 15	nQ2,Q2	Output		Differential output pair. LVPECL/ECL interface levels.
16, 17	nQ1,Q1	Output		Differential output pair. LVPECL/ECL interface levels.
18, 19	nQ0,Q0	Output		Differential output pair. LVPECL/ECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLK_SEL		2		pF
R_{PULLUP}	Input Pullup Resistor			75		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	3.9V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-3.9V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.3V to V_{CC} + 0.3V
Inputs, V_I (ECL mode)	0.3V to V_{EE} – 0.3V
Outputs, I_O Continuous Current	50mA
Package Thermal Impedance, θ_{JA} 20-Lead SSOP 20-Lead TSSOP	 100.4°C/W (0 mps) 115.0°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. LVPECL DC Characteristics, V_{CC} = 2.5V ±5% or 3.3V ±5%, V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Control Input CLK_SEL						
V_{IL}	Input Low Voltage		V_{CC} - 1.810		V_{CC} - 1.475	V
V_{IH}	Input High Voltage		V_{CC} - 1.165		V_{CC} - 0.880	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
Clock Input Pair CLKA, nCLKA (LVPECL Differential Signals)						
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.1		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 2		1.0		V_{CC} - 0.3	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
Clock Input Pair CLKB, nCLKB (HSTL Differential Signals)						
V_{DIF}	Differential Input Voltage; NOTE 3	V_{CC} = 3.3V	0.4			V
		V_{CC} = 2.5V	0.4			V
V_X	Differential Crosspoint Voltage; NOTE 4		0	0.68 - 0.9	V_{CC} - 1.0	V
I_{IN}	Input Current	$V_{IN} = V_x$ ±0.2V			200	µA
LVPECL Clock Outputs (Q[0:3], nQ[0:3])						
V_{OH}	Output High Voltage		V_{CC} - 1.2	V_{CC} - 0.808	V_{CC} - 0.7	V
V_{OL}	Output Low Voltage	V_{CC} = 3.3V ±5%	V_{CC} - 1.9	V_{CC} - 1.689	V_{CC} - 1.5	V
		V_{CC} = 2.5V ±5%	V_{CC} - 1.9	V_{CC} - 1.662	V_{CC} - 1.3	V
Supply Current						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current			49	60	mA

NOTE 1: V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
NOTE 2: V_{CMR} is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specification.
NOTE 3: V_{DIF} is the minimum differential HSTL input voltage swing required for device functionality.
NOTE 4: V_X is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X range and the input swing lies within the V_{PP} specification.

Table 3B. ECL DC Characteristics, V_{CC} = 0V, V_{EE} = -3.3V±5% or -2.5V±5%, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Control Input CLK_SEL						
V_{IL}	Input Low Voltage		-1.810		-1.475	V
V_{IH}	Input High Voltage		-1.165		-0.880	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
Clock Input Pair CLKA, nCLKA (LVPECL Differential Signals)						
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.1		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 2		V_{EE} + 1.0		-0.3	V
I_{IN}	Input Current	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$			100	µA
LVPECL Clock Outputs (Q[0:3], nQ[0:3])						
V_{OH}	Output High Voltage		-1.2	-0.808	-0.7	V
V_{OL}	Output Low Voltage	V_{EE} = -3.3V ±5%	-1.9	-1.689	-1.5	V
		V_{EE} = -2.5V ±5%	-1.9	-1.662	-1.3	V
Supply Current						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current			49	60	mA

NOTE 1: V_{PP} is the minimum differential input voltage swing required to maintain device functionality.
NOTE 2: V_{CMR} is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specification.

AC Electrical Characteristics

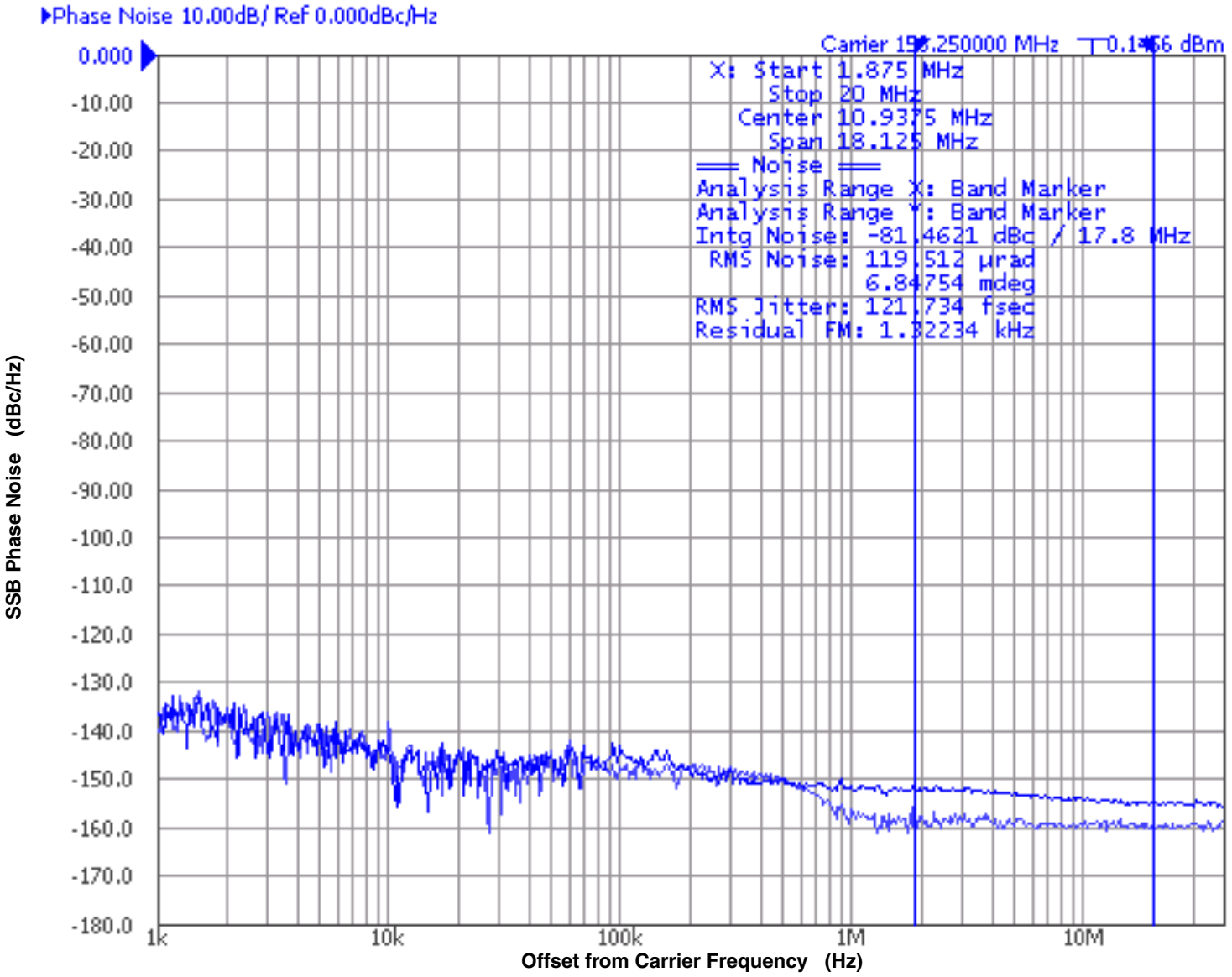
Table 4. AC Characteristics, (LVPECL/HSTL), V_{CC} = 3.3V ±5% or 2.5V ±5%, V_{EE} = 0V, or (ECL) V_{EE} = -3.3V ±5% or -2.5V ±5%, V_{CC} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{PP}	Differential Input Voltage; NOTE 1		0.15		1.3	V
V_{CMR}	Differential Input Crosspoint Voltage; NOTE 2		V_{EE} + 1.0		V_{CC} - 0.3	V
f_{CLK}	Input Frequency; NOTE 3				2.7	GHz
t_{PD}	Propagation Delay, CLKA or CLKB to Output Pair; NOTE 4		230		650	ps
V_{DIF}	HSTL Differential Input Voltage; NOTE 5		0.4		1.0	V
V_X	HSTL Input Differential Crosspoint Voltage; NOTE 6		V_{EE} + 0.01		V_{CC} - 1.0	V
V_O(pp)	Differential Output Voltage (peak-to-peak)	f_{OUT} < 300MHz	0.45	0.88	0.95	V
		f_{OUT} < 1.5GHz	0.3	0.74	0.95	V
tsk(o)	Output Skew				50	ps
tjit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	156.25MHz, @ 3.3V, 1.875MHz – 20MHz		0.114		ps
		312.5MHz @ 3.3V, 1.875MHz – 20MHz		0.052		ps
tsk(p)	Output Pulse Skew; NOTE 7	660MHz			75	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	0.05		0.3	ns

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: V_{PP} is the minimum differential ECL/LVPECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
NOTE 2: V_{CMR} is the crosspoint of the differential ECL/LVPECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} specification. Violation of V_{CMR} or V_{PP} impacts the device propagation delay, device and part-to-part skew.
NOTE 3: The IDT8T33FS314 is fully operational up to 2.7GHz and is characterized up to 1.5GHz.
NOTE 4: Propagation delay specified for output rise and fall times less than 5ns.
NOTE 5: V_{DIF} is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
NOTE 6: V_X is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X range and the input swing lies within the V_{DIF} specification. Violation of V_X or V_{DIF} impacts the device propagation delay, device and part-to-part skew.
NOTE 7: Output pulse skew is the absolute value of the difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

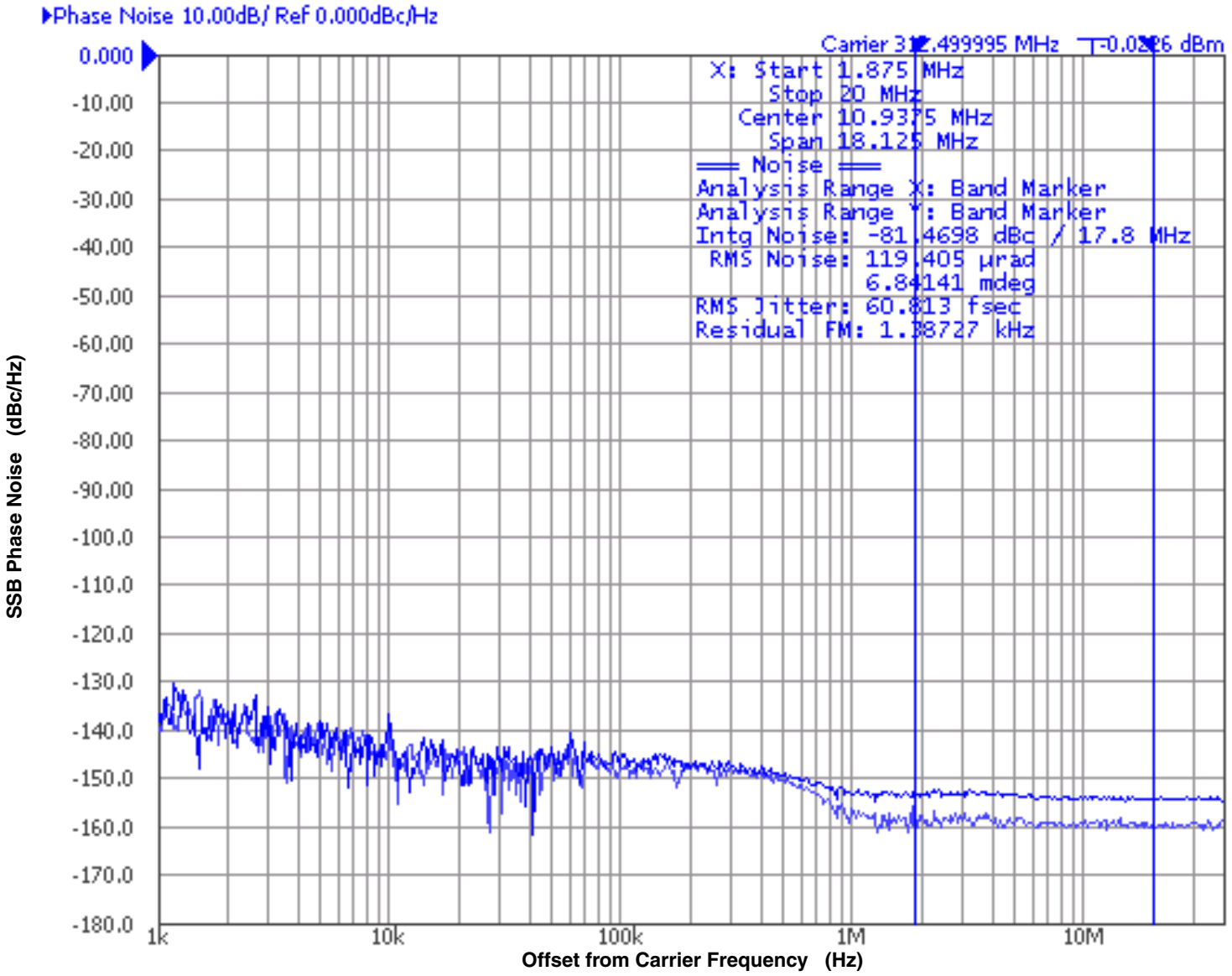
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



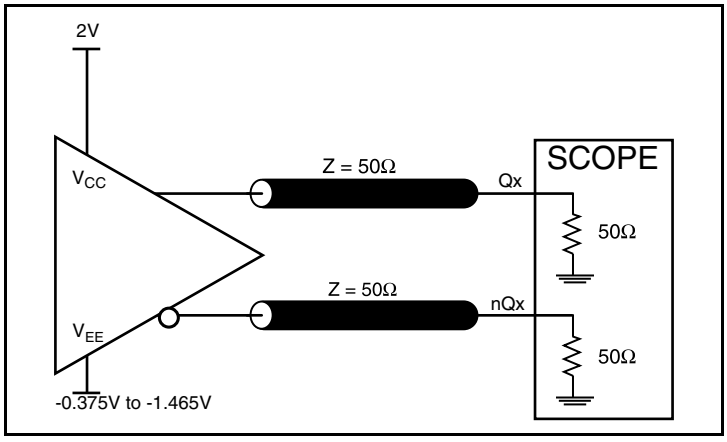
As with most timing specifications, phase noise measurements have issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

A Rohde & Schartz SMA100 was used as input source.

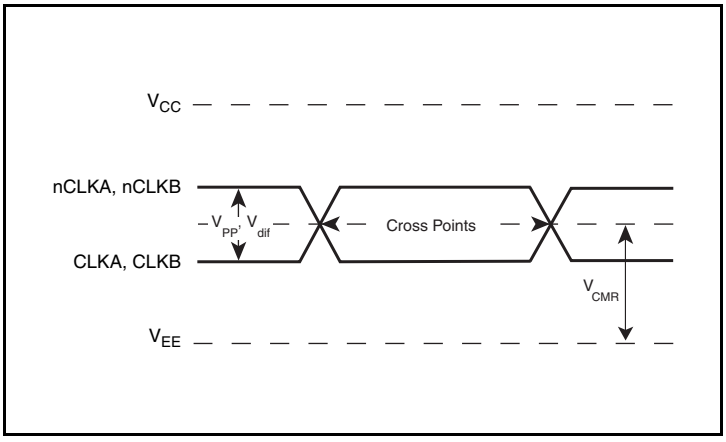


A Rohde & Schartz SMA100 was used as input source.

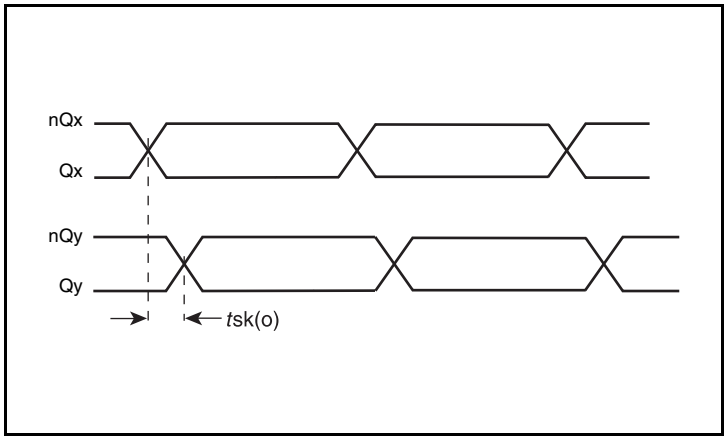
Parameter Measurement Information



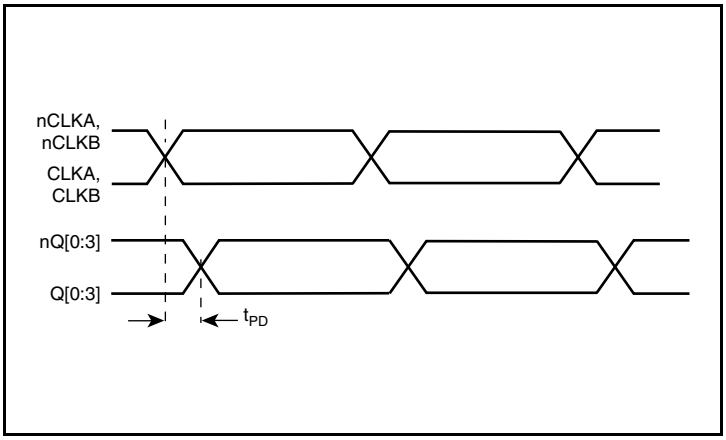
3.3V, 2.5V LVPECL Output Load Test Circuit



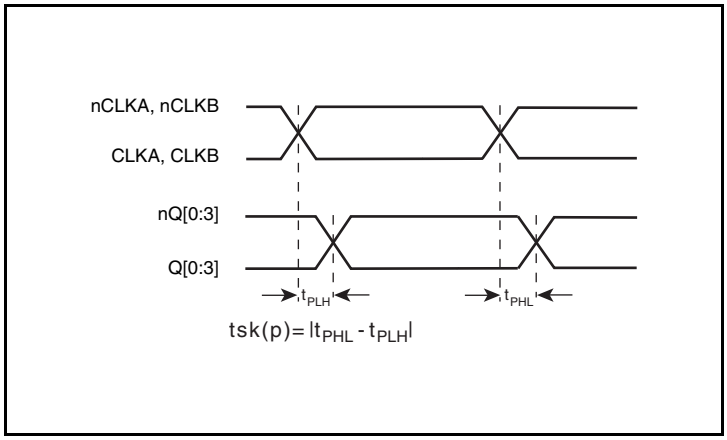
Differential Input Level



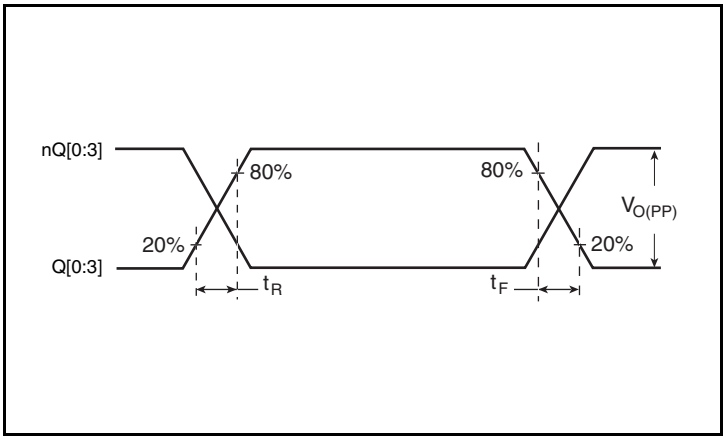
Output Skew



Propagation Delay



Output Pulse Skew



Output Rise/Fall Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

CLK/nCLK Inputs

For applications not requiring the use of a differential input, both the CLK and nCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 1.25V. Similarly, if the input clock swing is 1.8V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_1 at 0.9V. It is recommended to always use R1 and R2 to provide a known V_1 voltage. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways.

First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

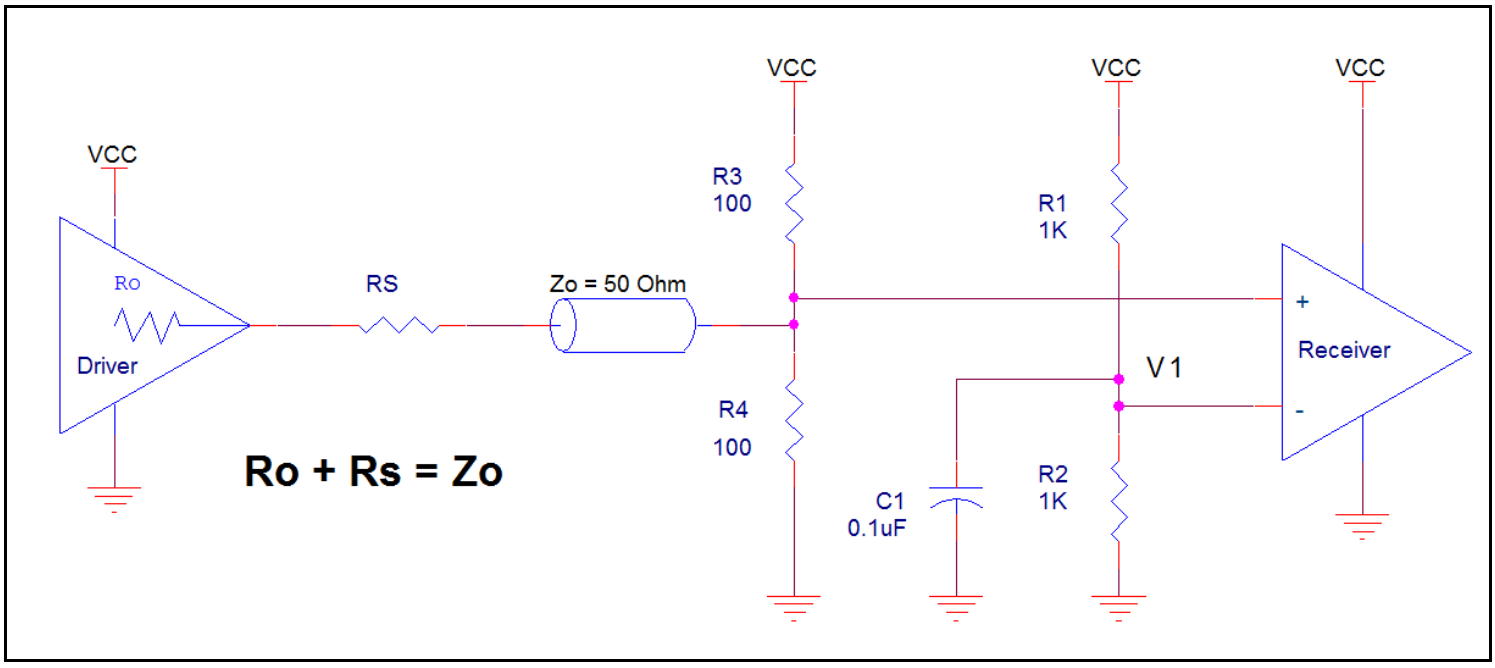


Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both $V_{O(PP)}$ and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 2A to Figure 2E* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 2A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

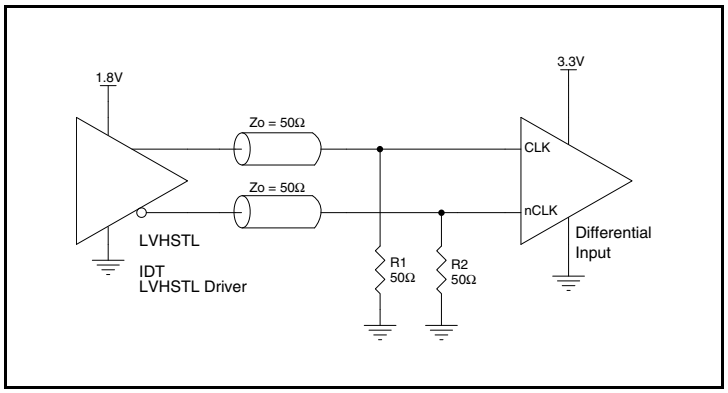


Figure 2A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

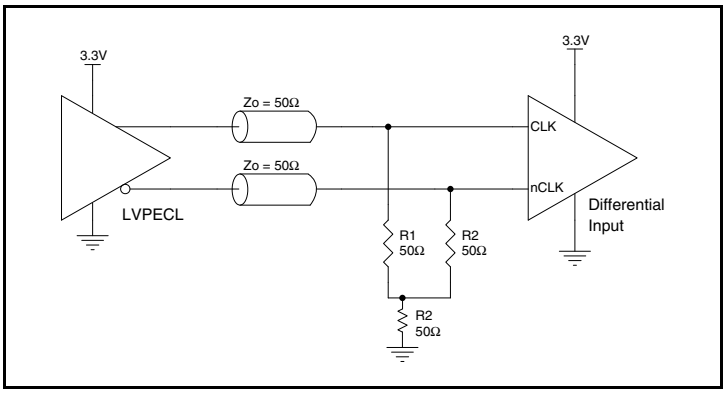


Figure 2B. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver

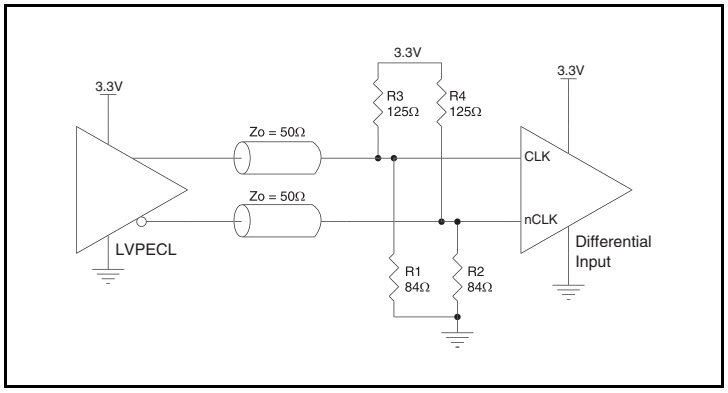


Figure 2C. CLKx/nCLKx Input Driven by a 3.3V LVPECL Driver

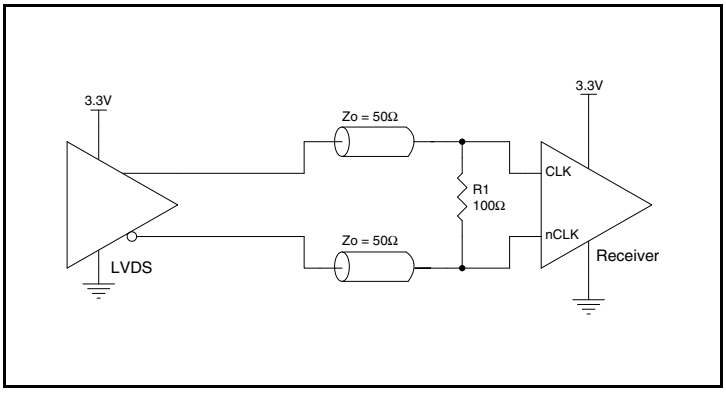


Figure 2D. CLKx/nCLKx Input Driven by a 3.3V LVDS Driver

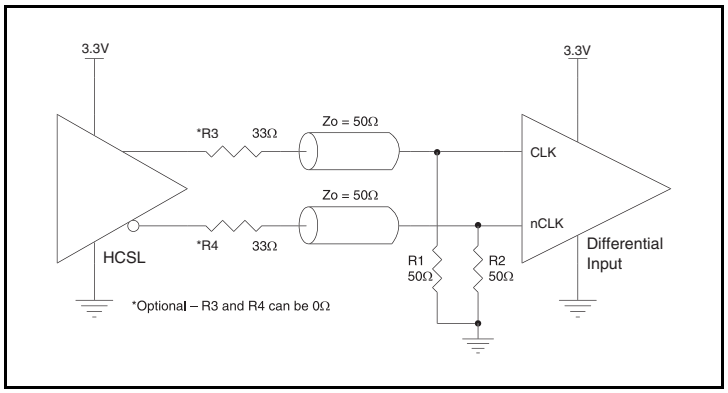


Figure 2E. CLKx/nCLKx Input Driven by a 3.3V HCSL Driver

2.5V Differential Clock Input Interface

CLKx/nCLKx accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both $V_{O(PP)}$ and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figure 3A to Figure 3E* show interface examples for the CLKx/nCLKx input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

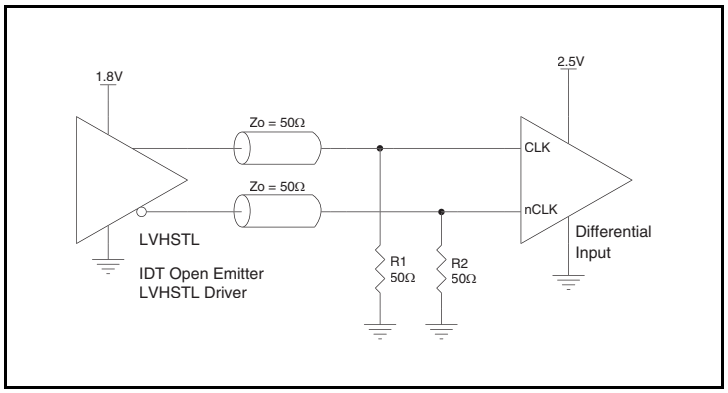


Figure 3A. CLKx/nCLKx Input Driven by an IDT Open Emitter LVHSTL Driver

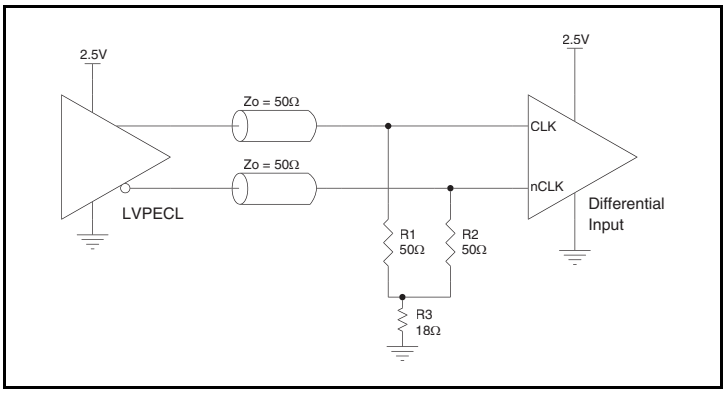


Figure 3B. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

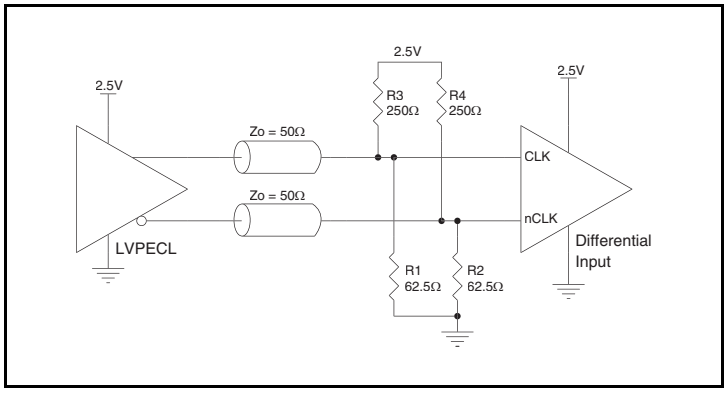


Figure 3C. CLKx/nCLKx Input Driven by a 2.5V LVPECL Driver

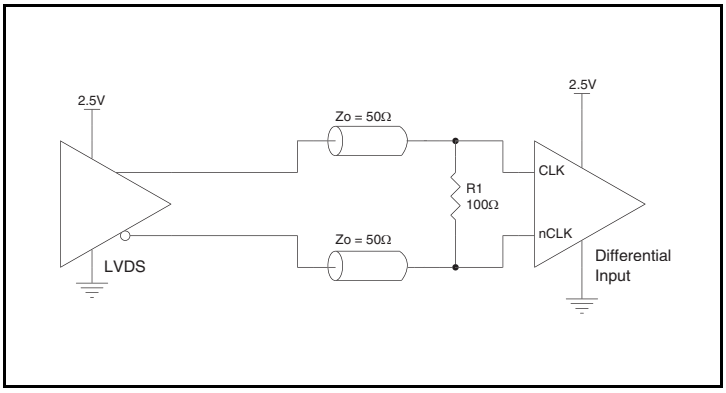


Figure 3D. CLKx/nCLKx Input Driven by a 2.5V LVDS Driver

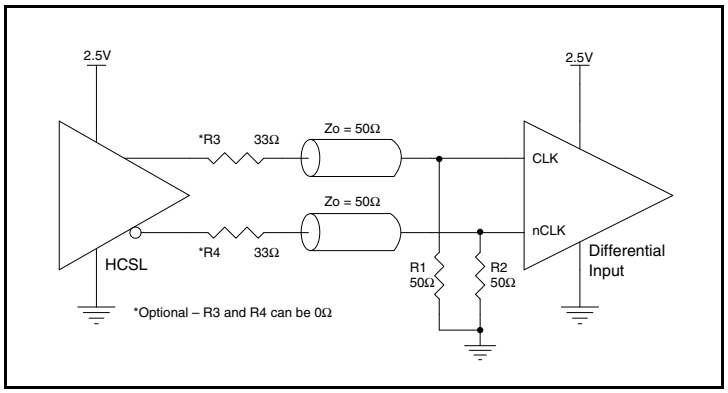


Figure 3E. CLKx/nCLKx Input Driven by a 2.5V HCSL Driver

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

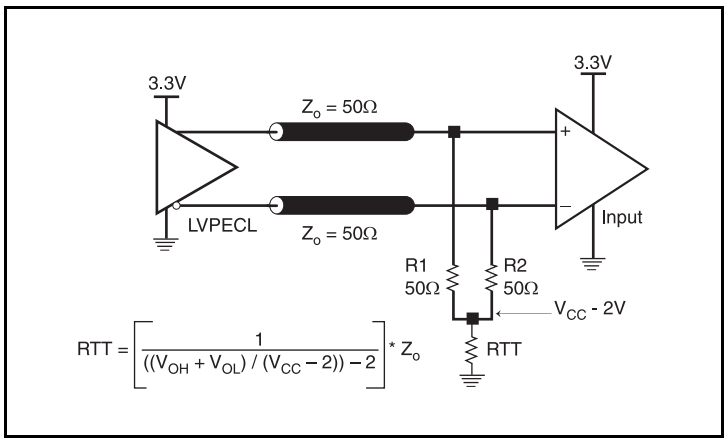


Figure 4A. 3.3V LVPECL Output Termination

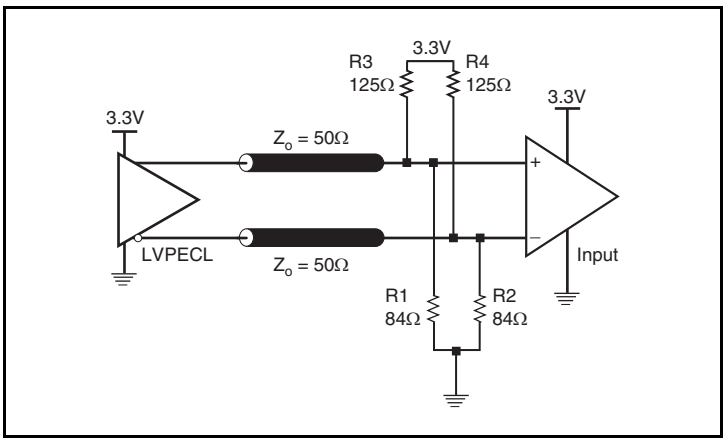


Figure 4B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 5A and Figure 5B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 5B can be eliminated and the termination is shown in Figure 5C.

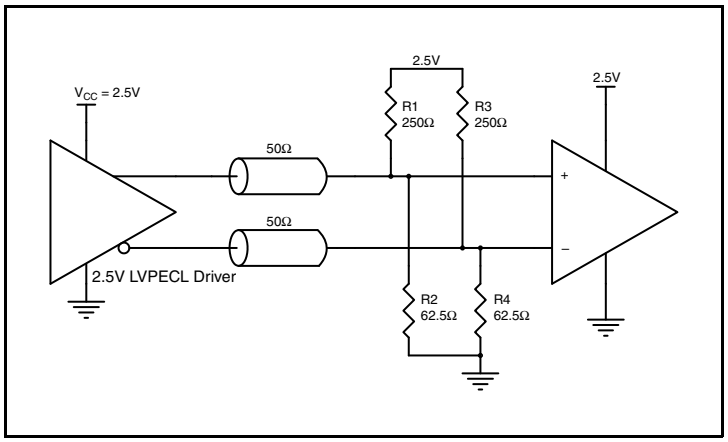


Figure 5A. 2.5V LVPECL Driver Termination Example

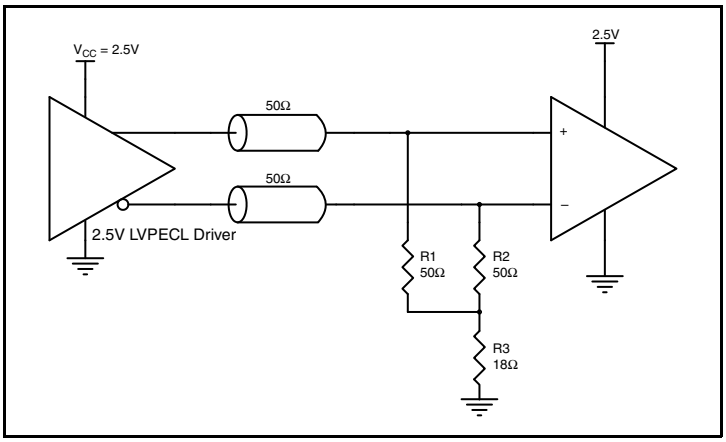


Figure 5B. 2.5V LVPECL Driver Termination Example

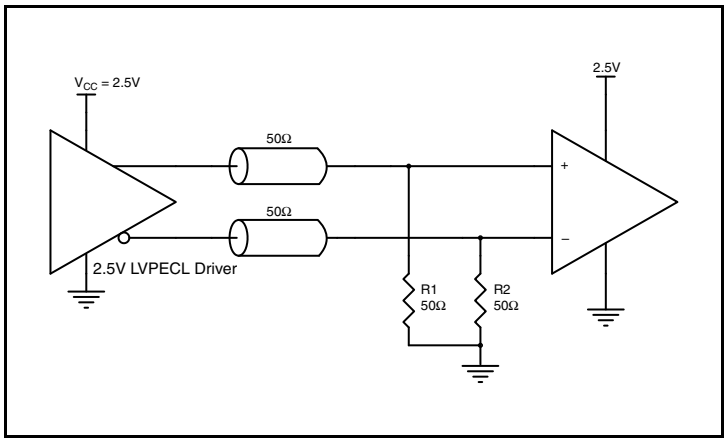


Figure 5C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T33FS314I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T33FS314I is the sum of the core power plus the power dissipated due to the load.
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 60mA = **207.9mW**
- Power (outputs)$_{MAX}$ = **33.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 * 33.2mW = **132.8mW**

  Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 207.9mW + 132.8mW = **340.7mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 115°C/W per Table 5A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.341W * 115°C/W = 124.2°C. This is within the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 5A. Thermal Resistance θ_{JA} for 20-Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	115.0°C/W	109.1°C/W	103.9°C/W

Table 5B. Thermal Resistance θ_{JA} for 20-Lead SSOP, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	100.4°C/W	92.7°C/W	87.3°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 6.*

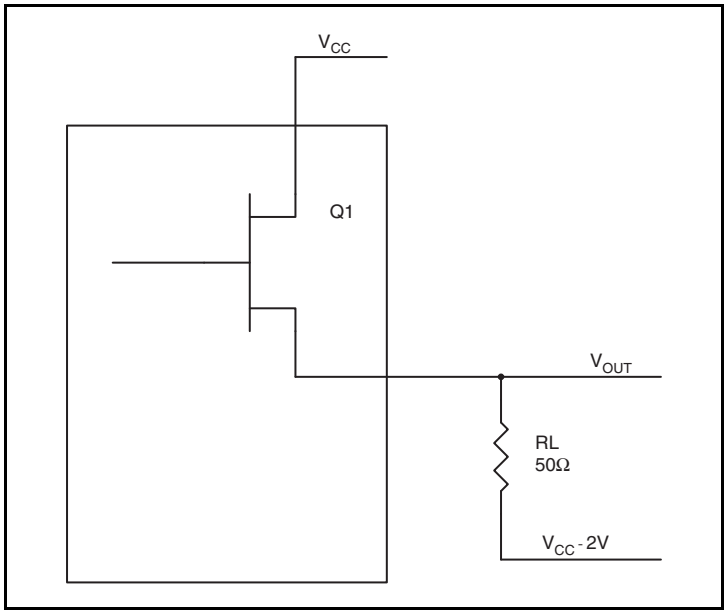


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.7V}$
  $(V_{CC\_MAX} – V_{OH\_MAX}) = \mathbf{0.7V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.5V}$
  $(V_{CC\_MAX} – V_{OL\_MAX}) = \mathbf{1.5V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.7V)/50\Omega] * 0.7V =$ **18.2mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_{L]} * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.5V)/50\Omega] * 1.5V =$ **15mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **33.2mW**

Reliability Information

Table 6A. θ_{JA} vs. Air Flow Table for a 20-Lead TSSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	115.0°C/W	109.1°C/W	103.9°C/W

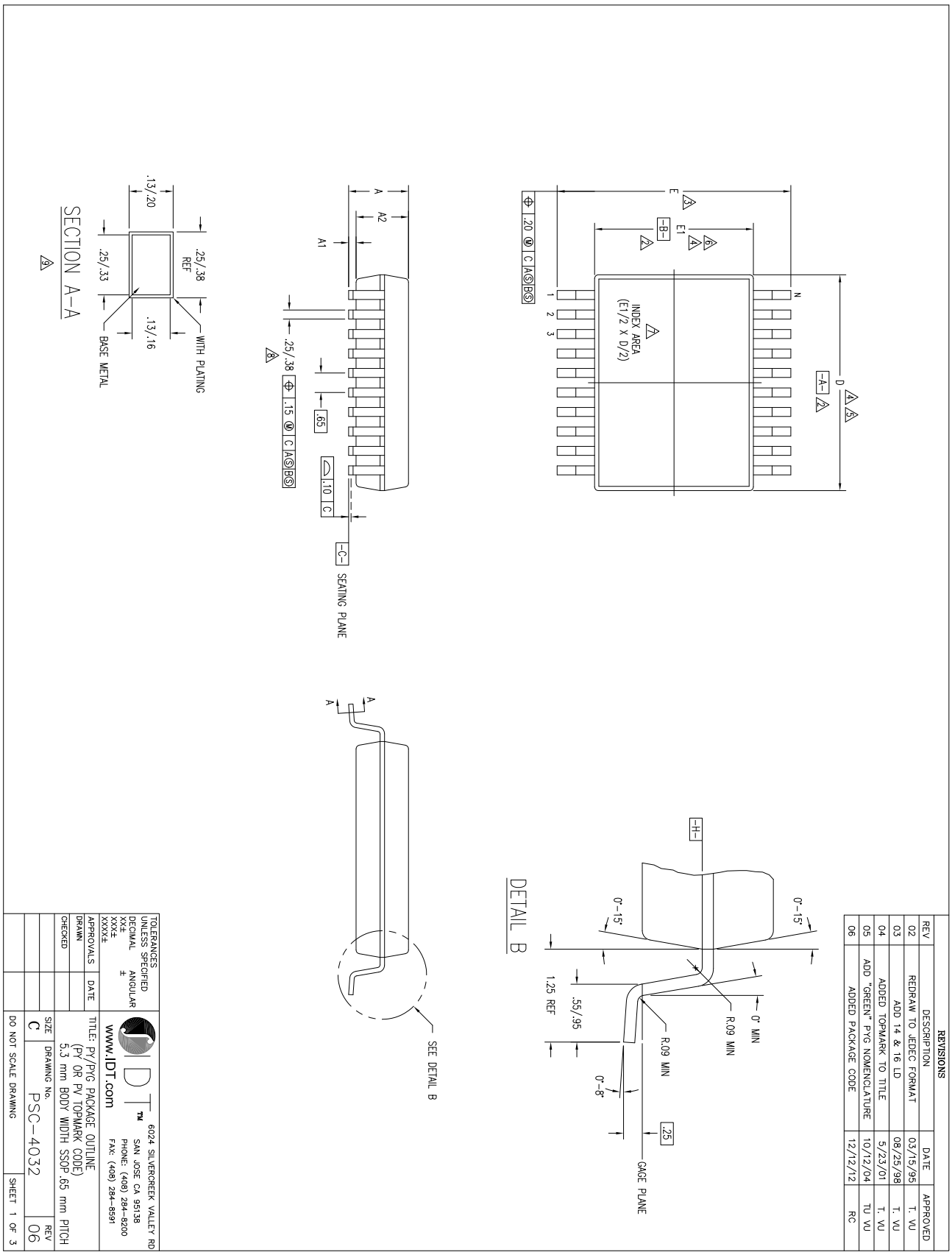
Table 6B. θ_{JA} vs. Air Flow Table for a 20-Lead SSOP

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	100.4°C/W	92.7°C/W	87.3°C/W

Transistor Count

The transistor count for IDT8T33FS314I is: 882

20-Lead SSOP Package Outline and Package Dimensions



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
02	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
03	ADD 14 & 16 LD	08/25/98	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	T. VU
05	ADD "GREEN" PYG NOMENCLATURE	10/12/04	TU VU
06	ADDED PACKAGE CODE	12/12/12	RC

SYMBOL	PY/PYG14 JEDEC VARIATION AB			NOTE	PY/PYG16 JEDEC VARIATION AC			NOTE	PY/PYG20 JEDEC VARIATION AE			NOTE	PY/PYG24 JEDEC VARIATION AG			NOTE	PY/PYG28 JEDEC VARIATION AH			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	1.73	1.86	1.99		1.73	1.86	1.99		1.73	1.86	1.99		1.73	1.86	1.99		1.73	1.86	1.99	
A1	.05	.13	.21		.05	.13	.21		.05	.13	.21		.05	.13	.21		.05	.13	.21	
A2	1.68	1.73	1.78		1.68	1.73	1.78		1.68	1.73	1.78		1.68	1.73	1.78		1.68	1.73	1.78	
D	5.90	6.20	6.50	4,5	5.90	6.20	6.50	4,5	7.07	7.20	7.33	4,5	8.07	8.20	8.33	4,5	10.07	10.20	10.33	4,5
E	7.65	7.80	7.90	3	7.65	7.80	7.90	3	7.65	7.80	7.90	3	7.65	7.80	7.90	3	7.65	7.80	7.90	3
E1	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6	5.20	5.30	5.38	4,6
N	14				16				20				24				28			

NOTES:

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6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .20 mm PER SIDE

7 DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

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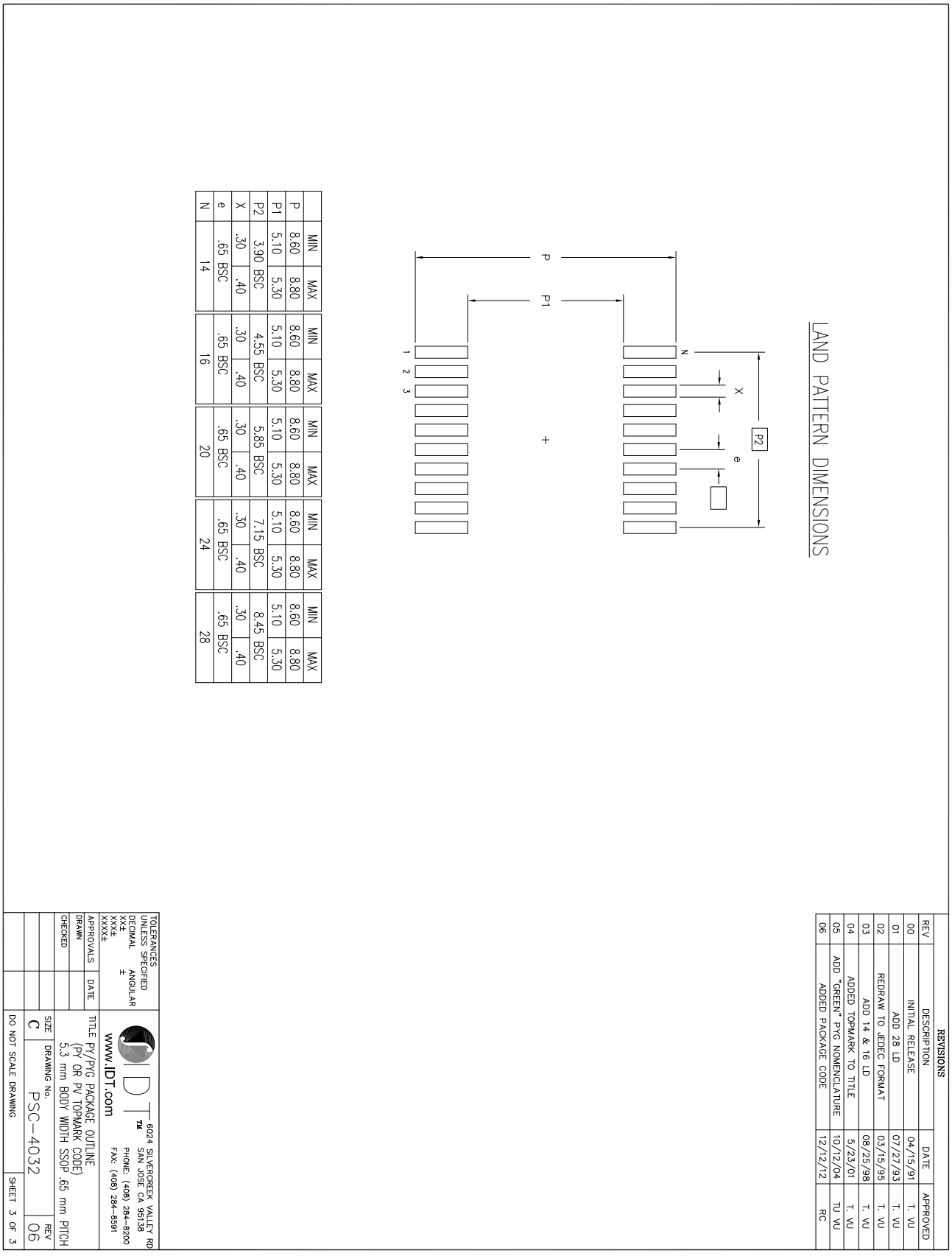
APPROVALS DATE DRAWN CHECKED	TITLE PY/PYG PACKAGE OUTLINE (PY OR PV TOPMARK CODE) 5.3 mm BODY WIDTH SSOP .65 mm PITCH		
	SIZE C	DRAWING No. PSC–4032	REV 06
	DO NOT SCALE DRAWING		SHEET 2 OF 3

20-Lead SSOP Package Outline and Package Dimensions, continued



	14		16		20		24		28	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	8.60	8.80	8.60	8.80	8.60	8.80	8.60	8.80	8.60	8.80
P1	5.10	5.30	5.10	5.30	5.10	5.30	5.10	5.30	5.10	5.30
P2	3.90 BSC		4.55 BSC		5.85 BSC		7.15 BSC		8.45 BSC	
X	.30	.40	.30	.40	.30	.40	.30	.40	.30	.40
e	.65 BSC		.65 BSC		.65 BSC		.65 BSC		.65 BSC	
N	14		16		20		24		28	

LAND PATTERN DIMENSIONS

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/15/91	T. VU
01	ADD 28 LD	07/27/93	T. VU
02	REDRAW TO JEDEC FORMAT	03/15/95	T. VU
03	ADD 14 & 16 LD	08/25/98	T. VU
04	ADDED TOPMARK TO TITLE	5/23/01	T. VU
05	ADD "GREEN" PYG NOMENCLATURE	10/12/04	TU VU
06	ADDED PACKAGE CODE	12/12/12	RC

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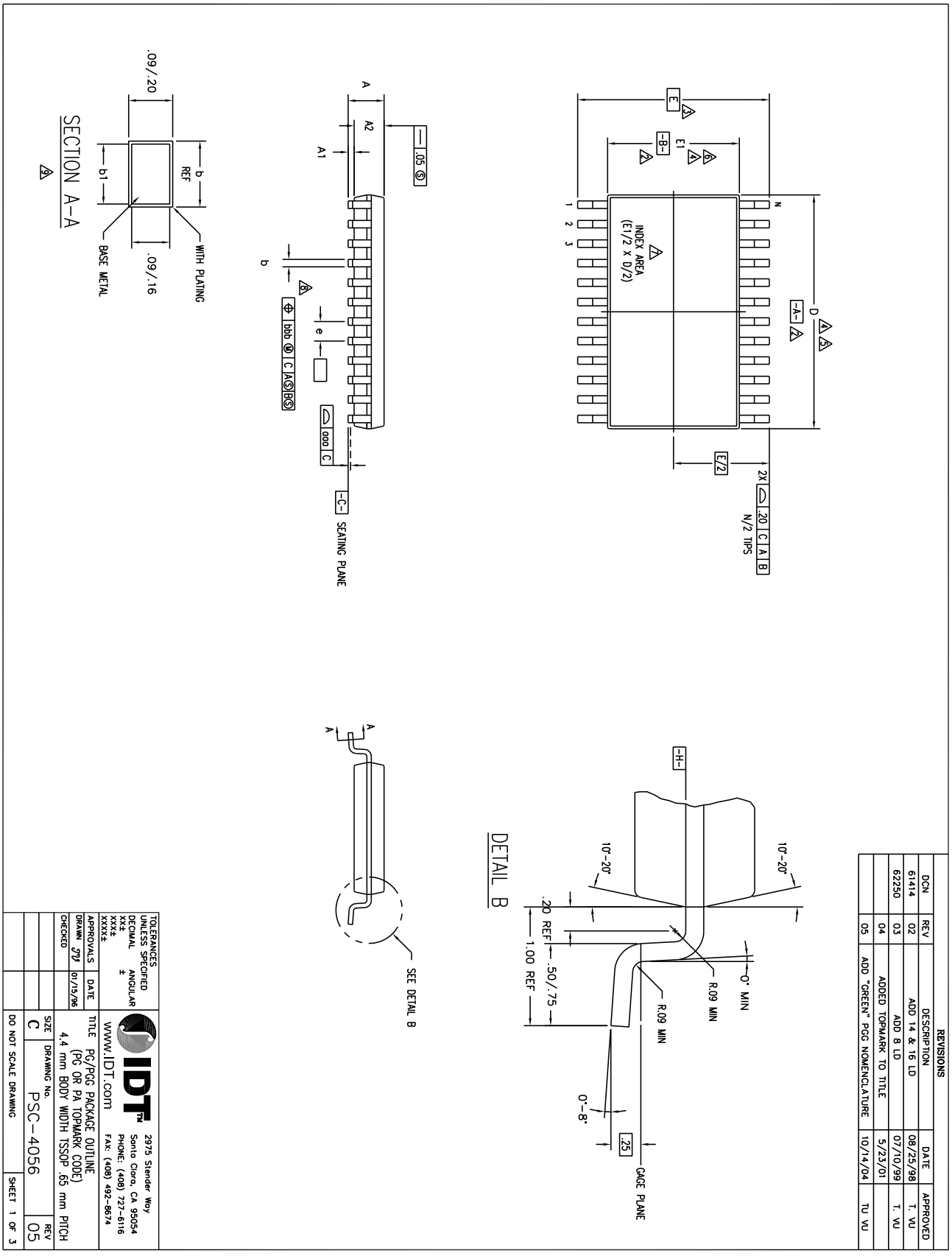
TITLE PY/PYG PACKAGE OUTLINE
(PY OR PV TOPMARK CODE)
5.3 mm BODY WIDTH SSOP .65 mm PITCH

SIZE C
DRAWING No. PSC-4032
REV 06

DO NOT SCALE DRAWING
SHEET 3 OF 3

20-Lead TSSOP Package Outline and Package Dimensions



REVISIONS				
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62250	03	ADD 8 LD	07/10/99	T. VU
	04	ADDED TOPMARK TO TITLE	5/23/01	
	05	ADD "GREEN" PGG NOMENCLATURE	10/14/04	TU VU

SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB-1			NOTE	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.20		–	–	1.20		–	–	1.20		–	–	1.20		–	–	1.20		–	–	1.20	
A1	.05	–	.15		.05	–	.15		.05	–	.15		.05	–	.15		.05	–	.15		.05	–	.15	
A2	.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05		.80	1.00	1.05	
D	2.90	3.00	3.10	4,5	4.90	5.00	5.10	4,5	4.90	5.00	5.10	4,5	6.40	6.50	6.60	4,5	7.70	7.80	7.90	4,5	9.60	9.70	9.80	4,5
E	6.40 BSC			3	6.40 BSC			3	6.40 BSC			3	6.40 BSC			3	6.40 BSC			3	6.40 BSC			3
E1	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6	4.30	4.40	4.50	4,6
e	.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC				.65 BSC			
b	.19	–	.30		.19	–	.30		.19	–	.30		.19	–	.30		.19	–	.30		.19	–	.30	
b1	.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25		.19	.22	.25	
aaa	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
bbb	–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10		–	–	.10	
N	8				14				16				20				24				28			

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

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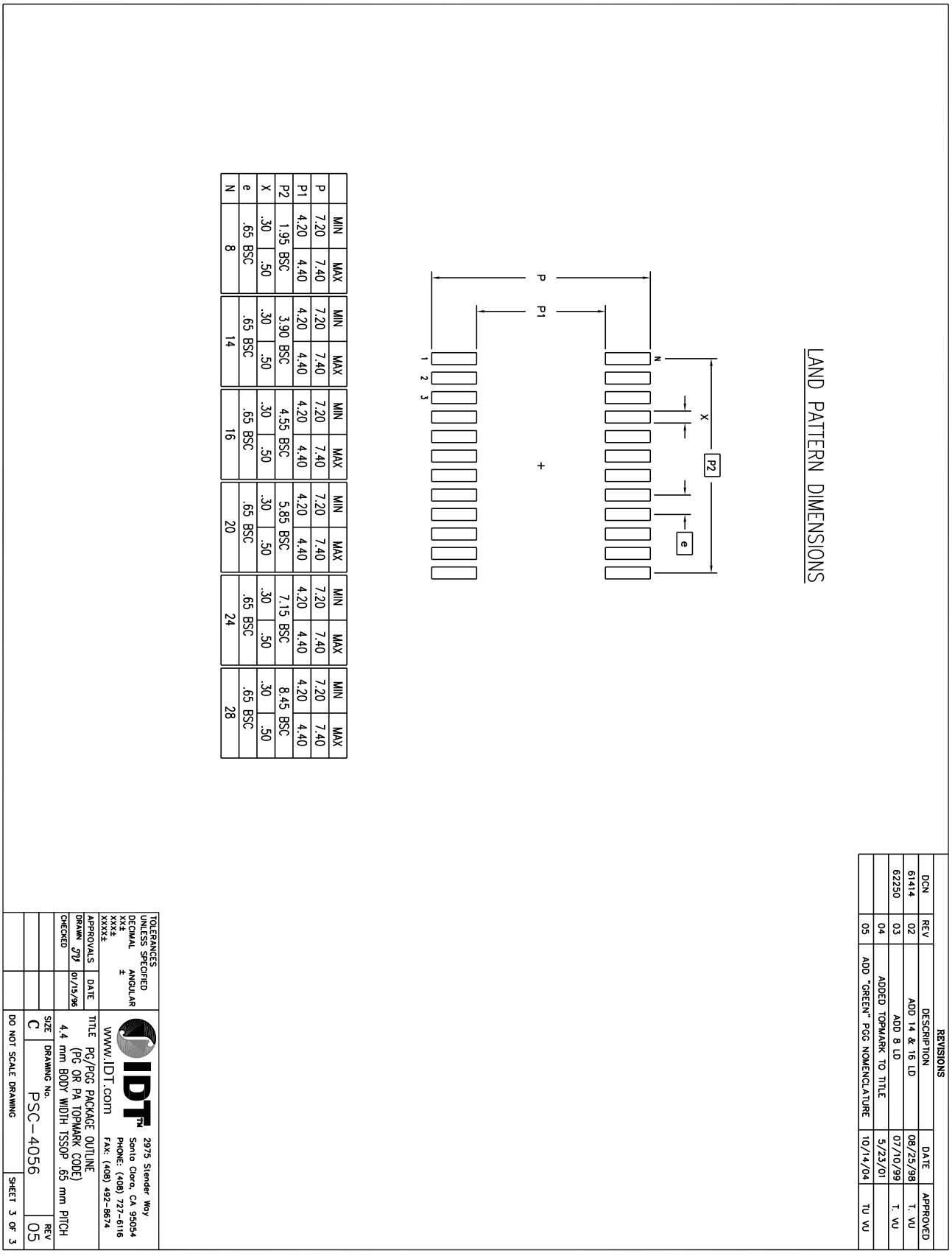
APPROVALS / DATE	TITLE	PG/PGG PACKAGE OUTLINE (PG OR PA TOPMARK CODE) 4.4 mm BODY WIDTH TSSOP .65 mm PITCH	
DRAWN JTV 01/15/96			
CHECKED			
	SIZE C	DRAWING No. PSC-4056	REV 05
	DO NOT SCALE DRAWING		SHEET 2 OF 3

20-Lead TSSOP Package Outline and Package Dimensions, continued



Ordering Information

Table 7. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T33FS314PGGI	IDT8T33FS314PGGI	“Lead-Free” 20-Lead TSSOP	Tube	-40°C to 85°C
8T33FS314PGGI8	IDT8T33FS314PGGI	“Lead-Free” 20-Lead TSSOP	Tape & Reel	-40°C to 85°C
8T33FS314PYGI	IDT8T33FS314PYGI	“Lead-Free” 20-Lead SSOP	Tube	-40°C to 85°C
8T33FS314PYGI8	IDT8T33FS314PYGI	“Lead-Free” 20-Lead SSOP	Tape & Reel	-40°C to 85°C

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(Rev.4.0-1 November 2017)

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