General Description

The IDT8T53S111I is a high-performance differential LVPECL fanout buffer. The device is designed for the fanout of high-frequency, very low additive phase-noise clock and data signals. The IDT8T53S111I is characterized to operate from a 3.3V and 2.5V power supply. Guaranteed output-to-output and part-to-part skew characteristics make the IDT8T53S111I ideal for those clock distribution applications demanding well-defined performance and repeatability. Two selectable differential inputs and ten low skew outputs are available. The integrated VREF voltage generator enables easy interfacing of single-ended signals to the device inputs. The device is optimized for low power consumption and low additive phase noise.

Features

- Ten low skew, low additive jitter LVPECL outputs
- Two selectable, differential LVPECL clock inputs
- Differential pairs can accept the following differential input levels: LVDS, LVPECL and CML
- Maximum input clock frequency: 2.5GHz
- LVCMOS interface levels for the control input (input select)
- Output skew: 15ps (typical)
- Propagation delay: 250ps (typical)
- Additive phase jitter, RMS; fREF = 156.25MHz (12kHz - 20MHz): 30fs (typical)
- Full 3.3V and 2.5V supply voltage
- Maximum device current consumption (IEE): 126mA
- Lead-free (RoHS 6) 32-Lead VFQFN package
- -40°C to 85°C ambient operating temperature

Pin Assignment

PCLK0
nPCLK0
PCLK1
nPCLK1
SEL
VREF
VOLTAGE REFERENCE

Pulldown
Pulldown
Pulldown

Q0
nQ0
Q1
nQ1
Q2
nQ2
Q3
nQ3
Q4
nQ4
Q5
nQ5
Q6
nQ6
Q7
nQ7
Q8
nQ8
Q9
nQ9

VCC
VCC
VCC
VCC
VCC
VCC
VCC
VCC

17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1

24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1

IDT8T53S111I
32-lead VFQFN
5mm x 5mm x 0.925mm package body
3.15mm x 3.15mm E-Pad
NL Package, Top View
### Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCC</td>
<td>Power</td>
<td>Power supply pin.</td>
</tr>
<tr>
<td>2</td>
<td>SEL</td>
<td>Input</td>
<td>Reference select control. See Table 3 for function. LVCMOS/LVTTL interface</td>
</tr>
<tr>
<td>3</td>
<td>PCLK0</td>
<td>Input</td>
<td>Non-inverting differential LVPECL clock/data input.</td>
</tr>
<tr>
<td>4</td>
<td>nPCLK0</td>
<td>Input</td>
<td>Inverting differential LVPECL clock input.</td>
</tr>
<tr>
<td>5</td>
<td>VREF</td>
<td>Output</td>
<td>Bias voltage generator for the nPCLK[0:1] inputs in single-ended input signal applications.</td>
</tr>
<tr>
<td>6</td>
<td>PCLK1</td>
<td>Input</td>
<td>Non-inverting differential LVPECL clock/data input.</td>
</tr>
<tr>
<td>7</td>
<td>nPCLK1</td>
<td>Input</td>
<td>Inverting differential LVPECL clock input.</td>
</tr>
<tr>
<td>8</td>
<td>VEE</td>
<td>Power</td>
<td>Negative power supply pin.</td>
</tr>
<tr>
<td>9, 16, 25, 32</td>
<td>VCCO</td>
<td>Power</td>
<td>Output power supply pins.</td>
</tr>
<tr>
<td>10, 11</td>
<td>nQ9, Q9</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>12, 13</td>
<td>nQ8, Q8</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>14, 15</td>
<td>nQ7, Q7</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>17, 18</td>
<td>nQ6, Q6</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>19, 20</td>
<td>nQ5, Q5</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>21, 22</td>
<td>nQ4, Q4</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>23, 24</td>
<td>nQ3, Q3</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>26, 27</td>
<td>nQ2, Q2</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>28, 29</td>
<td>nQ1, Q1</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
<tr>
<td>30, 31</td>
<td>nQ0, Q0</td>
<td>Output</td>
<td>Differential output pair. LVPECL interface levels.</td>
</tr>
</tbody>
</table>

**NOTE:** Pulldown and Pullup refers to an internal input resistors. See Table 2, Pin Characteristics, for typical values.

### Table 2. Pin Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIN</td>
<td>Input Capacitance</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>R_PULLDOWN</td>
<td>Input Pulldown Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td>R_PULLUP</td>
<td>Input Pullup Resistor</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

### Function Table

**Table 3A. SEL Input Selection Function Table**

<table>
<thead>
<tr>
<th>Input</th>
<th>SEL</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>PCLK0, nPCLK0 is the selected differential clock input.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>PCLK1, nPCLK1 is the selected differential clock input.</td>
</tr>
</tbody>
</table>

**NOTE:** SEL is an asynchronous control.
Absolute Maximum Ratings

NOTE: Stresses beyond those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the **DC Characteristics** or **AC Characteristics** is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

<table>
<thead>
<tr>
<th>Item</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage, $V_{CC}$</td>
<td>4.6V</td>
</tr>
<tr>
<td>Inputs, $V_I$</td>
<td>-0.5V to $V_{CC} + 0.5V$</td>
</tr>
<tr>
<td>Outputs, $I_O$ (LVPECL)</td>
<td>Continuous Current</td>
</tr>
<tr>
<td></td>
<td>Surge Current</td>
</tr>
<tr>
<td>$I_{REF}$</td>
<td>0.5mA</td>
</tr>
<tr>
<td></td>
<td>100mA</td>
</tr>
<tr>
<td>Package Thermal Impedance, $\theta_{JA}$</td>
<td>48.9°C/W (0 mps)</td>
</tr>
<tr>
<td>Storage Temperature, $T_{STG}$</td>
<td>-65°C to 150°C</td>
</tr>
</tbody>
</table>

DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics**, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$, $V_EE = 0V$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Power Supply Voltage</td>
<td>$V_{CC}$</td>
<td>3.135</td>
<td>3.3</td>
<td>3.465</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td>$V_{CC}$</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Table 4B. Power Supply DC Characteristics**, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$, $V_EE = 0V$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>Power Supply Voltage</td>
<td>$V_{CC}$</td>
<td>2.375</td>
<td>2.5</td>
<td>2.625</td>
<td>V</td>
</tr>
<tr>
<td>$I_{EE}$</td>
<td>Power Supply Current</td>
<td>$V_{CC}$</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**Table 4C. LVCMOS/LVTTL DC Characteristics**, $V_{CC} = V_{CCO} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $V_EE = 0V$, $T_A = -40°C$ to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IH}$</td>
<td>Input High Voltage</td>
<td>$V_{CC} = 3.465V$</td>
<td>2.2</td>
<td></td>
<td>$V_{CC} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.625V$</td>
<td>1.7</td>
<td></td>
<td>$V_{CC} + 0.3$</td>
<td>V</td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input Low Voltage</td>
<td>$V_{CC} = 3.465V$</td>
<td>-0.3</td>
<td>0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CC} = 2.625V$</td>
<td>-0.3</td>
<td>0.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{IH}$</td>
<td>Input High Current</td>
<td>SEL</td>
<td>$V_{CC} = V_{IN} = 3.465V$ or $2.625V$</td>
<td>150</td>
<td></td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{IL}$</td>
<td>Input Low Current</td>
<td>SEL</td>
<td>$V_{CC} = 3.465V$ or $2.625V$, $V_{IN} = 0V$</td>
<td>-10</td>
<td></td>
<td>$\mu$A</td>
</tr>
</tbody>
</table>
Table 4D. LVPECL DC Characteristics, \( V_{CC} = V_{CCO} = 3.3V \pm 5\%, V_{EE} = 0V, T_A = -40^\circ C \) to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{IH} )</td>
<td>Input High Current</td>
<td>PCLK0, nPCLK0 PCLK1, nPCLK1</td>
<td>( V_{CC} = V_{IN} = 3.465V )</td>
<td>150</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input Low Current</td>
<td>PCLK0, PCLK1 nPCLK0, nPCLK1</td>
<td>( V_{CC} = 3.465V, V_{IN} = 0V )</td>
<td>-10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{REF} )</td>
<td>Reference Voltage for Input Bias</td>
<td>( I_{REF} = 2mA )</td>
<td>( V_{CC} - 1.6 )</td>
<td>( V_{CC} - 1.1 )</td>
<td></td>
<td>( V )</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output High Voltage; NOTE 1</td>
<td></td>
<td>( V_{CCO} - 1.6 )</td>
<td>( V_{CCO} - 0.6 )</td>
<td></td>
<td>( V )</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Low Voltage; NOTE 1</td>
<td></td>
<td>( V_{CCO} - 2.0 )</td>
<td></td>
<td></td>
<td>( V )</td>
</tr>
</tbody>
</table>

NOTE: Input and output parameters vary 1:1 with \( V_{CC} \).  
NOTE 1: Outputs terminated with 50Ω to \( V_{CCO} - 2V \).

Table 4E. LVPECL DC Characteristics, \( V_{CC} = V_{CCO} = 2.5V \pm 5\%, V_{EE} = 0V, T_A = -40^\circ C \) to 85°C

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{IH} )</td>
<td>Input High Current</td>
<td>PCLK0, nPCLK0 PCLK1, nPCLK1</td>
<td>( V_{CC} = V_{IN} = 2.625V )</td>
<td>150</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Input Low Current</td>
<td>PCLK0, PCLK1 nPCLK0, nPCLK1</td>
<td>( V_{CC} = 2.625V, V_{IN} = 0V )</td>
<td>-10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{REF} )</td>
<td>Reference Voltage for Input Bias</td>
<td>( I_{REF} = 2mA )</td>
<td>( V_{CC} - 1.6 )</td>
<td>( V_{CC} - 1.1 )</td>
<td></td>
<td>( V )</td>
</tr>
<tr>
<td>( V_{OH} )</td>
<td>Output High Voltage; NOTE 1</td>
<td></td>
<td>( V_{CCO} - 1.4 )</td>
<td>( V_{CCO} - 0.8 )</td>
<td></td>
<td>( V )</td>
</tr>
<tr>
<td>( V_{OL} )</td>
<td>Output Low Voltage; NOTE 1</td>
<td></td>
<td>( V_{CCO} - 2.0 )</td>
<td></td>
<td></td>
<td>( V )</td>
</tr>
</tbody>
</table>

NOTE: Input and output parameters vary 1:1 with \( V_{CC} \).  
NOTE 1: Outputs terminated with 50Ω to \( V_{CCO} - 2V \).
### AC Electrical Characteristics

**Table 5. AC Electrical Characteristics, \( V_{CC} = V_{CCO} = 3.3V \pm 5\% \) or 2.5V \( \pm 5\% \), \( V_{EE} = 0V \), \( T_A = -40°C \) to 85°C**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{REF} )</td>
<td>Input Frequency</td>
<td>PCLK[0:1], nPCLK[0:1]</td>
<td>2.5</td>
<td>GHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{PD} )</td>
<td>Propagation Delay; NOTE 1</td>
<td>PCLK[0:1], nPCLK[0:1] to any Q[0:9], nQ[0:9] for ( V_{PP} = 0.1V ) or 0.3V</td>
<td>196</td>
<td>250</td>
<td>300</td>
<td>ps</td>
</tr>
<tr>
<td>( t_{sk(o)} )</td>
<td>Output Skew; NOTE 2, 3</td>
<td></td>
<td>15</td>
<td>50</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>( t_{sk(i)} )</td>
<td>Input Skew; NOTE 3</td>
<td></td>
<td>5</td>
<td>25</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>( t_{sk(p)} )</td>
<td>Pulse Skew</td>
<td>( f_{REF} = 50MHz )</td>
<td>14</td>
<td>38</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>( t_{sk(pp)} )</td>
<td>Part-to-Part Skew; NOTE 3, 4</td>
<td></td>
<td>17</td>
<td>115</td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>( t_{JIT} )</td>
<td>Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section</td>
<td>( f_{REF} = 156.52MHz ) Integration Range: 12kHz – 20MHz</td>
<td>30</td>
<td>120</td>
<td></td>
<td>fs</td>
</tr>
<tr>
<td>( t_{R} / t_{F} )</td>
<td>Output Rise/ Fall Time</td>
<td>20% to 80%</td>
<td>50</td>
<td>90</td>
<td>160</td>
<td>ps</td>
</tr>
<tr>
<td>MUX_ISOLATION</td>
<td>MUX Isolation; NOTE 5</td>
<td>( f_{REF} = 100MHz )</td>
<td>-75</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>( V_{PP} )</td>
<td>Input Peak-to-Peak Voltage; NOTE 5</td>
<td>( f \leq 1.5GHz )</td>
<td>0.1</td>
<td></td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f &gt; 1.5GHz )</td>
<td>0.2</td>
<td></td>
<td>1.5</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CMR} )</td>
<td>Common Mode Input Voltage; NOTE 6, 7</td>
<td></td>
<td>1.0</td>
<td></td>
<td>( V_{CCO} - 0.3 )</td>
<td>V</td>
</tr>
<tr>
<td>( V_{O(PP)} )</td>
<td>Output Voltage Swing, Peak-to-Peak</td>
<td>( f_{REF} \leq 2GHz )</td>
<td>0.5</td>
<td>0.65</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>( V_{DIFF_OUT} )</td>
<td>Differential Output Voltage Swing, Peak-to-Peak</td>
<td>( f_{REF} \leq 2GHz )</td>
<td>1.0</td>
<td>1.3</td>
<td>1.6</td>
<td>V</td>
</tr>
</tbody>
</table>

**NOTE:** Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

**NOTE 1:** Measured from the differential input crosspoint to the differential output crosspoint.

**NOTE 2:** Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the differential crosspoints.

**NOTE 3:** This parameter is defined in accordance with JEDEC Standard 65.

**NOTE 4:** Defined as skew between outputs on different devices operating at the same supply voltage, temperature, frequency and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential crosspoints.

**NOTE 5:** Qx, nQx outputs measured differentially. See *MUX Isolation diagram* in the Parameter Measurement Information section.

**NOTE 6:** \( V_{IL} \) should not be less than -0.3V.

**NOTE 7:** Common mode input voltage is defined as the crosspoint.
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

Measured using an Agilent - 5052 with a Wenzel 156.25MHz signal generator as the input source of the DUT.
Parameter Measurement Information

3.3V LVPECL Output Load AC Test Circuit

2.5V LVPECL Output Load AC Test Circuit

Differential Input Level

Output Skew

Part-to-Part Skew

Pulse Skew
Parameter Measurement Information, continued

**Input Skew**

\[ t_{sk(i)} = |t_{PD1} - t_{PD2}| \]

**MUX Isolation**

\[ MUX_{ISOL} = A_0 - A_1 \]

**Propagation Delay**

**Output Rise/Fall Time**

\[ t_R, t_F \]

\[ V_{DIFF\_OUT} \]
Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

**PCLK/nPCLK Inputs**
For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:

**LVPECL Outputs**
All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Wiring the Differential Input to Accept Single-Ended Levels

*Figure 1* shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{CC}/2$ is generated by the bias resistors $R_1$ and $R_2$. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of $R_1$ and $R_2$ might need to be adjusted to position the $V_1$ in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, $R_1$ and $R_2$ value should be adjusted to set $V_1$ at 1.25V. The values below are for when both the single ended swing and $V_{CC}$ are at the same voltage. This configuration requires that the sum of the output impedance of the driver ($R_o$) and the series resistance ($R_s$) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, $R_3$ and $R_4$ in parallel should equal the transmission line impedance. For most 50Ω applications, $R_3$ and $R_4$ can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however $V_{IL}$ cannot be less than -0.3V and $V_{IH}$ cannot be more than $V_{CC} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

![Figure 1. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels](image)
3.3V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the $V_{PP}$ and $V_{CMR}$ input requirements. *Figures 2A to 2E* show interface examples for the PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

**Figure 2A.** PCLK/nPCLK Input Driven by a CML Driver

**Figure 2B.** PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

**Figure 2C.** PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

**Figure 2D.** PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

**Figure 2E.** PCLK/nPCLK Input Driven by a 3.3V LVDS Driver
2.5V LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, LVDS, CML and other differential signals. Both signals must meet the \( V_{PP} \) and \( V_{CMR} \) input requirements. *Figures 3A to 3E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

**Figure 3A.** PCLK/nPCLK Input Driven by a CML Driver

**Figure 3B.** PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

**Figure 3C.** PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver

**Figure 3D.** PCLK/nPCLK Input Driven by a 2.5V LVPECL Driver with AC Couple

**Figure 3E.** PCLK/nPCLK Input Driven by a 2.5V LVDS Driver
VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 4. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 4. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)
Power Considerations
This section provides information on power dissipation and junction temperature for the IDT8T53S111I. Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the IDT8T53S111I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for VCC = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)\text{\text{MAX}} = V_{\text{CC,MAX}} \times I_{\text{EE,MAX}} = 3.465V \times 126mA = 436.59mW
- Power (outputs)\text{\text{MAX}} = 35mW/\text{Loaded Output pair}
  If all outputs are loaded, the total power is 10 * 35mW = 350mW

\text{Total Power}\text{\text{MAX}} (3.465V, with all outputs switching) = 436.59W + 350mW = 786.59W

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: \[ T_j = \theta_{JA} \times P_{d_{\text{total}}} + T_a \]
- Tj = Junction Temperature
- \theta_{JA} = Junction-to-Ambient Thermal Resistance
- Pd_{\text{total}} = Total Device Power Dissipation (example calculation is in section 1 above)
- T_a = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance \theta_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 48.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

\[ 85°C + 0.787W \times 48.9°C/W = 123.5°C \]

This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resistance \theta_{JA} for 32 Lead VFQFN, Forced Convection

<table>
<thead>
<tr>
<th>Multi-Layer PCB, JEDEC Standard Test Boards</th>
<th>0</th>
<th>1</th>
<th>2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Meters per Second</td>
<td>48.9°C/W</td>
<td>42.0°C/W</td>
<td>39.4°C/W</td>
</tr>
</tbody>
</table>
3. Calculations and Equations.
The purpose of this section is to calculate the power dissipation for the LVPECL output pair.
LVPECL output driver circuit and termination are shown in Figure 5.

![LVPECL Driver Circuit and Termination](image)

To calculate power dissipation per output pair due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.6V$
  
  
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.6V$

- For logic low, $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.3V$
  
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.3V$

$P_{d\_H}$ is power dissipation when the output drives high.

$P_{d\_L}$ is the power dissipation when the output drives low.

\[
P_{d\_H} = \left(\frac{V_{OH\_MAX} - (V_{CCO\_MAX} - 2V)}{R_L}\right) \times (V_{CCO\_MAX} - V_{OH\_MAX}) = \left(\frac{2V - (V_{CCO\_MAX} - V_{OH\_MAX})}{50\Omega}\right) \times 0.6V = 16.8\text{mW}
\]

\[
P_{d\_L} = \left(\frac{V_{OL\_MAX} - (V_{CCO\_MAX} - 2V)}{R_L}\right) \times (V_{CCO\_MAX} - V_{OL\_MAX}) = \left(\frac{2V - (V_{CCO\_MAX} - V_{OL\_MAX})}{50\Omega}\right) \times 1.3V = 18.2\text{mW}
\]

Total Power Dissipation per output pair = $P_{d\_H} + P_{d\_L} = 35\text{mW}$
Reliability Information

Table 7. $\theta_{JA}$ vs. Air Flow Table for a 32 Lead VFQFN

<table>
<thead>
<tr>
<th>Meters per Second</th>
<th>$\theta_{JA}$ at Air Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>Multi-Layer PCB, JEDEC Standard Test Boards</td>
<td>0: 48.9°C/W</td>
</tr>
</tbody>
</table>

Transistor Count

The transistor count for the IDT8T53S111I is: 342
### Ordering Information

#### Table 8. Ordering Information

<table>
<thead>
<tr>
<th>Part/Order Number</th>
<th>Marking</th>
<th>Package</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>8T53S111NLGI</td>
<td>IDT8T53S111NLGI</td>
<td>“Lead-Free” 32 Lead VFQFN</td>
<td>Tray</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>8T53S111NLGI8</td>
<td>IDT8T53S111NLGI</td>
<td>“Lead-Free” 32 Lead VFQFN</td>
<td>Tape &amp; Reel</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>

NOTE: Parts that are ordered with a “G” suffix to the part number are the Pb-Free configuration and are RoHS compliant.
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